10. IC SPEC

DVI

Consumer Component Interfaces

DigitalVisual Interface (DVI)

DVI was developed for transferring uncompressed digital video from a computer to a display monitor. It may also be used for interfacing devices such as settop boxes to televisions. DVI enhances the Digital Flat Panel (DFP) Interface by supporting more formats and timings, and supporting the High-bandwidth Digital Content Protection (HDCP) specification to ensure unauthorized copying of material is prevented. The interface supports VESA's Extended Display Identification Data (EDID) standard, Display Data Channel (DDC) standard, and Monitor Timing Specification (DMT). DDC and EDID enable automatic display detection and configuration. "TFT data mapping" is supported as the minimum requirement: one pixel per clock, eight bits per channel, MSB justified.

DVI uses transition-minimized differential signaling (TMDS). Eight bits of video data are converted to a 10-bit transition-minimized, DC-balanced value, which is then serialized. The receiver deserializes the data, and converts it back to eight bits. Thus, to transfer digital R'G'B' or YCbCr data requires three TMDS signals that comprise one TMDS link.

To further enhance DVI for the consumer market, Silicon Image developed a method of transferring digital audio over the existing clock channel.

TMDS Links

Either one or two TMDS links may be used, as shown in Figures 1. and 2. depending on the formats and timing required. A system supporting two TMDS links must be able to switch dynamically between formats requiring a single link and formats requiring a dual link.

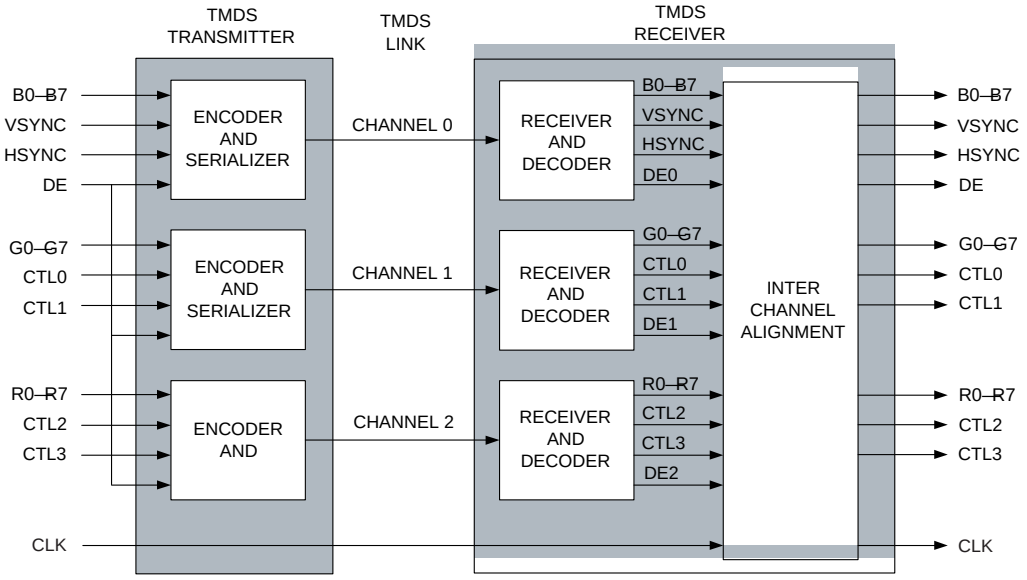

Figure1. DVI Single TMDS Link.

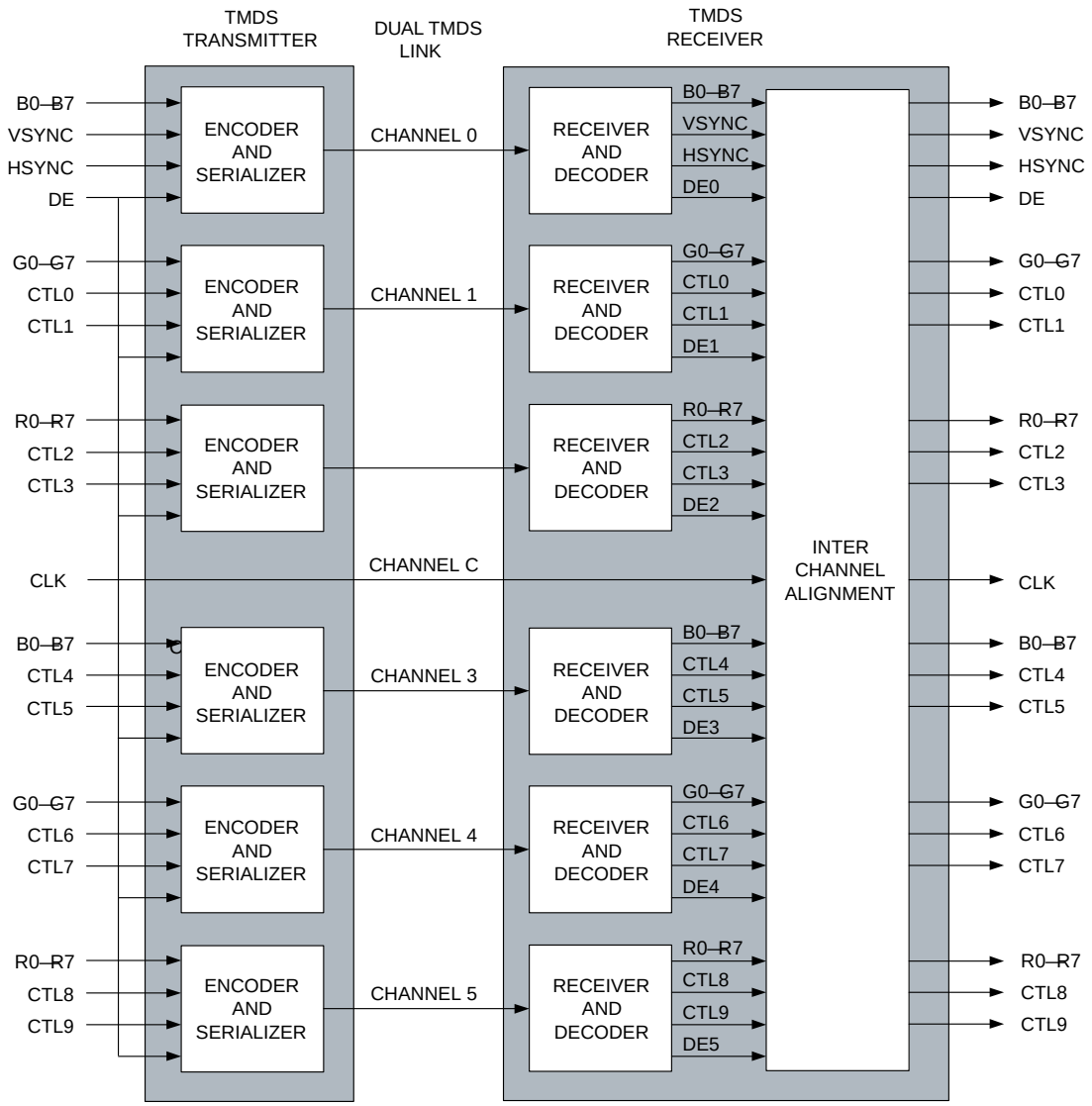

Figure 2. DVI Dual TMDS Link.

A single TMDS link is used to support all formats and timings requiring a clock rate of 25-165 MHz. Formats and timings requiring a clock rate >165 MHz are implemented using two TMDS links, with each TMDS link operating at one-half the frequency. Thus, the two TMDS links share the same clock and the bandwidth is shared evenly between the two links.

Video Data Formats

Typically, 24-bit R'G'B' data is transferred over a link, although any data format may be used, including 24-bit YCbCr for consumer applications. For applications requiring more than eight bits per color component, the second TMDS link may be used for the additional least significant bits.

Control Signals

In addition to the video data, there are up to 14 control signals:

HSYNC	horizontal sync
VSYNC	vertical sync
DE	data enable
CTL0-CTL3	reserved (link 0)
CTL4-CTL9	reserved (link 1)
CLK	1x sample clock

While DE is a "1," active video is processed. While DE is a "0," the HSYNC, VSYNC and CTL0-CTL9 signals are processed. HSYNC and VSYNC may be either polarity.

Digital-Only Connector

The digital-only connector, which supports dual link operation, contains 24 contacts arranged as three rows of eight contacts, as shown in Figure 3. Table 5. lists the pin assignments.

Digital-Analog Connector

In addition to the 24 contacts used by the digital-only connector, the 29-contact digital-analog connector contains five additional contacts to support analog video as shown in Figure 4. Table 6. lists the pin assignments.

HSYNC	horizontal sync
VSYNC	vertical sync
RED	analog red video
GREEN	analog green video
BLUE	analog blue video

The operation of the analog signals is the same as for a standard VGA connector.

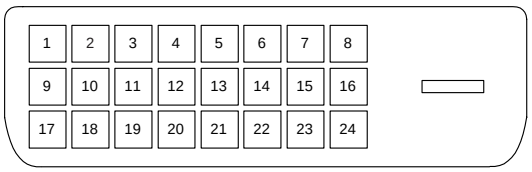

Figure 3. DVI Digital-Only Connector.

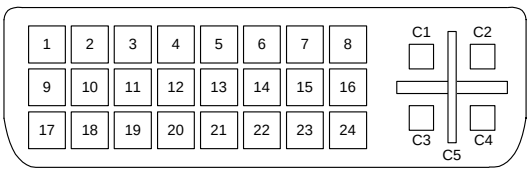

Figure 4. DVI Digital-Analog Connector.

Pin	Signal	Pin	Signal	Pin	SIgnal
1	D2-	9	D1-	17	D0-
2	D2	10	D1	18	D0
3	shield	11	shield	19	shield
4	D4-	12	D3-	20	D5-
5	D4	13	D3	21	D5
6	DDC SCL	14	+5V	22	shield
7	DDC SDA	15	ground	23	CLK
8	reserved	16	Hot Plug Detect	24	CLK-

Table 5. DVI Digital-Only Connector Signal Assignments.

Pin	Signal	Pin	Signal	Pin	SIgnal
1	D2-	9	D1-	17	D0-
2	D2	10	D1	18	D0
3	shield	11	shield	19	shield
4	D4-	12	D3-	20	D5-
5	D4	13	D3	21	D5
6	DDC SCL	14	+5V	22	shield
7	DDC SDA	15	ground	23	CLK
8	VSYNC	16	Hot Plug Detect	24	CLK-
C1	RED	C2	GREEN	C3	BLUE
C4	HSYNC	C5	ground		

Table 6. DVI Digital-Analog Connector Signal Assignments.

1 PRODUCT OVERVIEW

OVERVIEW

S5H2000X is an HDTV signal processing IC for digital broadcasting. It is also referred to as SAM2K-LITE.For optimum performance, SAM2K-LITE has been designed to work with built-in HDTVs or HD set-top boxes.It contains HDTV signal processing functions in a single unit and thus-allows you to easily construct a set.

This User's Manual is designed to help developers, who have a basic knowledge of MPEG and PCI, to develop STB or HDTV applications using SAM2K-LITE.

This manual contains the following topics.

- General feature
- Block diagram
- System diagram
- Pin & Control register description
- Internal module description
    - TS Demux
    - PCI interface
    - Audio interface
    - MPEG decoder
    - Display processor
    - Graphic processor
    - Memory interface
- Electrical characteristics and timing spec
- PKG information

GENERAL Features

- ARM7TDMI RISC CPU
  - Used for programmable TS demux
  - 67.5MHz speed @ 1.8V ±0.15V
  - 12Kbyte SRAM
- External memory interface
  - 64bit wide SDRAM interface
  - 64Mbit(32bit wide) x 4 or 64Mbit(32bit wide) x 2 SDRAM support @ CAS latency 3
- TS (Transport Stream) Demux engine
  - S/W demux architecture using ARM7TDMI
  - MPEG-2 or DSS TS demux support
  - DVB, ATSC support
  - Built-in DES descrambler
  - Up to 32 PIDs can be received at the same time
  - CRC(MPEG-2 : 32bit, DSS : 16bit) support
  - Video packets are transmitted to external SDRAM via DMA1.
  - Audio packets are transmitted to the host CPU's memory via PCI interface.
  - Allows filtering of desired information from the PSI packet and transmitting to the host CPU.
  - Built-in clock recovery circuit for programmable clock recovery.
- MPEG Video decoder
  - ISO/IEC 11172-2 (MPEG1) format support
  - SO/IEC 13818-2 MP@HL (MPEG2) format support
  - DSS MPEG1 format support
  - DSS MPEG2 SD and HD format support
- Display processor
  - 4 display planes (background, video, OSD, cursor plane)
  - Letter box, pan/scan display
  - Pillar-box (side well) / panorama display
  - 3D IPC support
  - PIP support
  - Flexible color space conversion support
- Various video inputs
  - TS stream input
  - Digital HD (RGB) input (24bit)
  - Digital SD input (8bit)
- Various video output formats
  - Digital HD video output (1080i, 720p, 480p, RGB/YCbCr)
  - Analog HD video output (RGB/YPbPr without sync or with 3 level sync)
  - Analog SD video output (CVBS, S-video)
- Graphic processor
  - 4 Graphic windows (on the OSD plane)
  - Blending (window or pixel blending, window and pixel blending)
  - H/W cursor
  - 2D Graphic accelerator
- Audio input
  - Audio stream or PCM input (through PCI bus)
  - External PCM input
- Audio output
  - IEC958 (SPDIF) audio output interface
  - I2S audio output interface
- On-chip peripherals
  - PCI interface (32bit, 66MHz)
  - I2C
- JTAG interface (for ARM7 only)
- Package
  - 352 pin TBGA

BLOCK DIAGRAM

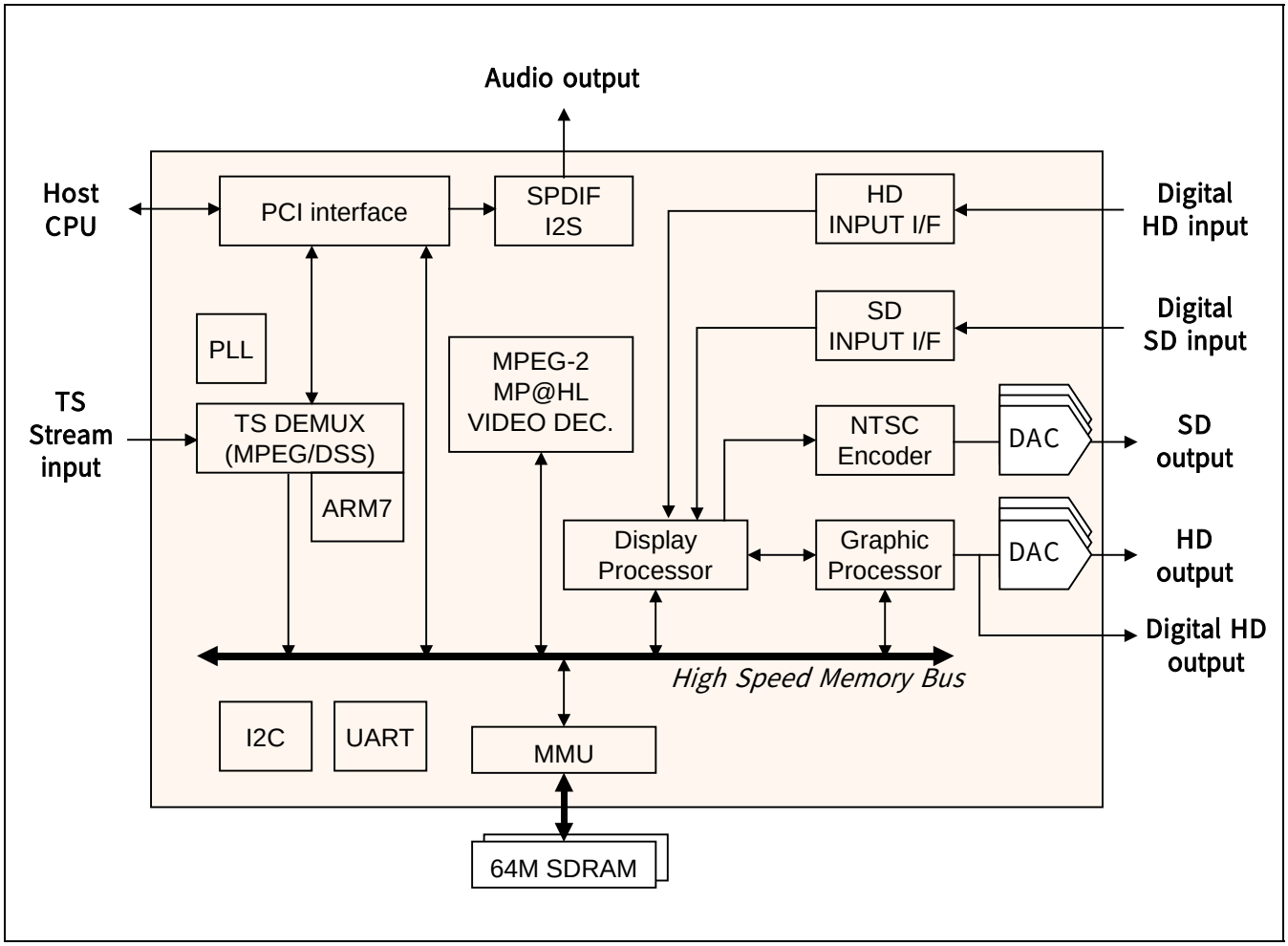

Figure 1-1. S5H2000X Block diagram

SYstem diagram

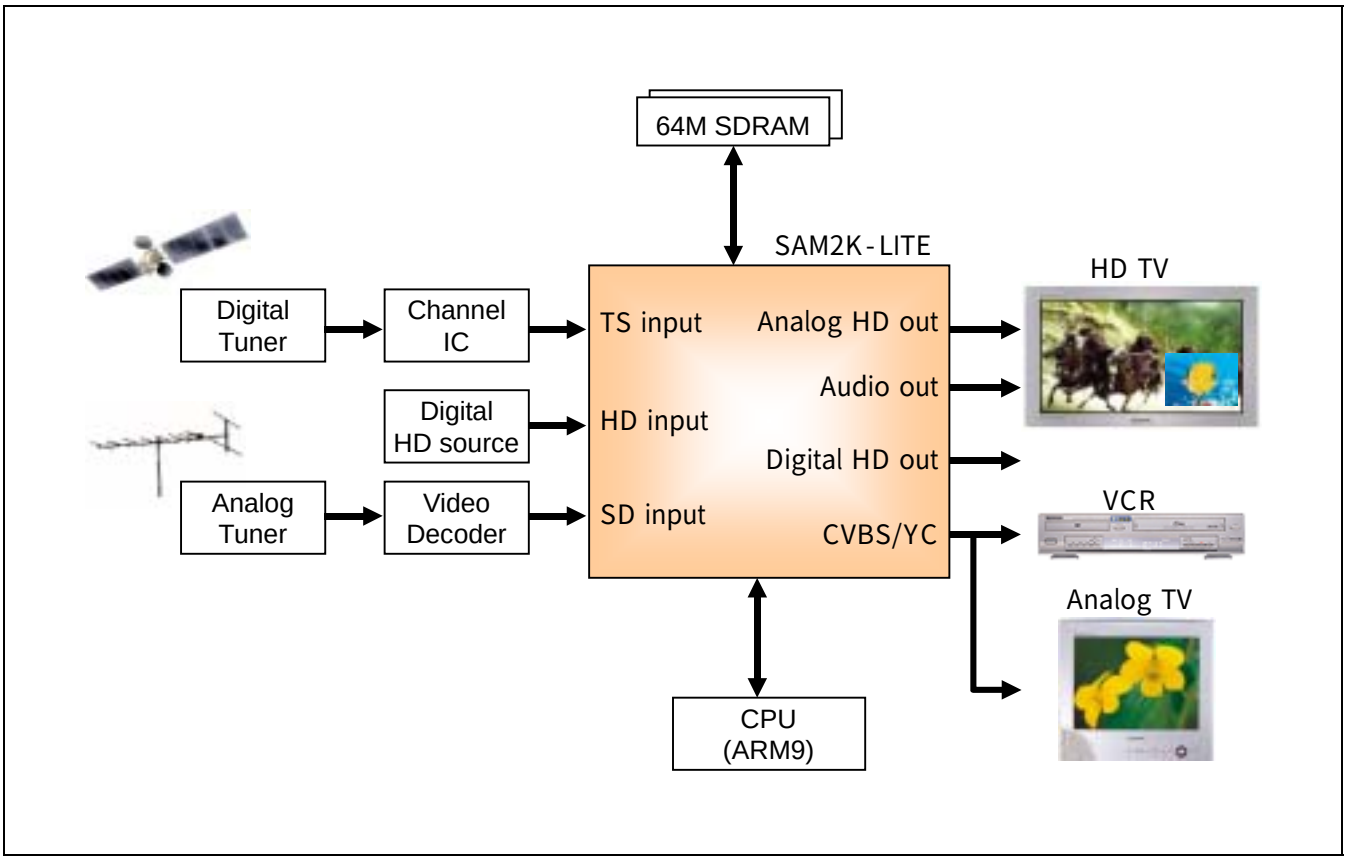

Figure 1-2 system diagram

pin assignments for 352 FBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	PVDDOP	PVSSI	MDATA7	MDQM1	MDATA3	PVSSI	PVDDOP	HOB7	PVSSOP	PVDDOP	HOB0	HOG6	PVDDOP
B	MDQM2	PVDDOP	MDATA 10	PVDDOP	MDATA5	PVSSOP	PVDDI	HO VSYNC	HOB5	HOB3	HOB1	FT24	HOG3
C	MDATA 18	MDATA 16	MDATA 13	MDATA 11	MDATA9	MDATA6	MDATA1	MDQM0	HVID CLK	HOB6	HOB2	FT135	HOG4
D	MDATA 19	MDATA 17	MDATA 14	MDATA 12	PVDDI	MDATA8	MDATA4	MDATA2	MDATA0	HO HSYNC	HOB4	HOG7	HOG5
E	PVDDI	PVSSI	PVSSOP	MDATA 15									
F	MDATA 25	MDQM3	MDATA 21	MDATA 20									
G	MDATA 26	MDATA 24	MDATA 23	MDATA 22									
H	MDATA 31	MDATA 28	MDATA 27	PVSSOP									
J	PVSSOP	MDATA 30	PVSSOP	MDATA 29									
K	nMCS1	nMWE	nMCAS	nMRAS									
L	MCKE	nMCS0	PVDDI	PVSSI									
M	MBA1	MBA0	PVDDOP	MCLK									
N	MADDR 3	MADDR 2	MADDR 1	MADDR 0									
P	PVDDOP	MADDR 4	MADDR 5	MADDR 6									
R	PVSSI	PVDDI	MADDR 7	MADDR 8									
T	MADDR 9	PVDDOP	MADDR 10	MDQM4									
U	MDATA 32	MDATA 33	MDATA 34	MDATA 35									
V	PVSSOP	PVDDOP	MDATA 36	MDATA 38									
W	MDATA 37	PVSSI	PVDDI	PVDDOP									
Y	MDATA 39	MDATA 40	MDATA 42	MDATA 43									
AA	MDQM5	MDATA 41	MDATA 46	MDQM6									
AB	MDATA 44	MDATA 45	MDATA 47	MDATA 50									
AC	PVDDOP	PVSSI	MDATA 51	MDATA 53	MDATA 55	MDATA 56	PVSSOP	MDATA 63	PDATA2	PDATA4	PDATA9	PDATA 13	PDATA 14
AD	MDATA 48	PVDDI	MDATA 52	MDATA 54	PVDDOP	MDATA 59	PVSSI	PDATA1	PVDDOP	PDATA8	PDATA 10	PVSSOP	PDATA 15
AE	MDATA 49	PVSSOP	PVSSI	PVDDI	MDATA 60	MDATA 61	PVDDI	PDATA3	PDATA7	nPCBE1	PDATA 11	PVSSI	nPLOCK
AF	PVDDOP	MDQM7	MDATA 57	MDATA 58	MDATA 62	nPCBE0	PDATA0	PDATA5	PDATA6	PVDDOP	PDATA 12	PVDDI	PVSSOP

3.3V

1.8V

0V

	14	15	16	17	18	19	20	21	22	23	24	25	26
A	aRPR	PAVSST_HD1	aHIRS	aY	PVSSOP	PAVSST_SD2	aCVBS	HOG1	HOG5	HOR1	HOR2	SI VSYNC	PVDDOP
B	aBPB	PAVDDT_HD1	aGY	PAVBB_DAC	PAVSST_SD1	aSCOMP	PVSSOP	HOG0	HOR4	SICLK	SI HSYNC	PVSSOP	SIFLD
C	aHVREF	PAVDDT_HD2	PAVDDI_DAC	aSIRS	PAVDDT_SD2	aC	HOR7	HOR3	PVDDOP	SIDATA6	SIDATA3	SIDATA2	SIDATA0
D	aHCOMP	PAVSST_HD2	PVSSI_DAC	PAVDDT_SD1	aSVREF	HOG2	HOR6	HOR0	SIDATA7	SIDATA5	SIDATA1	SCANEN	PVDDI
E										SIDATA4	TSTON	PVDDOP	HIB7
F										PVSSI	HI HSYNC	HI VSYNC	HIB3
G										HICLK	HIB5	HIB4	HIB2
H										HIB6	HIB1	HIG7	HIG5
J										PVDDOP	HIB0	HIG6	HIG4
K										HIG3	HIG2	HIG1	HIR7
L										HIG0	PVDDI	PVSSI	PVDDOP
M										HIR6	HIR5	HIR4	HIR3
N										HIR2	HIR1	HIR0	PVDDI_PLL
P										PAVDDT_PLL	aPLL2	aPLL1	PVSSI_PLL
R										IBCLK	PAVSST_PLL	PAVBB_PP	aPLL3
T										OLRCLK	IPCM	PVDDOP	ILRCLK
U										OHDCLK	OSPDIF	OBCLK	ODCLK
V										PVDDI	JTDI	IVOH	OADATA
W										PWM	JTMS	nJTRST	JTDO
Y										TSCLK	CLK27M	nRESET	JTCK
AA										TSDATA1	TSDATA7	PVDDOP	PVSSI
AB										I2CCLK	TSDATA4	TSVLD	BEND
AC	nPPERR	nPISEL	nPSTOP	nPCBE2	PVDDOP	PDATA23	PVDDOP	PDATA28	PDATA31	I2CDAT	TSDATA0	TSDATA3	TSDATA6
AD	nPSERR	nPGNT	PVDDOP	nPTRDY	PDATA17	PDATA18	PDATA22	PVDDI	PDATA27	PCISEL	PVSSI	PVDDI	TSDATA5
AE	PVDDOP	PCLK	nPDSEL	nPFRM	PVSSI	PDATA16	PDATA21	PDATA24	PVSSI	PDATA25	PDATA29	PVSSOP	TSDATA2
AF	nPINT	nPRST	nPREQ	nPIRDY	PVDDI	PPAR	PDATA19	PDATA20	nPCBE3	PDATA26	PVSSOP	PDATA30	PVDDOP

SAMSUNG ELECTRONICS

PIN DESCRIPTION

Table 1-1. S5H2000X Pin Descriptions (System)

Pin Name	Pin Type	Pin Description	Circuit Type	Pin Number	Share Pins
nRESET	I	System Reset (Active Low)		Y25	–
CLK27M	I	SYSTEM Clock		Y24	–
PWM	O	PWM Output for clock recovery		W23	–
BEND	I	Big (High) or Little (Low) Endian		AB26	–
OHDCLK	O	HD clock output		U23	–
IVOH	I	TEST PIN		V25	–
TSTON	I	TEST PIN		E24	–
SCAN_EN	I	TEST PIN		D25	–
FT24	I	24.576MHz Clock Input for TEST		B12	–
FT135	I	135MHz Clock Input for TEST		C12	–
aPLL1	AO	PLL Loop Filter		P25	–
aPLL2	AO	PLL Loop Filter		P24	–
aPLL3	AO	PLL Loop Filter		R26	–

Table 1-1. S5H2000X Pin Descriptions (Continued: Debugger)

Pin Name	Pin Type	Pin Description	Circuit Type	Pin Number	Share Pins
JTDI	I	JTAG Input		V24	–
JTDO	O	JTAG Output		W26	–
JTCK	I	JTAG Clock		Y26	–
nJTRST	I	JTAG Reset (Active Low)		W25	–
JTMS	I	JTAG Mode Select		W24	–

Table 1-1. S5H2000X Pin Descriptions (Continued: I2C)

Pin Name	Pin Type	Pin Description	Circuit Type	Pin Number	Share Pins
I2CCLK	O	I2C Clock Output		AB23	–
I2CDATA	I/O	I2C DATA		AC23	–

Table 1-1. S5H2000X Pin Descriptions (Continued: PCI)

Pin Name	Pin Type	Pin Description	Circuit Type	Pin Number	Share Pins
PDATA31 ~ PDATA24	I/O	32bit PCI Data and Address (33MHz)		AC22 AF25 AE24 AC21 AD22 AF23 AE23 AE21	–
PDATA23 ~ PDATA16	I/O	32bit PCI Data and Address (33MHz)		AC19 AD20 AE20 AF21 AF20 AD19 AD18 AE19	
PDATA15 ~ PDATA8	I/O	32bit PCI Data and Address (33MHz)		AD13 AC13 AC12 AF11 AE11 AD11 AC11 AD10	
PDATA7 ~ PDATA0	I/O	32bit PCI Data and Address (33MHz)		AE9 AF9 AF8 AC10 AE8 AC9 AD8 AF7	

Table 1-1. S5H2000X Pin Descriptions (Continued: PCI)

Pin Name	Pin Type	Pin Description	Circuit Type	Pin Number	Share Pins
nPCBE3 ~ nPCBE0	I/O	4bit PCI Bus Commend and Byte Enable		AF22 AC17 AE10 AF6	–
PPAR	I/O	PCI parity		AF19	
nPFRM	I/O	PCI cycle frame (Active LOW)		AE17	
nPTRDY	I/O	PCI target ready (Active LOW)		AD17	
nPIRDY	I/O	PCI initiator ready (Active LOW)		AF17	
nPSTOP	I/O	PCI stop (Active LOW)		AC16	
nPDSEL	I/O	PCI device select (Active LOW)		AE16	
nPREQ	O	PCI Bus request (Active LOW)		AF16	
nPISEL	I	PCI initialization device select (Active LOW)		AC15	
nPGNT	I	PCI Bus grant (Active LOW)		AD15	
PCLK	I	PCI clock		AE15	
nPRST	I	PCI reset (Active LOW)		AF15	
nPPERR	I/O	PCI parity error (Active LOW)		AC14	
nPSERR	O	PCI system error (Active LOW)		AD14	
nPINT	O	PCI interrupt signal (Active LOW)		AF14	
nPLOCK	I/O	PCI lock signal (Active LOW)		AE13	
PCISEL	I	PCI operation voltage selection (fixed 0V)		AD23	

Table 1-1. S5H2000X Pin Descriptions (Continued: TS DEMUX)

Pin Name	Pin Type	Pin Description	Circuit Type	Pin Number	Share Pins
TSDATA7 ~ TSDATA0	I	8bit Transport Stream DeMux Input		AA24 AC26 AD26 AB24 AC25 AE26 AA23 AC24	
TSCLK	I	Transport Stream DeMux Clock		Y23	

TSVLD	I	Transport Stream DeMux Valid		AB25	

Table 1-1. S5H2000X Pin Descriptions (Continued: SDRAM)

Pin Name	Pin Type	Pin Description	Circuit Type	Pin Number	Share Pins
MDATA63 ~ MDATA56	I/O	64bit SDRAM Data		AC8 AF5 AE6 AE5 AD6 AF4 AF3 AC6	
MDATA55 ~ MDATA48	I/O	64bit SDRAM Data		AC5 AD4 AC4 AD3 AC3 AB4 AE1 AD1	
MDATA47 ~ MDATA40	I/O	64bit SDRAM Data		AB3 AA3 AB2 AB1 Y4 Y3 AA2 Y2	
MDATA39 ~ MDATA32	I/O	64bit SDRAM Data		Y1 V4 W1 V3 U4 U3 U2 U1	

Table 1-1. S5H2000X Pin Descriptions (Continued: SDRAM)

Pin Name	Pin Type	Pin Description	Circuit Type	Pin Number	Share Pins
MDATA31 ~ MDATA24	I/O	64bit SDRAM Data		H1 J2 J4 H2 H3 G1 F1 G2	
MDATA23 ~ MDATA16	I/O	64bit SDRAM Data		G3 G4 F3 F4 D1 C1 D2 C2	
MDATA16 ~ MDATA8	I/O	64bit SDRAM Data		E4 D3 C3 D4 C4 B3 C5 D6	
MDATA7 ~ MDATA0	I/O	64bit SDRAM Data		A3 C6 B5 D7 A5 D8 C7 D9	

Table 1-1. S5H2000X Pin Descriptions (Continued: SDRAM)

Pin Name	Pin Type	Pin Description	Circuit Type	Pin Number	Share Pins
MADDR10 ~ MADDR0	O	11bit SDRAM Address		T3 T1 R4 R3 P4 P3 P2 N1 N2 N3 N4	
MDQM7 ~ MDQM0	O	8bit SDRAM Data MASK		AF2 AA4 AA1 T4 F2 B1 A4 C8	
MBA1	O	2bit SDRAM Bank Address		M1	
MBA0				M2	
MCLK	O	SDRAM Clock		M4	
MCKE	O	SDRAM Clock Enable		L1	
nMCS1	O	SDRAM Chip Select 1 (Active LOW)		K1	
nMCS0	O	SDRAM Chip Select 0 (Active LOW)		L2	
nMWE	O	SDRAM Write Enable (Active LOW)		K2	
nMRAS	O	SDRAM Row Address (Active LOW)		K4	
nMCAS	O	SDRAM Column Address (Active LOW)		K3	

Table 1-1. S5H2000X Pin Descriptions (Continued: External Video data input-SD)

Pin Name	Pin Type	Pin Description	Circuit Type	Pin Number	Share Pins
SIDATA7 ~ SIDATA0	I	8bit SD Video Data Input		D22 C23 D23 E23 C24 C25 D24 C26	
SICLK	I	SD Video Data Clock		B23	
SIHSYNC	I	SD Video H Sync		B24	
SIVSYNC	I	SD Video V Sync		A25	
SIFID	I	SD Video Field ID		B26	

Table 1-1. S5H2000X Pin Descriptions (Continued: External Video data input-HD)

Pin Name	Pin Type	Pin Description	Circuit Type	Pin Number	Share Pins
HIR7 ~ HIR0	I	HD Video R Data Input		K26 M23 M24 M25 M26 N23 N24 N25	
HIG7 ~ HIG0	I	HD Video G Data Input		H25 J25 H26 J26 K23 K24 K25 L23	

Table 1-1. S5H2000X Pin Descriptions (Continued: External Video data input-HD)

Pin Name	Pin Type	Pin Description	Circuit Type	Pin Number	Share Pins
HIB7 ~ HIB0	I	HD Video **B** Data Input		E26 H23 G24 G25 F26 G26 H24 J24	
HICLK	I	HD Video Data Clock		G23	
HIHSYNC	I	HD Video H Sync		F24	
HIVSYNC	I	HD Video V Sync		F25	

Table 1-1. S5H2000X Pin Descriptions (Continued: Video data output-analog SD)

Pin Name	Pin Type	Pin Description	Circuit Type	Pin Number	Share Pins
aCVBS	AO	SD Analog Composite Video Output		A20	
aY	AO	SD Analog Luminance Video Output		A17	
aC	AO	SD Analog Chroma Video Output		C19	
aSCOMP	AO	SD DAC Compensation		B19	
aSVREF	AO	SD DAC Voltage Reference		D18	
aSIRS	AO	SD DAC Current Reference		C17	

Table 1-1. S5H2000X Pin Descriptions (Continued: Video data output-analog HD)

Pin Name	Pin Type	Pin Description	Circuit Type	Pin Number	Share Pins
aRPR	AO	HD Analog Video R Output		A14	
aGY	AO	HD Analog Video G Output		B16	
aBPB	AO	HD Analog Video B Output		B14	
aHCOMP	AO	HD DAC Compensation		D14	
aHVREF	AO	HD DAC Voltage Reference		C14	
aHIRS	AO	HD DAC Current Reference		A16	

Table 1-1. S5H2000X Pin Descriptions (Continued: External Video data output-digital HD)

Pin Name	Pin Type	Pin Description	Circuit Type	Pin Number	Share Pins
HOR7 ~ HOR0	O	HD Video **R** Data Output		C20 D20 A22 B22 C21 A23 A24 D21	
HOG7 ~ HOG0	O	HD Video **G** Data Output		D12 A12 D13 C13 B13 D19 A21 B21	
HOB7 ~ HOB0	O	HD Video **B** Data Output		A8 C10 B9 D11 B10 C11 B11 A11	
HVIDCLK	I	HD Video Data Clock		C9	
HOVSYNC	O	HD Video H Sync Output		B8	
HOHSYNC	O	HD Video V Sync Output		D10	

Table 1-1. S5H2000X Pin Descriptions (Continued: Audio output)

Pin Name	Pin Type	Pin Description	Circuit Type	Pin Number	Share Pins
ILRCLK	I	Audio Left/Right Clock Input		T26	
IBCLK	I	Bit Clock Input		R23	
IPCM	I	PCM Data Input		T24	
OBCLK	O	Bit Clock Output		U25	
ODCLK	O	DAC Clock Output		U26	
OLRCLK	O	Left/Right indicate signal		T23	
OADATA	O	DATA Output for External audio DAC		V26	
OSPDIF	O	SPDIF Output		U24	

Table 1-1. S5H2000X Pin Descriptions (Continued: Power)

Pin Name	Pin Type	Pin Description	Circuit Type	Pin Number	Share Pins
PVDDOP		Digital PAD Power (3.3V)		A1 A7 A10 A13 A26 B2 B4 C22 E25 J23 L26 M3 P1 T2 T25 V2 W4 AA25 AC1 AC18 AC20 AD5 AD9 AD16 AE14 AF1 AF10 AF26	–
PVSSOP		Digital PAD Ground		A9 A18 B6 B20 B25 E3 H4 J1 J3 V1 AC7 AD12	–

Table 1-1. S5H2000X Pin Descriptions (Continued: Power)

Pin Name	Pin Type	Pin Description	Circuit Type	Pin Number	Share Pins
PVDDI	_	Digital Internal Power (1.8V)		AE2 AE25 AF13 AF24 B7 D5 D26 E1 L3 L24 R2 V23 W3 AD2 AD21 AD25 AE4 AE7 AF12 AF18	_
PVSSI	_	Digital Internal Ground		A2 A6 E2 F23 L4 L25 R1 W2 AA26 AC2 AD7 AD24 AE3 AE12 AE18 AE22	_

Table 1-1. S5H2000X Pin Descriptions (Continued: Power)

Pin Name	Pin Type	Pin Description	Circuit Type	Pin Number	Share Pins
PVSSI	–	Digital Internal Ground		A2 A6 E2 F23 L4 L25 R1 W2 AA26 AC2 AD7 AD24 AE3 AE12 AE18 AE22	–
PAVDDT	–	DAC PAD Power (3.3V)		B15 C15 C18 D17	–
PAVSST	–	DAC PAD Ground		A15 A19 B18 D15	–
PVDDI_DAC	–	DAC Internal Power (3.3V)		C16	–
PVSSI_DAC	–	DAC Internal Ground		D16	–
PAVBB_DAC	–	DAC Bulk Ground		B17	–
PAVDDT_PLL	–	PLL PAD Power (1.8V)		P23	–
PAVSST_PLL	–	PLL PAD Ground		R24	–
PAVBB_PLL	–	PLL Bulk Ground		R25	–
PVDDI_PLL	–	PLL Internal Power (1.8V)		N26	–
PVSSI_PLL	–	PLL Internal Ground		P26	–

NOTES

2 ADDRESS SPACE

OVERVIEW

Basically, S5H2000X communicates with external devices through PCI.

S5H2000X requests the required amount of memory (The amount should be previously indicated.) From the host through the base address registers, BAR0 and BAR1, of the PCI configuration registers. All the registers of the S5H2000X have addresses which are determined by offset from BAR0 and BAR1. The address space that the PCI host device allocates to S5H2000X BAR0 and BAR1 exists within the range of the PCI address space (32 bits – 4GB (Giga bytes).

For example, if the S3C2800X is the PCI host device, it detects S5H2000X during PCI scanning upon boot-up and recognizes the requested address space (memory or I/O size) via BAR0and BAR1. S3C2800X is designed to have a maximum PCI address space of 128MB (Mega bytes).

Hence, although the total PCI address space is 4GB because the PCI address bus is 32 bits, the S3C2800X can only use up to 128MB of address space. The S3C2800X has a built-in address conversion logic gate which picks up the desired starting address from the PCI address space of 4GB.

The following example describes in detail the addressing for a device constructed with S5H2000X and S3C2800X.

This device requests from the host 4-MB of memory via BAR0 and 32-MB of memory via BAR1 in accordance with the PCI us 2.1 specification. This request is known to the S3C2800X, which is the PCI host, during PCI scanning.

The PCI start address of the S3C2800X is designed to be 0x2000 0000. If the value of the PCIBATAPM_[31:27] register of the S3C2800X is set to 0100 0b and you read the momory location of 0x2000 0010 from the S3C2800X, the requested address is 0x4000 0010 on the PCI bus. That is, the address_[31:27] of 3C2800X is converted the value of PCIBATAPM_[31:27] and is output on the PCI bus. If 0x4000 0000 is written to-S5H2000X's BAR0, the address is mapped to S5H2000X's BAR0 + 0x000 0010 and the content in the mapped address is read.

ADDRESS SPACE

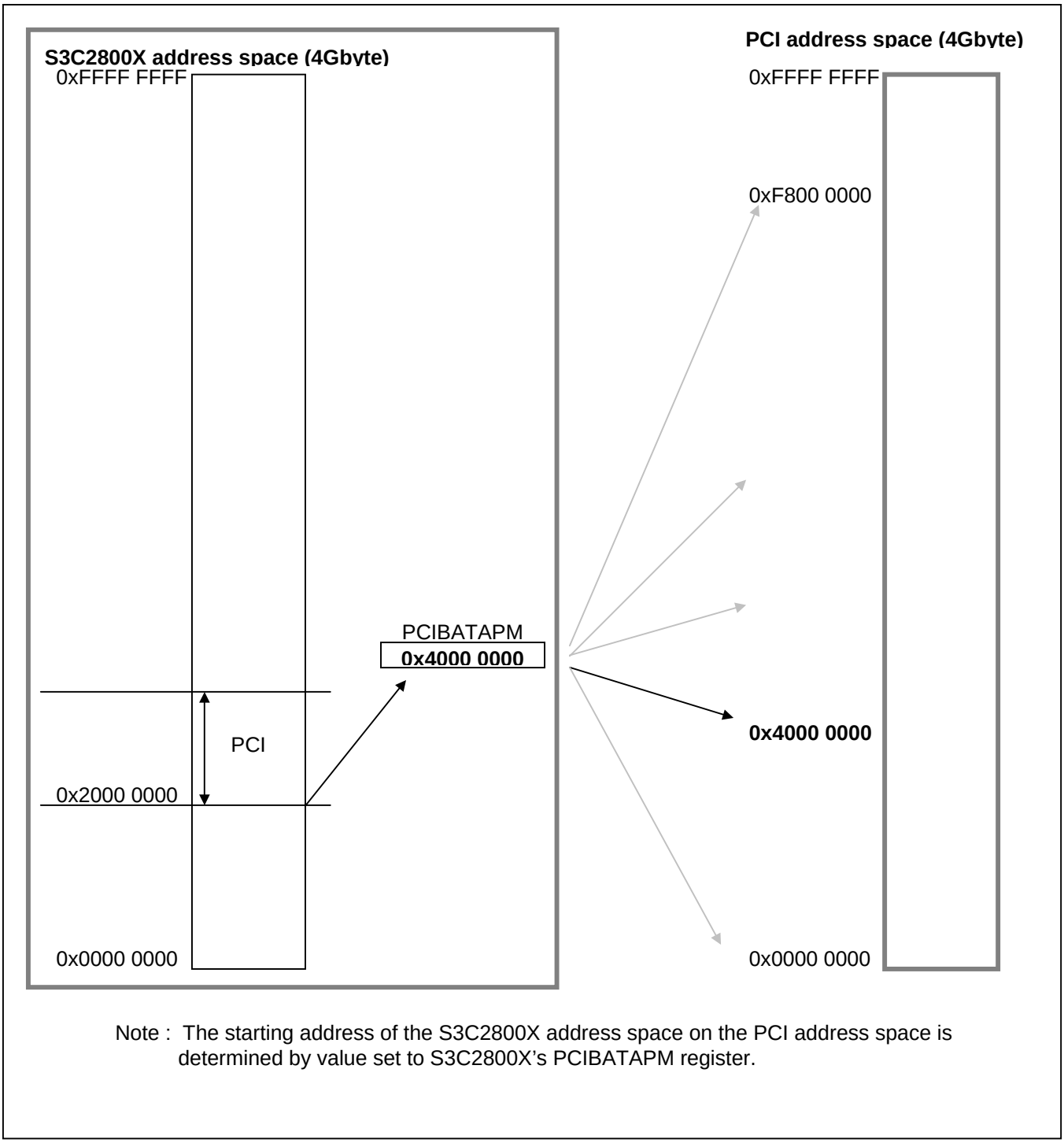

Figure 2-1 Host and S5H2000X address space

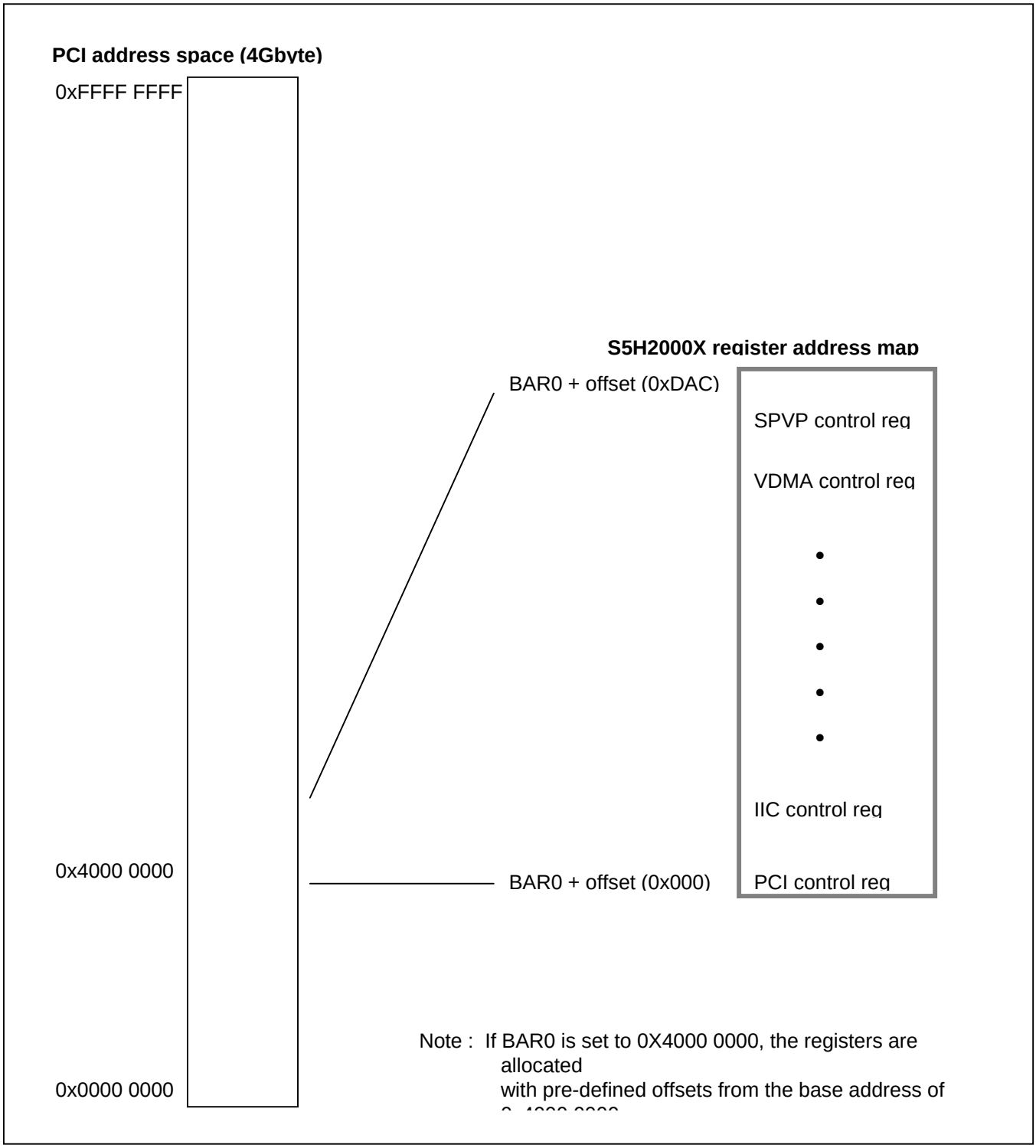

Figure 2-2 S5H2000X PCI memory address space

REGISTER MAP

Table 2-1. S5H2000X Register map (PCI control register)

Name	Address	Description	Type	Reset value
GSCR_AMMR	BAR0+00h	Arbitration Mode of Master	R/W	0
GSCR_IER	BAR0+04h	Interrupt Enable Register	R/W	0
GSCR_IPCR	BAR0+08h	Interrupt Pending & Clear Register	R/W	0
GSCR_MMSR	BAR0+0ch	Master Module Status Register	R	0
GSCR_SRN	BAR0+14h	Soft Reset_N	R/W	0

Table 2-1. S5H2000X Register map (continued: PCI W_TS_DPSRAM)

Name	Address	Description	Type	Reset value
LTCR1_PSA	BAR0+c0h	PCI Start Address	R/W	0
LTCR1_LSA	BAR0+c4h	Local Start Address	R/W	0
LTCR1_TBC	BAR0+c8h	Transfer Byte-Count	R/W	0
LTCR1_AxC	BAR0+cch	Auxiliary Control	R/W	0
LTCR1_XBC	BAR0+d0h	Transferred Byte-Count	R	0
LTCR1_ESR	BAR0+d4h	Error Status	R	0

Table 2-1. S5H2000X Register map (continued: PCI GP interface register)

Name	Address	Description	Type	Reset value
LGCR_PSA	BAR0+e0h	PCI Start Address	R	0
LGCR_DSR	BAR0+e4h	Data Size	R	0
LGCR_AxC	BAR0+e8h	Auxiliary Control	R/W	0
LGCR_TDS	BAR0+ech	Transferred Data Size	R	0
LGCR_ESR	BAR0+f0h	Error Status	R	0

Table 2-1. S5H2000X Register map (continued: PCI Audio DMA register)

Name	Address	Description	Type	Reset value
LDCR_PSA0	BAR0+100h	Audio DMA Control Register	R/W	0
LDCR_PSA1	BAR0+104h	Audio DMA Control Register	R/W	0
LDCR_TWC0	BAR0+108h	Audio DMA Control Register	R/W	0
LDCR_TWC1	BAR0+10ch	Audio DMA Control Register	R/W	0
LDCR_AxC	BAR0+110h	Audio DMA Control Register	R/W	0
LDCR_XWC0	BAR0+114h	Audio DMA Control Register	R	0
LDCR_XWC1	BAR0+118h	Audio DMA Control Register	R	0
LDCR_ESR	BAR0+11ch	Audio DMA Control Register	R	0
LACR_IO	BAR0+124h	Audio INOUT Setting Register	R/W	0
LACR_VAL	BAR0+128h	Audio IEC958 Control Register	R/W	0
LACR_STATUS	BAR0+12ch	Audio Channel Status Register	R	0

Table 2-1. S5H2000X Register map (continued: PCI HSMB register)

Name	Address	Description	Type	Reset value
LHCR_PSA	BAR0+140h	PCI Start Address	R/W	0
LHCR_LSA	BAR0+144h	Local Start Address	R/W	0
LHCR_TBC	BAR0+148h	Transfer Byte-Count	R/W	0
LHCR_AxC	BAR0+14ch	Auxiliary Control	R/W	0
LHCR_XBC	BAR0+150h	Transferred Byte-Count	R	0
LHCR_ESR	BAR0+154h	Error Status	R	0

Table 2-1. S5H2000X Register map (continued: PCI SP interface register)

Name	Address	Description	Type	Reset value
LVCR_PHA	BAR0+160h	PCI Head Address	R/W	0
LVCR_CQS	BAR0+164h	Circular Que Size	R/W	0
LVCR_AxC	BAR0+168h	Auxiliary Control	R/W	0
LVCR_WPA	BAR0+16ch	Write Point Address	R	0
LVCR_XBC	BAR0+170h	Transferred Byte-Count	R	0
LVCR_ESR	BAR0+174h	Error Status	R	0

Table 2-1. S5H2000X Register map (continued: PCI Header FIFO register)

Name	Address	Description	Type	Reset value
VFRM_REG0	BAR0+180h	Header Register_0	R	0
VFRM_REG1	BAR0+184h	Header Register_1	R	0
VFRM_REG2	BAR0+188h	Header Register_2	R	0
VFRM_REG3	BAR0+18ch	Header Register_3	R	0
VFRM_REG4	BAR0+190h	Header Register_4	R	0
VFRM_REG5	BAR0+194h	Header Register_5	R	0
VFRM_REG6	BAR0+198h	Header Register_6	R	0
VFRM_REG7	BAR0+19ch	Header Register_7	R	0
VFRM_REG8	BAR0+1a0h	Header Register_8	R	0
VFRM_REG9	BAR0+1a4h	Header Register_9	R	0
VFRM_REG10	BAR0+1a8h	Header Register_10	R	0
VFRM_REG11	BAR0+1ach	Header Register_11	R	0
VFRM_REG12	BAR0+1b0h	Header Register_12	R	0
VFRM_REG13	BAR0+1b4h	Header Register_13	R	0
VFRM_REG14	BAR0+1b8h	Header Register_14	R	0
VFRM_REG15	BAR0+1bch	Header Register_15	R	0

Table 2-1. S5H2000X Register map (continued: PCI Write Pointer for Header register)

Name	Address	Description	Type	Reset value
HDR_WPTR	BA R0+1c0h	Write Pointer for Header	R	0

Table 2-1. S5H2000X Register map (continued: PLL Mode register)

Name	Address	Description	Type	Reset value
RPLL_PLL135	BAR0+1e0h	135MHz PLL mode Register	R/W	0x4970
RPLL_PLL38P4	BAR0+1e4h	38.4MHz PLL mode Register	R/W	0x6ce0
RPLL_PLL24P5	BAR0+1e8h	24.576MHz PLL mode Register	R/W	0x5c61

Table 2-1. S5H2000X Register map (continued: Interrupt control register)

Name	Address	Description	Type	Reset value
INTR_QUE0	BAR0+240h	Interrupt Queue 0 Register	R/W	0
INTR_MASK0	BAR0+244h	Interrupt Mask 0 Register	R/W	0
INTR_ACK0	BAR0+248h	Interrupt Acknowledge 0 Register	R/W	0
INTR_QUE1	BAR0+24ch	Interrupt Queue 1 Register	R/W	0
INTR_MASK1	BAR0+250h	Interrupt Mask 1 Register	R/W	0
INTR_ACK1	BAR0+254h	Interrupt Acknowledge 1 Register	R/W	0
INTR_ARMI	BAR0+258h	ARM Interrupt Register	R/W	0
INTR_ARMA	BAR0+25ch	ARM Acknowledge Register	R/W	0
INTR_ARMPR	BAR0+260h	ARM Priority Register	R/W	0
INTR_ARMM	BAR0+264h	ARM Mask Register	R/W	0
INTR_ARMPD	BAR0+268h	ARM Pending Register	R/W	0

Table 2-1. S5H2000X Register map (continued: IIC control register)

Name	Address	Description	Type	Reset value
I2C_CTRL	BAR0+280h	I2C Control Register	R/W	0
I2C_ADDR	BAR0+284h	I2C Address Register	R/W	0
I2C_TXDAT	BAR0+288h	I2C Transmitted Data Register	R/W	0
I2C_RXDAT	BAR0+28ch	I2C Received Data Register	R	0
I2C_CLK	BAR0+290h	I2C Clock Register	R/W	0
I2C_STATUS	BAR0+294h	I2C Status Register	R	0

Table 2-1. S5H2000X Register map (continued: TS DMA1 control register)

Name	Address	Description	Type	Reset value
DMA1_SRC_ADDR	BAR0+400h	DMA1 source address Register	R/W	0
DMA1_TAR_ADDR	BAR0+404h	DMA1 target address Register	R/W	0
DMA1_CTRL	BAR0+408h	DMA1 Control Register	R/W	0

Table 2-1. S5H2000X Register map (continued: TS Buffer control register)

Name	Address	Description	Type	Reset value
BUFFER_VALID1	BAR0+420h	Buffer 1 Validity Register	R	0

Table 2-1. S5H2000X Register map (continued: PID control register)

Name	Address	Description	Type	Reset value
PID0	BAR0+480h	PID 0 Setting Register	R/W	0
PID1	BAR0+484h	PID 1 Setting Register	R/W	0
PID2	BAR0+488h	PID 2 Setting Register	R/W	0
PID3	BAR0+48ch	PID 3 Setting Register	R/W	0
PID4	BAR0+490h	PID 4 Setting Register	R/W	0
PID5	BAR0+494h	PID 5 Setting Register	R/W	0
PID6	BAR0+498h	PID 6 Setting Register	R/W	0
PID7	BAR0+49ch	PID 7 Setting Register	R/W	0
PID8	BAR0+4a0h	PID 8 Setting Register	R/W	0
PID9	BAR0+4a4h	PID 9 Setting Register	R/W	0
PID10	BAR0+4a8h	PID 10 Setting Register	R/W	0
PID11	BAR0+4ach	PID 11 Setting Register	R/W	0
PID12	BAR0+4b0h	PID 12 Setting Register	R/W	0
PID13	BAR0+4b4h	PID 13 Setting Register	R/W	0
PID14	BAR0+4b8h	PID 14 Setting Register	R/W	0
PID15	BAR0+4bch	PID 15 Setting Register	R/W	0
PID16	BAR0+4c0h	PID 16 Setting Register	R/W	0
PID17	BAR0+4c4h	PID 17 Setting Register	R/W	0
PID18	BAR0+4c8h	PID 18 Setting Register	R/W	0
PID19	BAR0+4cch	PID 19 Setting Register	R/W	0
PID20	BAR0+4d0h	PID 20 Setting Register	R/W	0
PID21	BAR0+4d4h	PID 21 Setting Register	R/W	0
PID22	BAR0+4d8h	PID 22 Setting Register	R/W	0
PID23	BAR0+4dch	PID 23 Setting Register	R/W	0
PID24	BAR0+4e0h	PID 24 Setting Register	R/W	0
PID25	BAR0+4e4h	PID 25 Setting Register	R/W	0
PID26	BAR0+4e8h	PID 26 Setting Register	R/W	0
PID27	BAR0+4ech	PID 27 Setting Register	R/W	0
PID28	BAR0+4f0h	PID 28 Setting Register	R/W	0
PID29	BAR0+4f4h	PID 29 Setting Register	R/W	0
PID30	BAR0+4f8h	PID 30 Setting Register	R/W	0
PID31	BAR0+4fch	PID 31 Setting Register	R/W	0

Table 2-1. S5H2000X Register map (continued: DES control register)

Name	Address	Description	Type	Reset value
SCRM_CTRL1	BAR0+580h	DES Control Register 1	R/W	0
ODD_HIGH1	BAR0+584h	DES1 ODD KEY MSB 32bit	R/W	0
ODD_LOW1	BAR0+588h	DES1 ODD KEY LSB 32bit	R/W	0
EVEN_HIGH1	BAR0+58ch	DES1 EVEN KEY MSB 32bit	R/W	0
EVEN_LOW1	BAR0+590h	DES1 EVEN KEY LSB 32bit	R/W	0
SCRM_CTRL2	BAR0+594h	DES Control Register 2	R/W	0
ODD_HIGH2	BAR0+598h	DES2 ODD KEY MSB 32bit	R/W	0
ODD_LOW1	BAR0+59ch	DES2 ODD KEY LSB 32bit	R/W	0
EVEN_HIGH2	BAR0+5a0h	DES2 EVEN KEY MSB 32bit	R/W	0
EVEN_LOW2	BAR0+5a4h	DES2 EVEN KEY LSB 32bit	R/W	0
SCRM_CTRL3	BAR0+5a8h	DES Control Register 3	R/W	0
ODD_HIGH3	BAR0+5ach	DES3 ODD KEY MSB 32bit	R/W	0
ODD_LOW3	BAR0+5b0h	DES3 ODD KEY LSB 32bit	R/W	0
EVEN_HIGH3	BAR0+5b4h	DES3 EVEN KEY MSB 32bit	R/W	0
EVEN_LOW3	BAR0+5b8h	DES3 EVEN KEY LSB 32bit	R/W	0
SCRM_CTRL4	BAR0+5bch	DES Control Register 4	R/W	0
ODD_HIGH4	BAR0+5c0h	DES4 ODD KEY MSB 32bit	R/W	0
ODD_LOW4	BAR0+5c4h	DES4 ODD KEY LSB 32bit	R/W	0
EVEN_HIGH4	BAR0+5c8h	DES4 EVEN KEY MSB 32bit	R/W	0
EVEN_LOW4	BAR0+5cch	DES4 EVEN KEY LSB 32bit	R/W	0
SCRM_CTRL5	BAR0+5d0h	DES Control Register 5	R/W	0
ODD_HIGH5	BAR0+5d4h	DES5 ODD KEY MSB 32bit	R/W	0
ODD_LOW5	BAR0+5d8h	DES5 ODD KEY LSB 32bit	R/W	0
EVEN_HIGH5	BAR0+5dch	DES5 EVEN KEY MSB 32bit	R/W	0
EVEN_LOW5	BAR0+5e0h	DES5 EVEN KEY LSB 32bit	R/W	0
SCRM_CTRL6	BAR0+5e4h	DES Control Register 6	R/W	0
ODD_HIGH6	BAR0+5e8h	DES6 ODD KEY MSB 32bit	R/W	0
ODD_LOW6	BAR0+5ech	DES6 ODD KEY LSB 32bit	R/W	0
EVEN_HIGH6	BAR0+5f0h	DES6 EVEN KEY MSB 32bit	R/W	0
EVEN_LOW6	BAR0+5f4h	DES6 EVEN KEY LSB 32bit	R/W	0

Table 2-1. S5H2000X Register map (continued: Clock Recovery register)

Name	Address	Description	Type	Reset value
PCR_CTRL1	BAR0+6c0h	System Clock Reference Counter	R/W	0
PCR_CTRL2	BAR0+6c4h	System Clock Reference Counter	R/W	0
PWM_CTRL	BAR0+6c8h	PWM Duty Control	R/W	0

Table 2-1. S5H2000X Register map (continued: TS Input Switch register)

Name	Address	Description	Type	Reset value
EXT_CTRL	BAR0+6e0h	TS Input Switch External Control	R/W	0

Table 2-1. S5H2000X Register map (continued: DP control register)

Name	Address	Description	Type	Reset value
DP_REG_0	BAR0+800h	sync on	R/W	0
DP_REG_1	BAR0+804h	source on / off	R/W	0
DP_REG_2	BAR0+808h	display mode	R/W	0
DP_REG_3	BAR0+80ch	display size	R/W	0
DP_REG_4	BAR0+810h	hd output h sync location / rate	R/W	0
DP_REG_5	BAR0+814h	hd output h active	R/W	0
DP_REG_6	BAR0+818h	hd output v active	R/W	0
DP_REG_7	BAR0+81ch	hd output 656 v active	R/W	0
DP_REG_8	BAR0+820h	SP vsync start 0/1	R/W	0
DP_REG_10	BAR0+828h	Main / Sub horizontal processing start	R/W	0x0101
DP_REG_11	BAR0+82ch	Main video enable horizontal	R/W	0
DP_REG_12	BAR0+830h	Main video enable vertical	R/W	0
DP_REG_13	BAR0+834h	Main2 /PIG / IPC sync	R/W	0
DP_REG_14	BAR0+838h	Sub video enable horizontal	R/W	0
DP_REG_15	BAR0+83ch	Sub video enable vertical 0	R/W	0
DP_REG_18	BAR0+848h	Display main video enable horizontal	R/W	0
DP_REG_19	BAR0+84ch	Display main video enable vertical	R/W	0
DP_REG_20	BAR0+850h	Display sub video enable horizontal	R/W	0
DP_REG_21	BAR0+854h	Display sub video enable vertical	R/W	0
DP_REG_22	BAR0+858h	HD sync	R/W	0
DP_REG_23	BAR0+85ch	SD sync	R/W	0
DP_REG_24	BAR0+860h	External SD sync	R/W	0x74

Table 2-1. S5H2000X Register map (continued: DP control register)

Name	Address	Description	Type	Reset value
DP_REG_25	BAR0+864h	External SD horizonal active	R/W	0
DP_REG_26	BAR0+868h	External SD vertical active	R/W	0
DP_REG_27	BAR0+86ch	External HD sync	R/W	0
DP_REG_28	BAR0+870h	External HD horizonal active	R/W	0
DP_REG_29	BAR0+874h	External HD vertical active	R/W	0
DP_REG_30	BAR0+878h	External Base Display Pointer	R/W	0
DP_REG_31	BAR0+87ch	1h size for External Display Pointer	R/W	0
DP_REG_32	BAR0+880h	Sub sample mode & mmu request length	R/W	0
DP_REG_33	BAR0+884h	Main Vertical filter coefficient Main Video data Vertical start location	R/W	0
DP_REG_34	BAR0+888h	Main Video data horizontal Start/End	R/W	0
DP_REG_35	BAR0+88ch	Main Video data horizontal size Main Horizontal Active Size	R/W	0
DP_REG_37	BAR0+894h	IPC threshold	R/W	0
DP_REG_38	BAR0+898h	Pano on & Left/Center region Size	R/W	0
DP_REG_39	BAR0+89ch	Main Horizontal Coefficient	R/W	0
DP_REG_40	BAR0+8a0h	Pano coefficient A & B	R/W	0
DP_REG_41	BAR0+8a4h	Polyphase filter coefficient	R/W	0x7ff0
DP_REG_42	BAR0+8a8h	Polyphase filter coefficient	R/W	0x66fffa50
DP_REG_43	BAR0+8ach	Polyphase filter coefficient	R/W	0x98764310
DP_REG_44	BAR0+8b0h	Polyphase filter coefficient	R/W	0x35790bba
DP_REG_45	BAR0+8b4h	Polyphase filter coefficient	R/W	0x12348100
DP_REG_46	BAR0+8b8h	Polyphase filter coefficient	R/W	0x2b688dd6
DP_REG_47	BAR0+8bch	Polyphase filter coefficient	R/W	0xffef3adb
DP_REG_48	BAR0+8c0h	Polyphase filter coefficient	R/W	0x078f9fc0
DP_REG_49	BAR0+8c4h	Polyphase filter coefficient	R/W	0x05ac9b3a
DP_REG_50	BAR0+8c8h	Polyphase filter coefficient	R/W	0x030751a8
DP_REG_51	BAR0+8cch	Polyphase filter coefficient	R/W	0x00820692
DP_REG_52	BAR0+8d0h	Polyphase filter coefficient	R/W	0xbba97530
DP_REG_53	BAR0+8d4h	Polyphase filter coefficient	R/W	0x1346789a
DP_REG_54	BAR0+8d8h	Polyphase filter coefficient	R/W	0x166bffa4
DP_REG_55	BAR0+8dch	Polyphase filter coefficient	R/W	0x1ffc
DP_REG_56	BAR0+8e0h	Main Write 1h size	R/W	0
DP_REG_57	BAR0+8e4h	Main Color matirx	R/W	0
DP_REG_58	BAR0+8e8h	Main Color matirx	R/W	0

Table 2-1. S5H2000X Register map (continued: DP control register)

Name	Address	Description	Type	Reset value
DP_REG_59	BAR0+8ech	Main boundary color	R/W	0
DP_REG_60	BAR0+8f0h	Sub mmu request size	R/W	0
DP_REG_61	BAR0+8f4h	Sub display & video data horizontal size	R/W	0
DP_REG_62	BAR0+8f8h	Sub horizontal filter coef	R/W	0
DP_REG_63	BAR0+8fch	Sub Color matrix	R/W	0
DP_REG_64	BAR0+900h	Sub Color matrix	R/W	0
DP_REG_65	BAR0+904h	Sub vertical filter coef / video data vertical start	R/W	0
DP_REG_66	BAR0+908h	Sub video data horizontal start & end	R/W	0
DP_REG_67	BAR0+90ch	Sub boundary color	R/W	0
DP_REG_68	BAR0+910h	Display background color	R/W	0
DP_REG_69	BAR0+914h	SD output mode	R/W	0
DP_REG_70	BAR0+918h	SD output filter ratio	R/W	0
DP_REG_71	BAR0+91ch	Digital Encoder Mode	R/W	0
DP_REG_72	BAR0+920h	Macrovision interface	R/W	0xd2bd73e
DP_REG_73	BAR0+924h	Macrovision interface	R/W	0x90db665b
DP_REG_74	BAR0+928h	Macrovision interface	R/W	0x000000ff
DP_REG_75	BAR0+92ch	Macrovision interface	R/W	0x020df6f0
DP_REG_76	BAR0+930h	Macrovision interface	R/W	0x0000f0cf
DP_REG_77	BAR0+934h	Macrovision interface	R/W	0x00000000
DP_REG_78	BAR0+938h	SD output Caption Control	R/W	0
DP_REG_79	BAR0+93ch	DAC Control	R/W	0
DP_REG_80	BAR0+940h	Interrupt event register	R/W	0
DP_REG_81	BAR0+944h	Interrupt mask register	R/W	0
DP_REG_82	BAR0+948h	SD interrupt input	R/W	0
DP_REG_83	BAR0+94ch	HD interrupt input	R/W	0
DP_REG_84	BAR0+950h	SD toggle count	R	0
DP_REG_85	BAR0+954h	HD progressive & 4line count at 81MHz	R	0
DP_REG_86	BAR0+958h	HD vertical & horizontal count	R	0
DP_REG_87	BAR0+95ch	HD output Analog sync control	R/W	0
DP_REG_88	BAR0+960h	HDout & SDout DAC Connection status	R	0
DP_REG_89	BAR0+964h	SD horizontal start & end	R/W	0
DP_REG_90	BAR0+968h	HD/SD select	R/W	0
DP_REG_91	BAR0+96ch	Polyphase filter sign	R/W	0
DP_REG_92	BAR0+970h	Polyphase filter sign	R/W	0

Table 2-1. S5H2000X Register map (continued: DP control register)

Name	Address	Description	Type	Reset value
DP_REG_93	BAR0+974h	Polyphase filter sign	R/W	0
DP_REG_94	BAR0+978h	Polyphase filter sign	R/W	0
DP_REG_95	BAR0+97ch	SD output vertical position	R/W	0
DP_REG_96	BAR0+980h	SD output vertical position	R/W	0
DP_REG_93	BAR0+974h	Polyphase filter sign	R/W	0
DP_REG_94	BAR0+978h	Polyphase filter sign	R/W	0
DP_REG_95	BAR0+97ch	SD output vertical position	R/W	0

Table 2-1. S5H2000X Register map (continued: GP control register)

Name	Address	Description	Type	Reset value
WHPR_0	BAR0+a00h	Horizontal position register for window 0	R/W	0
WHPR_1	BAR0+a04h	Horizontal position register for window 1	R/W	0
WHPR_2	BAR0+a08h	Horizontal position register for window 2	R/W	0
WHPR_3	BAR0+a0ch	Horizontal position register for window 3	R/W	0
WVPR_0	BAR0+a20h	Vertical position register for window 0	R/W	0
WVPR_1	BAR0+a24h	Vertical position register for window 1	R/W	0
WVPR_2	BAR0+a28h	Vertical position register for window 2	R/W	0
WVPR_3	BAR0+a2ch	Vertical position register for window 3	R/W	0
WMR_0	BAR0+a40h	Mode register for window 0	R/W	0
WMR_1	BAR0+a44h	Mode register for window 1	R/W	0
WMR_2	BAR0+a48h	Mode register for window 2	R/W	0
WMR_3	BAR0+a4ch	Mode register for window 3	R/W	0
WAR_0	BAR0+a60h	Base address register for window 0	R/W	0
WAR_1	BAR0+a64h	Base address register for window 1	R/W	0
WAR_2	BAR0+a68h	Base address register for window 2	R/W	0
WAR_3	BAR0+a6ch	Base address register for window 3	R/W	0
BCR	BAR0+a80h	Background color/blink control register	R/W	0
VER	BAR0+a84h	Video effect register	R/W	0
PAR	BAR0+a8ch	Pixel α value register	R/W	0
CHPR	BAR0+aa4h	Horizontal cursor position register	R/W	0
CVPR	BAR0+aa8h	Vertical cursor position register	R/W	0
CASR	BAR0+aach	Cursor address & size register	R/W	0
CCR_0	BAR0+ab0h	Cursor color register for index 0	R/W	0
CCR_1	BAR0+ab4h	Cursor color register for index 1	R/W	0
CCR_2	BAR0+ab8h	Cursor color register for index 2	R/W	0

Table 2-1. S5H2000X Register map (continued: GP control register)

Name	Address	Description	Type	Reset value
CCR_3	BAR0+abch	Cursor color register for index 3	R/W	0
CCR_4	BAR0+ac0h	Cursor color register for index 4	R/W	0
CCR_5	BAR0+ac4h	Cursor color register for index 5	R/W	0
CCR_6	BAR0+ac8h	Cursor color register for index 6	R/W	0
CCR_7	BAR0+acch	Cursor color register for index 7	R/W	0

Table 2-1. S5H2000X Register map (continued: GA control register)

Name	Address	Description	Type	Reset value
GA_SIZE	BAR0+b04h	BLT hor./ver. pixel size register	R/W	0
GA_CS1_0	BAR0+b10h	Source1 BLT mode register in cpu memory	R/W	0
GA_CS1_1	BAR0+b14h	Source1 BLT start address in cpu memory	R/W	0
GA_DST_0	BAR0+b30h	Destination BLT mode register in local memory	R/W	0
GA_DST_1	BAR0+b34h	Destination window base address in local memory	R/W	0
GA_DST_2	BAR0+b38h	Destination BLT start point in local memory	R/W	0
GA_START	BAR0+ba8h	BLT start register	R/W	0
GA_RST	BAR0+bach	GA reset register	R/W	0
GA_STAT	BAR0+bb0h	GA status register	R/W	0

Table 2-1. S5H2000X Register map (continued: MMU control register)

Name	Address	Description	Type	Reset value
BASE_ADDR_0	BAR0+c00h	Base address register 0, 1 for MPEG memory 0: MPEG/T/Y/I, 1: MPEG/T/Y/P	R/W	0x000 0x088
BASE_ADDR_1	BAR0+c04h	Base address register 2, 3 for MPEG memory 2: MPEG/T/Y/B0, 3: MPEG/T/Y/B1	R/W	0x110 0x198
BASE_ADDR_4	BAR0+c10h	Base address register 8, 9 for MPEG memory 8: MPEG/T/C/I, 9: MPEG/T/C/P	R/W	0x440 0x484
BASE_ADDR_5	BAR0+c14h	Base address register 10, 11 for MPEG memory 10: MPEG/T/C/B0, 11: MPEG/T/C/B1	R/W	0x4C8 0x50C
BASE_ADDR_8	BAR0+c20h	Base address register 16, 17 for MPEG memory 16: MPEG/B/Y/I, 17: MPEG/B/Y/P	R/W	0x220 0x2A8
BASE_ADDR_9	BAR0+c24h	Base address register 18, 19 for MPEG memory 18: MPEG/B/Y/B0, 19: MPEG/B/Y/B1	R/W	0x330 0x3B8
BASE_ADDR_12	BAR0+c30h	Base address register 24, 25 for MPEG memory 24: MPEG/B/C/I, 25: MPEG/B/C/P	R/W	0x550 0x594

Table 2-1. S5H2000X Register map (continued: MMU control register)

Name	Address	Description	Type	Reset value
BASE_ADDR_13	BAR0+c34h	Base address register 26, 27 for MPEG memory 26: MPEG/B/C/B0, 27: MPEG/B/C/B1	R/W	0x5d8 0x61C
BASE_ADDR_32	BAR0+c80h	Base address register 64, 65 for DP memory 64: 0x000, 65: external memory 1	R/W	0
BASE_ADDR_33	BAR0+c84h	Base address register 66, 67 for DP memory 66: external memory 2, 67: external memory 3	R/W	0
BASE_ADDR_34	BAR0+c88h	Base address register 68, 69 for DP memory 68: external memory 4, 69: external memory 5	R/W	0
BASE_ADDR_35	BAR0+c8ch	Base address register 70, 71 for DP memory 70: external memory 6, 71: external memory 7	R/W	0
BASE_ADDR_36	BAR0+c90h	Base address register 72, 73 for DP memory 72: external memory 8, 73: external memory 9	R/W	0
BASE_ADDR_37	BAR0+c94h	Base address register 66, 67 for DP memory 74: external memory 10, 75: external memory 11	R/W	0
REFRESH_COUNT	BAR0+c98h	Refresh Counter	R/W	0x3FF
MMU_CONF	BAR0+c9ch	MMU Configuration Register	R/W	0x18040
REF_CYCLE	BAR0+ca0h	Refresh Cycle Register	R/W	0xA
HALT_LIMIT	BAR0+ca4h	Halt Limit Register	R/W	0x64
MMU_ERR_INFO	BAR0+ca8h	MMU Error Status Information Register	R	0

Table 2-1. S5H2000X Register map (continued: VDMA control register)

Name	Address	Description	Type	Reset value
CVDBUF_ST	BAR0+d00h	CVD Buffer Start Address	R/W	0
CVDBUF_SZ	BAR0+d04h	CVD Buffer Size	R/W	0
CVD_STATUS	BAR0+d08h	CVD Status Register	R/W	0
CVD_WRPTR	BAR0+d0ch	CVD Buffer Write Pointer	R/W	0
CVD_RDPTR	BAR0+d10h	CVD Buffer Read Pointer	R	0

Table 2-1. S5H2000X Register map (continued: SPVP control register)

Name	Address	Description	Type	Reset value
SP_CTRL0	BAR0+d80h	SP Control Register 0	R/W	0
SP_CTRL1	BAR0+d90h	SP Control Register 1	R/W	0
SP_STATUS	BAR0+d94h	SP Status Register	R/W	0
SP_DECM	BAR0+da4h	Decimation Register	R/W	0
VP_STATUS	BAR0+da8h	VP Status Register	R	0
VP_TIMER	BAR0+dach	VP Timer Register	R/W	0

Note: Reset value (DP_REG_41 ~ DP_REG55) for DP control register may vary with modes.

NOTE

3 TS DEMUX

OVERVIEW

Transport Stream (henceforth, TS) demux has software demux architecture which is executed by a 128-MIPS ARM7TDMI RISC core. Hence, analysis and processing of MPEG 2 or DSS TS video and audio and PSI packet headers such as PAT, PMT, SDT, and EIT are programmable and provide a wide range of applications.

There is only one TS demux input by default. If you need multiple input sources, you should place mux outside the chip.

The major features of TS are:

- S/W demux architecture using ARM7TDMI
- MPEG-2 or DSS TS demux support
- DVB, ATSC support
- Built-in DES descrambler
- Up to 9 demux modes supported (provided by S/W)
- Up to 32 PIDs can be received at the same time.
- CRC (MPEG-2: 32bit, DSS: 16bit) support
- Video packets are transferred to external SDRAM via DMA1.
- Audio packets are transferred to the memory of the host CPU via a PCI interface.
- Allows extraction of desired information from the PSI packet and transmition to the host CPU.
- Built-in clock recovery circuit for programmable clock recovery

Architecture

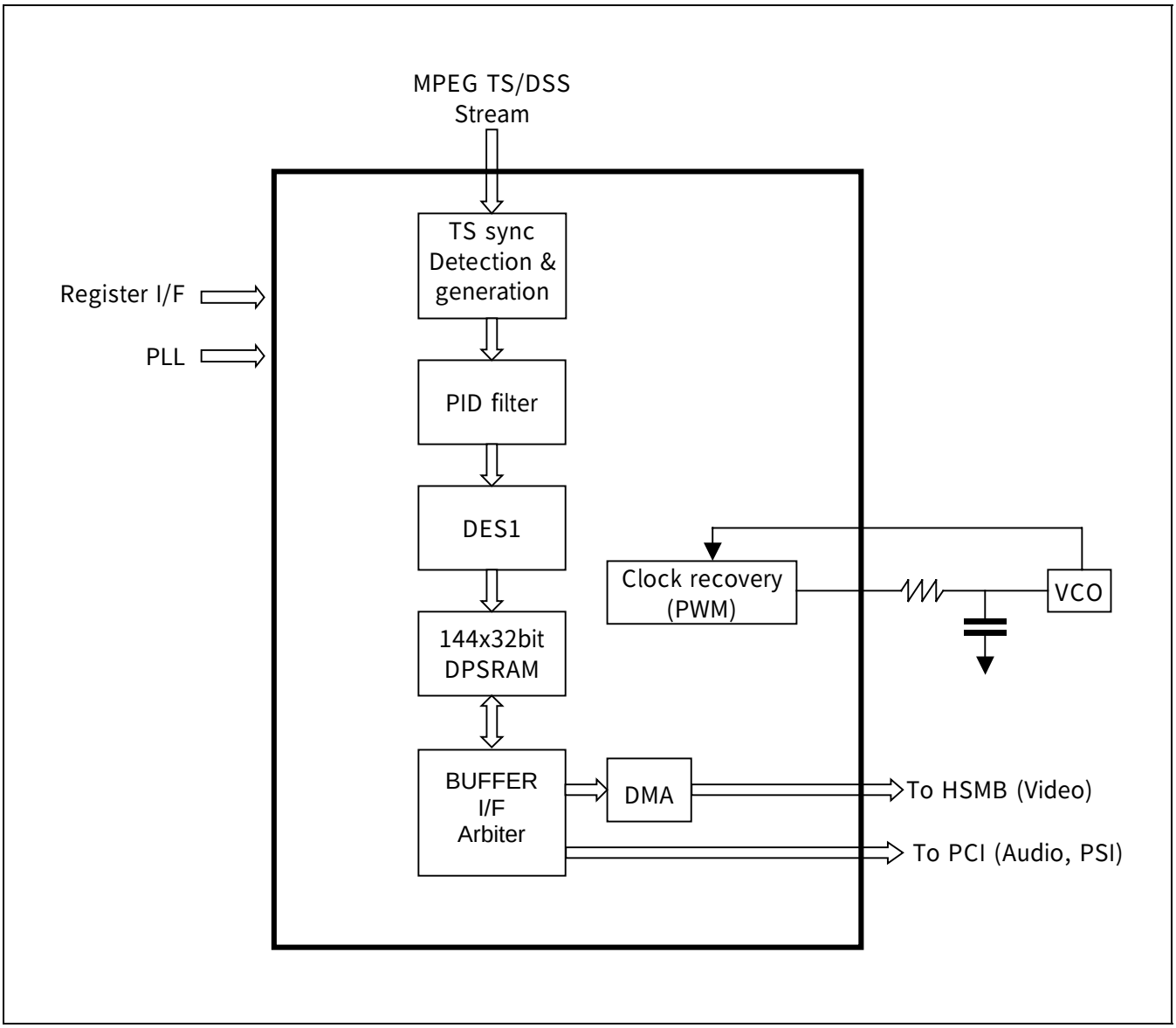

Figure 3-1 TS Demux block diagram

S/W demux

The TS demux block filters and classifies only the necessary data from the TS (transport stream) and transfers it to the specified location.

S5H2000X TS demux allows you to control this filtering, classification and transfer programmatically (using software). This feature provides great flexibility.

For example, an MPEG TS packet is composed of 188 bytes and each packet has its own PID. The TS demux of the S5H2000X which receives those TS packets has 32 PID filters. By setting the desired PID to these filters, you can select only those packets needed. The same principle is also applied to the DSS.

Those filtered TS packets pass through the DES and are buffered at DPSRAM, and then the desired data is filtered by the specified conditions and then transferred to the S5H2000X's external memory or the PCI.

The conditions to apply for filtering TS packets on DPSRAM can be specified programmatically. The filtering conditions depend entirely on the programmer himself. The demo program provides a demux algorithm you can use, but you can develop and apply completely different or more efficient algorithms.

H/W REGISTERS

The H/W registers used to construct TS demux are:
TS sync detection, PID filtering, DES, DMA, clock recovery, arbiter control, and data registers. These compose all the hardware registers. How to take advantage of them depends on the programmer himself.

DMA1 FOR VIDEO DATA TRANSPORT

When a valid DPSRAM buffer is filled with a packet (188 bytes for MPEG; 130 bytes for DSS) the corresponding bit of the B_VALID[2:0] of BUFFER_VALID register is set to 1. ARM7 poll this bit continually. When it detects that the bit has changed to 1, it begins transmitting the packet data. When DMA1 finishes transmitting the packet data, an interrupt is invoked and ARM7 clears the bit by writing 1 to the corresponding B_VALID[n] bit during the interrupt service routine.

Since this product is designed to process audio decoding on external processors, APM7 moves only video data to the external memory via DMA1. Audio and PSI data are transferred to the memory of the external processors via PCI.

DMA1_SRC_ADDR register

Name	Address	Description	Type	Reset value
DMA1_SRC_ADDR	BAR0 +0x400	Source address of DMA1	R/W	0

Bits	Name	Description	Reset value
[9:0]	SOURCE_ADDR	Address of the data to be transferred via DMA1. It is an address on the DPSRAM.	0
[31:10]	–	Not used	–

DMA1_TAR_ADDR register

Name	Address	Description	Type	Reset value
DMA1_ TAR_ADDR	BAR0 +0x404	Target address of DMA1	R/W	0

Bits	Name	Description	Reset value
[23:0]	SOURCE_ADDR	Address of the location to which the data is transferred via DMA1. It is an address on the external memory.	0
[31:24]	–	Not used	–

DMA1_CTRL register

Name	Address	Description	Type	Reset value
DMA1_ CTRL	BAR0 +0x408	Sets the size of the data to transmit and activates DMA1.	R/W	0

Bits	Name	Description	Reset value
[0]	DMA1_TEN	Write "1": Starts the data transfer via DMA1. When the transfer is complete, it resets to "0" automatically.	0
[1]	–	Not used	–
[9:2]	TRANS_SIZE	The size of the data to transmit (unit: byte)	0
[31:10]	–	Not used	–

*Note: Both the data size and the start bit can be set at the same time.

DPSRAM BUFFER VALID REGISTER

The TS packets that pass through the PID filtering and DES are buffered at the DPSRAM buffer one by one. At this time, the BUFFER_VALID register indicates whether the packets can be buffered or not.

The size of a buffer is 192 bytes. For MPEG TS, when 188 bytes are buffered the B_VALID[n] bit is set to "1" and the packet data is buffered by the next buffer. For DSS, the packet data is buffered at the next buffer when 130 bytes have been filled. The 3 buffers repeat, buffering in turn.

ARM7 polls the value of this register continually. When the value is not "0" it begins service, that is, it transfers the packet data to the specified place and clears the B_VALID[n] bit.

BUFFER_VALID register

Name	Address	Description	Type	Reset value
BUFFER_VALID	BAR0 +0x420	Indicates the validity of the DPSRAM buffer.	R/W	0

Bits	Name	Description	Reset value
[0]	B_VALID0	0 = valid, buffering is enabled 1 = invalid, buffering is disabled.	0
[1]	B_VALID1	0 = valid, buffering is enabled 1 = invalid, buffering is disabled.	0
[2]	B_VALID2	0 = valid, buffering is enabled 1 = invalid, buffering is disabled.	0
[31:3]	–	Not used	–

PID REGISTER FOR PACKET FILTERING

This register is used to filter only the necessary TS packets and then decode them.

When the desired PID values are set in the PID registers, only the packets that have that particular PID value will pass.

There are 32 PID registers, PID1 to PID32.

If the bit[16] of PID1 register is set to 1, all packets will be passed regardless of the PID values.

PID1 register

Name	Address	Description	Type	Reset value
PID1	BAR0 +0x480	PID filter의 PID register	R/W	0

Bits	Name	Description	Reset value
[12:0]	PID	Sets the PID or SCID for the TS packets to filter. For SCID, bit[12] is ignored because it is 12 bits.	0
[14:13]	–	Not used	–
[15]	EN	0 = Filtering disable 1 = Filtering enable	0
[16]	P_BYPASS	0 = Performs packet filtering. 1 = Bypasses packets without filtering. This flag is valid only if the EN flag is set to "1".	0
[31:17]	–	Not used	–

PID2~PID32 register

Name	Address	Description	Type	Reset value
PID2 ~ PID32	BAR0 +0x480 + 4*(n-1)	PID register for PID filtering	R/W	0

NOTE: n = 2 ~ 32

Bits	Name	Description	Reset value
[12:0]	PID	Sets the PID or SCID for the TS packets to filter. For SCID, bit[12] is ignored because it is of 12 bits.	0
[14:13]	–	Not used	–
[15]	EN	0 = Filtering disable 1 = Filtering enable	0
[31:16]	–	Not used	–

DES CONTROL REGISTER

This register controls the DES. It sets the necessary conditions and controls whether to execute de-scrambling.

There are 6 registers that have controls and keys. This means that when 32 packets are passed through the PID filtering, they can be de-scrambled with 6 different kinds of scramble data.

Generally, DES control is implemented according to the complexity of encryption so that it works in a specific DES algorithm mode. There are three DES algorithm modes (ECB: Electronic CodeBook, CBC: Cipher Block Chaining, CFB: Cipher FeedBack). This product is configured to work in ECB algorithm mode.

SCRM_CTRL1 ~ SCRM_CTRL6 register

Name	Address	Description	Type	Reset value
SCRM_CTRL1 ~ 6	BAR0 +0x580 +20*(n-1)	PID filter의 PID register	R/W	0

NOTE: n = 1 ~ 6

Bits	Name	Description	Reset value
[0]	KEY	Don't care	0
[1]	SCRM	Should be always set to "0".	0
[2]	EN	0 = De-scramble disable 1 = De-scramble enable	0
[7:3]	QUEUE_NUM	Indicates which of the 32 PID filters to be de-scrambled. For example, "0" indicates PID1 and "31"indicates PID32.	0
[31:8]	–	Not used	–

ODD_HIGH1 ~ ODD_HIGH6 register

Name	Address	Description	Type	Reset value
ODD_HIGH1 ~ ODD_HIGH6	BAR0 +0x584 +20*(n-1)	High 32 bits of the DES odd key	R/W	0

NOTE: n = 1 ~ 6

Bits	Name	Description	Reset value
[31:0]	ODD_KEY_HIGH	High 4 bytes [55:24] of the DES odd key	0

ODD_LOW1 ~ ODD_LOW6 register

Name	Address	Description	Type	Reset value
ODD_LOW1 ~ ODD_LOW6	BAR0 +0x588 +20*(n-1)	Low 32 bits of the DES odd key	R/W	0

NOTE: n = 1 ~ 6

Bits	Name	Description	Reset value
[23:0]	ODD_KEY_LOW	Low 4 bytes [23:0] of the DES odd key	0
[31:24]	–	Not used	–

EVEN_HIGH1 ~ EVEN _HIGH6 register

Name	Address	Description	Type	Reset value
EVEN_HIGH1 ~ EVEN _HIGH6	BAR0 +0x58C +20*(n-1)	High 32 bits of the DES even key	R/W	0

NOTE: n = 1 ~ 6

Bits	Name	Description	Reset value
[31:0]	EVEN _KEY_HIGH	High 4 bytes [55:24] of the DES even key	0

EVEN _LOW1 ~ EVEN _LOW6 register

Name	Address	Description	Type	Reset value
ODD_LOW1 ~ ODD_LOW6	BAR0 +0x590 +20*(n-1)	Low 32 bits of the DES odd key	R/W	0

NOTE: n = 1 ~ 6

Bits	Name	Description	Reset value
[23:0]	EVEN _KEY_LOW	Low 4 bytes [23:0] of the DES even key	0
[31:24]	–	Not used	–

PCR CONTROL REGISTERS

The Encoder transfers PCR data to the packets or PSI packets that have an adaptation field with which to synchronize them. PCR control registers are used to compare that data with the S5H2000X's SCR registers (in this case the S5H2000X is the decoder).

When PCR data is received for the first time, the H/W writes the data to S5H2000X's SCR registers. SCR is counted with the frequency of 27Mhz. An SCR counter consists of 42 bits. When the low 9-bit counter reaches 300, the high 33-bit counter increases by 1.

PCR_CTRL1 register

Name	Address	Description	Type	Reset value
PCR_CTRL1	BAR0+0x6C0	The System Clock reference counter value	R/W	0

Bits	Name	Description	Reset value
[31:0]	PCR_BASE	For MPEG2, the TS PCR base[31:0] value For DSS, the SCR[31:10] value	0

PCR_CTRL2 register

Name	Address	Description	Type	Reset value
PCR_CTRL2	BAR0+0x6C4	The System Clock reference counter value	R/W	0

Bits	Name	Description	Reset value
[8:0]	PCR_EXT	For MPEG2, the TS PCR extension[8:0] value For DSS, theSCR[8:0] value	0
[9]	CLK_MODE	0 = Operates in the PCR mode of MPEG2 TS 1 = Operates in the SCR mode of DSS	0
[14:10]	–	Not used	–
[15]	PCR_BASE	For MPEG2, the TS PCR base[32] value For DSS, the SCR[9] value	
[31:16]	–	Not used	–

PWM CONTROL REGISTER

This register controls the PWM to compensate for the difference between the PCR value and the counter value using a VCO.

If the PCR value is less than the counter value, then the decoder chip counter (S5H2000X) should be operated slowly.

The PWM_CTRL value should be set to a value more than 0x80 in order to operate the VCO slowly. Then, the counter will operate slowly and the counter value will approach the PCR value. If the PCR value is more than the counter value, then the decoder chip counter should be operated fast. The PWM_CTRL value should be set to a value less than 0x80 so that the VCO operates fast.

PWM_CTRL register

Name	Address	Description	Type	Reset value
PWM_CTRL	BAR0+ 0x6C8	PWM pulse duty	R/W	0x80

Bits	Name	Description	Reset value
[7:0]	PWM_VALUE	Adjustment value for the PWM output duty When set to 0x80, duty is 50%.	0x80
[31:8]	–	Not used	–

EXTERNAL INTERFACE CONTROL REGISTER

This register controls the TS sync detection block.

It sets the conditions for sync detection and sync missing. It also specifies the type of external stream to accept, and enables/disables the sync detection.

EXT_IF_CTRL register

Name	Address	Description	Type	Reset value
EXT_IF_CTRL	BAR0+ 0x6E0	Controls the TS sync detection block operation.	R/W	0

Bits	Name	Description	Reset value
[1:0]	SYNC_LOSS	Sync is determined to be lost when the sync byte is lost the specified number of times consecutively. Valid only in TS input mode.	0
[4:2]	SYNC_LOCK	Sync is accepted when the sync byte occurs the specified number of times consecutively. Valid only in TS input mode.	0
[5]	DSSorTS	0 = TS input mode 1 = DSS input mode	0
[6]	RESET_SYNC	0 = Normal 1 = TS sync detection block reset Reverts to "0" after reset.	0
[7]	EN	0 = Sync detection block disable 1 = Sync detection block enable	0
[31:8]	–	Not used	–

EXTERNAL INTERFACE STATUS REGISTER

This register indicates the status of the TS sync detection block.

It indicates whether a sync is detected or not, that is, a sync that matches the conditions which are set on the SYNC_LOCK bits of the EXT_IF_CTRL register.

EXT_IF_CTRL register

Name	Address	Description	Type	Reset value
EXT_IF_STS	BAR0+6e0h	TS Input Switch Status	R	0

Bits	Name	Description	Reset value
[0]	SYNC_LOCKED	0 = Sync unlocked 1 = Sync locked	0
[31:1]	–	Not used	–

S/W REGISTERS

The S/W registers used to construct the TS demux are:
TS demux control, Queue, PCR, command, PTS, and data filtering registers.

These registers are developed and provided by Samsung developers. Users can use them as they are or develop and apply new algorithms if needed.

PACKET CONTROL REGISTER

The BUFFER_VALID register is continually polled. When the value is not "0", the service begins. The PCR register contains the content to serve.

The H/W writes the PID filtering value, instead of the PID value, to the header of the packet that passes through the PID filter. For example, if a packet passes through PID filtering which has a PID value matching the value of the PID15 filter, its original PID value (which has been transferred from the broadcasting station) is cleared and changed to "15" which is the value of the PID filter it is currently passing. ARM7 can recognize that the packet has passed through the PID15 filter by reading the PID value set on the packet header and service will begin according to the content contained in the PCONTROL15 register.

PCONTROL1 ~ PCONTROL32 registers

Name	Address	Description	Type	Reset value
PCONTROL1~ PCONTROL32	S_REG_BASE + 4*(n-1)	These registers contain information, such as the demux mode, target area, etc, necessary for de-multiplexing the TS packet.	R/W	0

*n : 1~32

Bits	Name	Description	Reset value
[3:0]	DEMUX_M	Sets in what format to demux the TS packet.	0
[4]	PTS_ON	Indicates whether or not to perform A/V synchronization using the PTS information contained in the packet which has the current queue PID. When set to "1", synchronization is performed.	0
[8:5]	NUM_FILTER	Number of section filters. The maximum value is 8. That is, up to 8 section filters can be applied to a PID. When set to "0", section filtering is not used.	0
[14:9]	S_FILTER	The Start Number of the section filter to apply to the packet that will be saved to the queue. The Start Number should be the number of a filter in the section filter bank. The maximum value is 32.	0
[23:15]	Q_SIZE	Queue size. Queue_size = Q_size(9bit) X 4096 bytes. Maximum: 2048 K bytes = 16 M bits	0
[27:24]	TARGET	Location of the queue 0: Video buffer on external memory. 1: Section data buffer 2~13: Reserved 14: Section data buffer on PCI memory	
[28]	Reserved	Reserved	
[29]	PCR_EN	Indicates whether to extract PCR info from the packet that has the PID set to the current queue number. When set to "1", an extraction is performed.	

[30]	LOAD_PCR	Indicates whether to initialize the STC counter by extracting PCR info from the packet that has the PID set to the current queue number. When set to "1", an initialization is performed.	

The following S/W demux modes are provided by developers.

Mode	Value	Description
MPEG2_TP	0x0	The 188-byte MPEG 2 transport packet is output as is.
MPEG2_PES	0x1	Only the PES (Packetized Elementary Stream) is output from the MPEG 2 TP.
MPEG2_PES_payload	0x2	Only the elementary stream is output from the MPEG 2 TP.
MPEG2_section	0x3	Only section data is output from the MPEG 2 TP. A CRC (32-bit) check can be applied optionally. Section filtering can be applied to the output of desired sections only.
MPEG2_adaptation	0x4	Only the adaptation field is output from the MPEG 2 TP.
DSS_TP	0x8	The 130-byte DSS transport packet is output as is.
DSS_PES	0x9	The Prefix (2 bytes), CC (Continuity Count), and HD (Header Designator) are removed from the DSS transport packet, and the result is output. For example, the PES is output for DirectTV-HD when the elementary stream is output.
DSS_PES_payload	0xA	Used when the MPEG 2 PES packet is carried on payload (the transport block) of the DSS transport packet (DirectTV-HD). The elementary stream is output.
DSS_CAP	0xB	Used to process DSS CAP (Conditional Access Packet). The Prefix (2 bytes) is removed and the result is output.
DSS_section	0xC	Only section data is output from the DSS TP. A CRC (16-bit) check can be applied optionally. Section filtering can be applied to the output of the desired sections only.
MPEG2_TP	0x0	The 188-byte MPEG 2 transport packet is output as is.

Q ADDRESS REGISTERS

For video, DPSRAM data is saved to the external SDRAM and then decoded. For audio, it is saved to the host CPU's SDRAM via the PCI and then decoded. The Q address registers indicate those saving addresses.

QSTART_ADDR: Start address of the de-multiplexed data (That is, the start address of an image block).

QHDR_ADDR: Start address of the queue to write the data to.

QEND_ADDR: Used only for section filters. Indicates the end of the section data.

QSTART_ADDR1 ~ QSTART_ADDR32 registers

Name	Address	Description	Type	Reset value
QSTART_ADDR1~ QSTART_ADDR32	S_REG_BASE +0xC0+4*(n-1)	Start address of the queue in which the de-multiplexed TS data will be saved.	R/W	0

*n : 1~32

Bits	Name	Description	Reset value
[31:0]	Q_START_ADDR	Start address of the queue. If the target area is the PCI, it should be a 32-bit value. If the target area is the external SDRAM, it should be a 24-bit value.	0

QHDR_ADDR1 ~ QHDR_ADDR32 registers

Name	Address	Description	Type	Reset value
QHDR_ADDR1~ QHDR_ADDR32	S_REG_BASE +0x180+4*(n-1)	Header pointer to the current queue	R	0

*n : 1~32

Bits	Name	Description	Reset value
[31:0]	Q_HDR_ADDR	Write address of the queue. QSTART_ADDR indicates the start address.	0

QEND_ADDR1 ~ QEND_ADDR32 registers

Name	Address	Description	Type	Reset value
QEND_ADDR1~ QEND_ADDR32	S_REG_BASE +0x180+4*(n-1)	The Queue end pointer of a section. Valid only if the data is section data.	R	0

*n : 1~32

Bits	Name	Description	Reset value
[31:0]	Q_END_ADDR	Indicates the end of the section. QSTART_ADDR indicates the start address.	0

AUXQ ADDRESS REGISTERS

For video, the DPSRAM data is saved to the external SDRAM and then decoded. For audio, it is saved to the host CPU's SDRAM via the PCI and then decoded. The AUXQ address registers indicate those saving addresses.

AUXQ_START_ADDR: Start address of the de-multiplexed data (That is, the start address of an image block).

AUXQ_END_ADDR: End address of the de-multiplexed data (That is, the end address of an image block).

AUXQ_START_ADDR register

Name	Address	Description	Type	Reset value
AUXQ_START_ADDR	S_REG_BASE +0x280	Start address of the queue in which to save the DSS auxiliary packet.	R/W	0

Bits	Name	Description	Reset value
[31:0]	AUXQ_START_ADDR	Start address of the auxiliary queue. If the target area is the PCI, it should be a 32-bit value. If the target area is the external SDRAM, it should be a 24-bit value.	0

AUXQ_WRITE_ADDR register

Name	Address	Description	Type	Reset value
AUXQ_WRITE_ADDR	S_REG_BASE +0x284	Write address of the queue in which to save DSS auxiliary packet.	R	0

Bits	Name	Description	Reset value
[31:0]	AUXQ_WRITE_ADDR	Write address of the auxiliary queue	0

PACKET PCR COUNTER REGISTER

The PCR value read from the packet. For TS, it is 42 bits (33 bits + 9 bits). For DSS, it is 32 bits (22 bits + 10 bits).

This register saves the PCR value which was transferred to included an adaptation field or a specific packet in relation to clock recovery. That is, the broadcasting station includes the value based on a 27-MHz clock to the adaptation field of the packet header or a specific PSI packet, during compression of the stream before transfer. The transfer cycle of this information is within 0.1 sec.

The decoding system sets the first OCR value it receives, after initialization, as the counter value of the system reference clock. This counter is operated with the clock (27MHz) of the decoding system, and when a new PCR value is given via a packet, it is compared with the system clock reference counter value to synchronize with the PWM.

The low 9 bits of the system reference clock counter is incremented with the 27-MHz clock, and when the count reaches 300, the high 33-bit counter is increased in increments of one.

PKT_PCR_COUNTER1 register

Name	Address	Description	Type	Reset value
PKT_PCR_COUNTER1	S_REG_BASE +0x290	The PCR value extracted from the packet for which the PCR_EN field of the PCONTROL register is set to "1".	R	0

Bits	Name	Description	Reset value
[31:0]	Q_ PKT_PCR_BASE_ADDR	For MPEG 2 TS, it is the PCR base [0:31] value. For DSS TS, the PCR base [21:0] value is the SCR[31:10] value.	0

PKT_PCR_COUNTER2 register

Name	Address	Description	Type	Reset value
PKT_PCR_COUNTER1	S_REG_BASE +0x290	The PCR value extracted from the packet for which the PCR_EN field of the PCONTROL register is set to "1".	R	0

Bits	Name	Description	Reset value
[8:0]	PKT_PCR_EXT	For MPEG 2 TS, it is the PCR extension value. For DSS TS, it is SCR[8:0].	0
[14:9]	Reserved	Reserved	
[15]	PKT_PCR_BASE	For MPEG 2 TS, it is the PCR base[32] value. For DSS TS, it is SCR[9].	0
[31:16]	Reserved	Reserved	

LATCH PCR COUNTER REGISTER

When extracting the PCR value from the packet, the system clock reference counter value is latched to this register.

This value is compared with the PKT_PCR_COUNTER value to perform clock recovery through the PWM.

LT_PCR_COUNTER1 register

Name	Address	Description	Type	Reset value
LT_PCR_COUNTER1	S_REG_BASE +0x298	The system clock value latched when extracting the PCR value from the packet.	R	0

Bits	Name	Description	Reset value
[31:0]	Q_ PKT_PCR_BASE_ADDR	For MPEG 2 TS, it is the PCR base[0:31] value. For DSS TS, the [31:10] value is the SCR[21:0] value of 32 bits.	0

PKT_PCR_COUNTER2 register

Name	Address	Description	Type	Reset value
LT_PCR_COUNTER1	S_REG_BASE +0x29C	The system clock value latched when extracting the PCR value from the packet.	R	0

Bits	Name	Description	Reset value
[8:0]	LT_PCR_EXT	For MPEG 2 TS, it is the PCR extension value. For DSS TS, it is the SCR[8:0] value.	0
[14:9]	Reserved	Reserved	
[15]	LT_PCR_BASE	For MPEG 2 TS, it is the PCR base[32] value. For DSS TS, it is the SCR[9] value	0
[31:16]	Reserved	Reserved	

COMMAND REGISTERS

This register does not have a direct relationship with the TS demux.

This register is used to control system operations. That is, it is used for play, pause, reset, and synchronization.

COMMAND_REG register

Name	Address	Description	Type	Reset value
COMMAND_REG	S_REG_BASE +0x2A0	Command register	R/W	0

Bits	Name	Description	Reset value
[15:0]	CMD	Command register. Commands are: 0x1000 = VIDEO_Play 0x2000 = VIDEO_Pause 0x3000 = VIDEO_Reset 0x4000 = SET_AVsync	0
[30:16]	Reserved		
[31]	CMD_VALID	Command validity. Indicates whether the command set on the CMD field is valid or not. When the CMD field is set to "0", a new command is written and then set to "1". This field is cleared to "0" automatically after SAM2K reads the command.	0

CMD_ARG1 ~ CMD_ARG4 registers

Name	Address	Description	Type	Reset value
CMD_ARG1	S_REG_BAS+ 0x2A4+4*(n-1)	Command argument register	R/W	0

*n = 1 ~ 4

Bits	Name	Description	Reset value
[31:0]	ARG	Arguments used in the command. It indicates the video number, queue number, and whether A/V synchronization is on/off, etc. Arguments should be used in the order that the command requires. For example, in the case of VIDEO_Pause, the video number should be set on CMD_ARG1 and the On/Off should be set on CMD_ARG2.	0

*Note: For example, in the case of VIDEO_Play (arg1, arg2), appropriate values should be set for ARG1 and ARG2 before calling it and then it should be called.

CMD_STATUS register

Name	Address	Description	Type	Reset value
CMD_STATUS	S_REG_BASE +0x2C0	Current command status	R	0

Bits	Name	Description	Reset value
[31:0]	CMD_S	Indicates the status of the command currently being performed. Possible command statuses are: 0x00 = IDLE 0x02 = RUNNING 0x04 = FAIL 0x08 = DONE. IDLE indicates the initial state. RUNNING indicates the command is in operation. FAIL indicates the command was not performed. DONE indicates the command was performed successfully.	0

ARM_INT_STATUS register

Name	Address	Description	Type	Reset value
ARM_INT_STATUS	S_REG_BASE +0x250	Flag that indicates the ISR operation status of the ARM7 or external CPU on the SP interrupt generation.	R	0

Bits	Name	Description	Reset value
[0]	?	?	
[1]	DEC_INTR	Indicates the ISR operation status of the CPU or ARM7 on the DEC_INTR generation.	0
[2]	PIC_INTR	Indicates the ISR operation status of the CPU or ARM7 on the PIC_INTR generation.	0
[3]	GOP_INTR	Indicates the ISR operation status of the CPU or ARM7 on the GOP_INTR generation.	0
[4]	SEQ_INTR	Indicates the ISR operation status of the CPU or ARM7 on the SQ_INTR generation.	0
[31:5]	?	?	

ARM STATUS REGISTER

The current debug status is written to this register when debugging ARM7. Therefore, the content to write to this register will differ depending on how to use it with the debugging S/W you create.

ARM_STATUS register

Name	Address	Description	Type	Reset value
ARM_STATUS	S_REG_BASE +0x260~0x26C	For ARM7 debugging	R	0

Bits	Name	Description	Reset value
[31:0]	ARM_S	When debugging, you can write the value so that you can check out the internal situation of the chip by reading this register externally. For example , you can write the timer value to this register when an external interrupt occurs. Then, you let the host CPU read this register to check the current status of the timer.	0

VIDEO PTS (Presentation Time Stamp) REGISTER

This register contains the PTS value of the frame currently being decoded. Otherwise, it contains the PTS value of the most recent decoded frame.

VIDEO_PTS0 ~ VIDEO_PTS2 registers

Name	Address	Description	Type	Reset value
VIDEO_PTS0~ VIDEO_PTS2	S_REG_BASE +0x270~0x278	VIDEO_PTS0~1 are the PTS values of the I and P frames. VIDEO_PTS2 is the PTS value of the B frame.	R	0

Bits	Name	Description	Reset value
[30:0]	PTS VALUE	High 31 bits [32:2] of video PTS.	0
[31]	VALIDITY	PTS value validity flag	

VIDEO PTS (Presentation Time Stamp) Q REGISTERS

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VIDEO_PTSQ_HIGH0 ~ VIDEO_PTSQ_HIGH47 registers

Name	Address	Description	Type	Reset value
VIDEO_PTSQ_HIGH0~ VIDEO_PTSQ_HIGH47	S_REG_BASE +0x280~0x33C	PTS queue write pointer on Vbv buffer	R	0

Bits	Name	Description	Reset value
[14:0]	WRITE_POINTER	Write pointer: Q_hdr_addr[23:10]: Because SAM2K' s memory is 15 bits, Q_hdr_addr [31:25]becomes 0.	R
[30:15]	–	Not used	–
[31]	VALIDITY	PTS queue value validity flag	R

VIDEO_PTSQ_LOW0 ~ VIDEO_PTSQ_LOW47 registers

Name	Address	Description	Type	Reset value
VIDEO_PTSQ_LOW0~ VIDEO_PTSQ_LOW47	S_REG_BASE +0x340~0x3EC	PTS value buffer	R	0

Bits	Name	Description	Reset value
[30:0]	PTS VALUE	Filter byte data 7	R
[31]	–	Not used	–

FILTER MASK REGISTER

This register contains information for the section of the packet data that passed the PID filter, or the section that controls filtering for the payload.

It has an 8-byte filter depth. With this register, you can control the Filtering Enable/Disable for each byte and point to which position of the packet will be filtered. If filtering is disabled, you should set the POS value to 0.

FILTER_MASK1 ~ FILTER_MASK32 registers

Name	Address	Description	Type	Reset value
FILTER_MASK 1 ~ FILTER_MASK 32	S_REG_BASE +0x400~0x47C	Set the filter byte mask and the data offset.	R/W	0

Bits	Name	Description	Reset value
[2:0]	POS7	Relative byte offset of Byte 7 from Byte 6. Therefore, the actual position of Byte 7 is POS1+POS2+POS3...+POS7.	R/W
[5:3]	POS6	Relative byte offset of Byte 6 from Byte 5. Therefore, the actual position of Byte 6 is POS1+POS2...+POS6.	R/W
[8:6]	POS5	Relative byte offset of Byte 5 from Byte 4. Therefore, the actual position of Byte 5 is POS1+POS2...+POS5.	R/W
[11:9]	POS4	Relative byte offset of Byte 4 from Byte 3. Therefore, the actual position of Byte 4 is POS1+POS2+POS3+POS4.	R/W
[14:12]	POS3	Relative byte offset of Byte 3 from Byte 2. Therefore, the actual position of Byte 3 is POS1+POS2+POS3.	R/W
[17:15]	POS2	Relative byte offset of Byte 2 from Byte 1. Therefore, the actual position of Byte 2 is POS1+POS2.	R/W
[20:18]	POS1	Byte position of Byte 1. The position of the first byte of the section is 0. For MPEG2, POS1 should be equal to or larger than 3.	R/W
[22:21]	–	Reserved	–
[23]	F_MODE	Filter mode bit. Set to "0" to check whether it is the same as the data set on the filter. Otherwise, set to "1". "1" means negative filtering mode.	R/W
[24]	CRC	CRC check on/off. Indicates whether to check the CRC. When set to "1", CRC is checked and the section data sis discarded if it does not match.	R/W
[25]	BYTE_M7	Byte 7 enable. "1" means Byte 7 is valid.	R/W
[26]	BYTE_M6	Byte 6 enable. "1" means Byte 6 is valid.	R/W
[27]	BYTE_M5	Byte 5 enable. "1" means Byte 5 is valid.	R/W
[28]	BYTE_M4	Byte 4 enable. "1" means Byte 4 is valid.	R/W
[29]	BYTE_M3	Byte 3 enable. "1" means Byte 3 is valid. For DSS, this field is ignored.	R/W

FILTER MASK REGISTER (continued)

Bits	Name	Description	Reset value
[30]	BYTE_M2	Byte 2 enable. "1" means Byte 2 is valid. For DSS, this field is ignored.	R/W
[31]	BYTE_M1	Byte 1 enable. "1" means Byte 1 is valid. For DSS, this field is ignored.	R/W

FILTER DATA REGISTERS

These registers save the data to the filter.

FILTER_DATA_HIGH1 ~ FILTER_DATA_HIGH32 registers

Name	Address	Description	Type	Reset value
FILTER_DATA_HIGH1~ FILTER_DATA_HIGH 32	S_REG_BASE +0x480~0x4FC	High 4 bytes of filter data	R/W	0

Bits	Name	Description	Reset value
[7:0]	BYTE3	Filter byte data 3. For DSS, it is table_id[7:0].	R/W
[15:8]	BYTE2	Filter byte data 2. For DSS, it is table_id[15:8]	R/W
[23:16]	BYTE1	Filter byte data 1. For DSS, it is table_id[23:16]	R/W
[31:24]	TABLE_ID	table_id[7:0] of the section. For DSS, it is table_id[31:24]	R/W

FILTER_DATA_LOW1 ~ FILTER_DATA_LOW32 registers

Name	Address	Description	Type	Reset value
FILTER_DATA_LOW1~ FILTER_DATA_LOW 32	S_REG_BASE +0x500~0x57C	Low 4 bytes of filter data	R/W	0

Bits	Name	Description	Reset value
[7:0]	BYTE7	Filter byte data 7	R/W
[15:8]	BYTE6	Filter byte data 6.	R/W
[23:16]	BYTE5	Filter byte data 5.	R/W
[31:24]	BYTE4	Filter byte data 4	R/W

FILTER STATE REGISTERS

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F_STATE1 ~ F_STATE32 registers

Name	Address	Description	Type	Reset value
F_STATE 1~ F_STATE 32	S_REG_BASE +0x580~0x5FC	Filter state		

Bits	Name	Description	Reset value
[31:0]			

FILTER CRC REGISTERS

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F_CRC1 ~ F_ CRC32 registers

Name	Address	Description	Type	Reset value
F_CRC 1 ~ F_CRC 32	S_REG_BASE +0x600~0x67C	Filter CRC		

Bits	Name	Description	Reset value
[31:0]			

FILTER HEADER ADDRESS REGISTERS

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F_HDR_ADDR1 ~ F_ HDR_ADDR32 registers

Name	Address	Description	Type	Reset value
F_HDR_ADDR 1 ~ F_HDR_ADDR 32	S_REG_BASE +0x680~0x6FC	Filter header address		

Bits	Name	Description	Reset value
[31:0]			

NOTE

4 PCI & DMA

OVERVIEW

When the PCI block becomes bus master, it can read/write data from/to the memory of the host system. When it becomes the target, the host system controls it and it works as an interface for data transfer. The internal control registers and local memory (SDRAM) area of SAM2K-LITE can be accessed via the PCI bus. SAM2K-LITE's PCI block can be largely divided into the master interface module and the target only interface module. The master interface module has the PCI master/target function and consists of PCI_GP_IF, PCI_AD_IF, PCI_TS_DP_IF, PCI_SP_IF, and PCI_HSMB_IF. The PCI target only module can only receive data from the bus in slave mode, and consists of PCI_TAR_HSMB_IF, PCI_SRAM_IF, and PCI_REG_IF.

For audio data, since it is not decoded by SAM2K-LITE, it is transferred to the host CPU via the PCI. The audio data decoded by the host CPU is then transferred back to SAM2K-LITE via the PCI and output on the dedicated output port. In addition, the PSI (Packet Specific Information) data is transferred to the host CPU via the PCI.

For video data, it is transferred to the external memory via DMA1 as described in Chapter 3.

PCI CONTROLLER FEATURES

- PCI Master and target device
- 32-bit up to 33 MHz at 3.3V
- PCI Local Bus Specification Rev. 2.1 compliant
- System clock can run asynchronously to PCI clock
- Supports two base address registers
  - ⓐ Memory base address 0 : prefetchable, 4MBytes fixed size

    Allocated for internal memory used in each PCI interface module like System controller, SP, DPSRAM
  - ⓑ Memory base address 1 : prefetchable, 32Mbytes fixed size

    Allocated for external HSMB for external SDRAM
- Four independent 8-word deep FIFO
- Not supports 64-bit addressing

TERMINOLOGY OF REGISTER GROUPS

- SFR (Special Function Registers) : There is no PCI specific register
- PCI configuration registers : PCI configuration header (can be accessed by configuration cycle)

Architecture

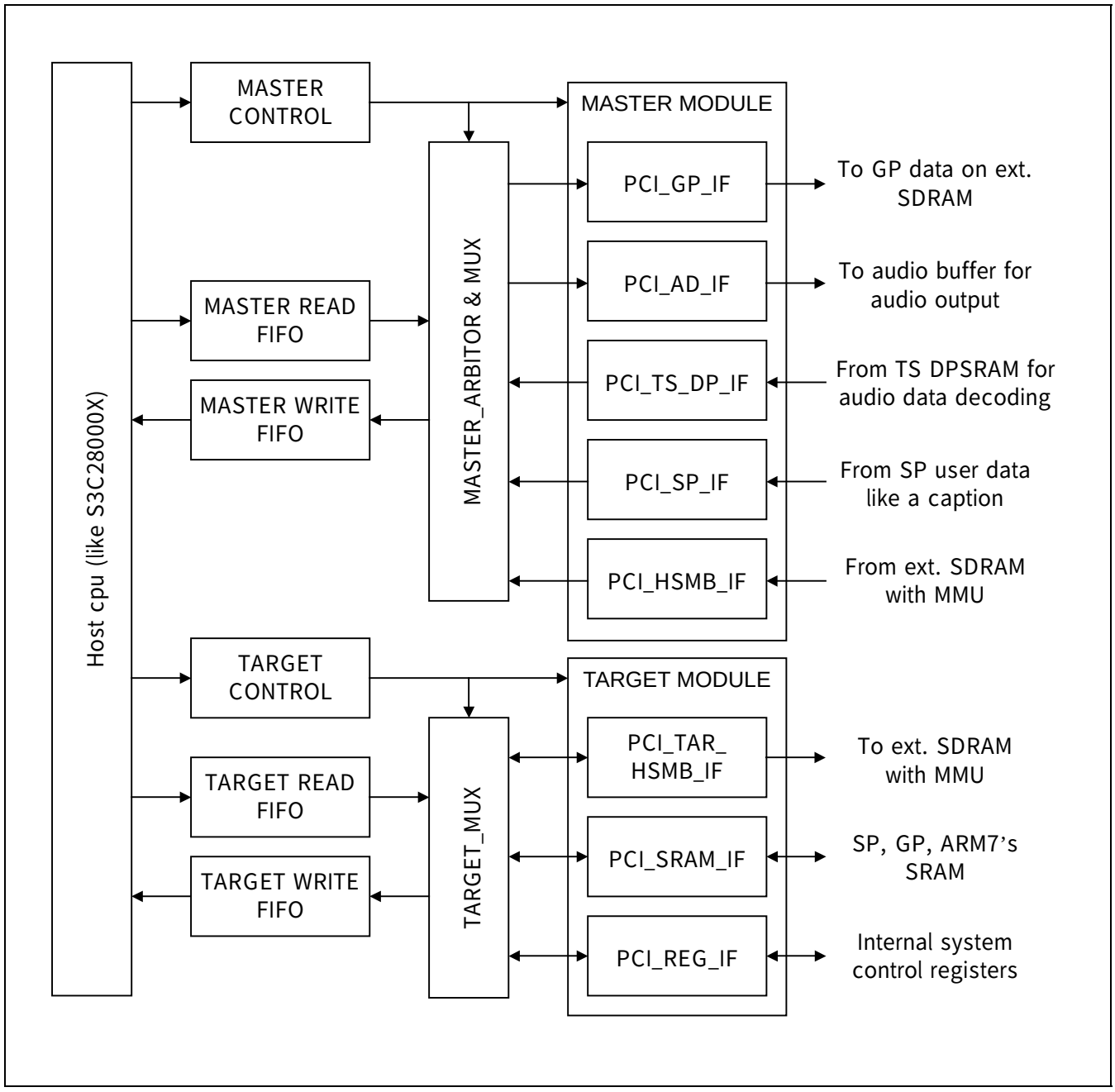

Figure 4-1 PCI block diagram

PCI Configuration Registers

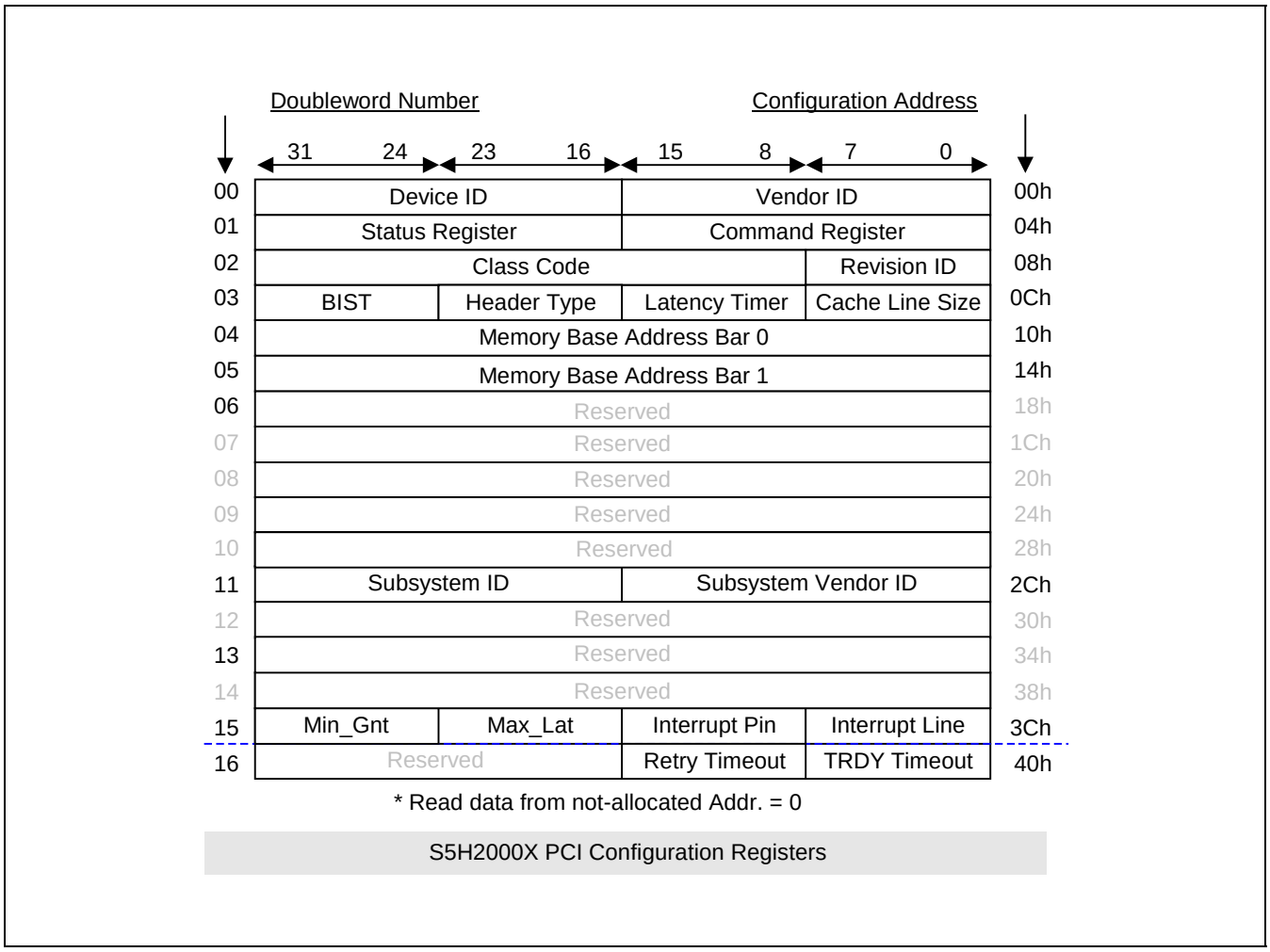

Figure 17-10. PCI Configuration Registers

All configuration registers are described in "PCI Local Bus Specification Revision 2.1".

Because the PCI configuration space of SAM2K-LITE is not connected to the internal bus of SAM2K-LITE, it can be accessed only by an external PCI device. Therefore, the initial value should be set during registration of the device driver or with the host CPU.

Table 4-2. PCI Configuration Registers Overview

Offset	Bits	Name	R/W(1)		Description	Reset Value
			LB(2)	PCI		
0x00	[15:0]	Vendor ID	-	R/O	Chip vendor identification	0x144D
	[31:16]	Device ID	-	R/O	Chip device identification	0xA010
0x04	[15:0]	Command Register	-	R/W	Basic control register to perform PCI access	0x0000
	[31:16]	Status Register	-	R/W/C	PCI bus-related status register	0x0280
0x08	[7:0]	Revision ID	-	R/O	Identifies the revision number of the device	0x00
	[31:8]	Class Code	-	R/O	Identifies the basic function of the device	0x048000
0x0C	[7:0]	Cache Line Size	-	R/W	System cache line size	0x00
	[15:8]	Latency Timer	-	R/W	Maximum clocks that master can own the bus	0x00
	[23:16]	Header Type	-	R/O	Indicates a single or multi-function	0x00
	[31:24]	BIST	-	R/O	Register for built-in self-test	0x00
0x10	[31:0]	Memory Base Address 0	-	R/O	Memory bar 0 size and location (of fast decode)	0x0000 0000
0x14	[31:0]	Memory Base Address 1	-	R/O	Memory bar 1 size and location (of medium decode)	0x0000 0000
0x18–0x2B		Reserved	-		Reserved	
0x2C	[15:0]	Subsystem Vendor ID	-	R/O	Add-in card or subsystem vendor identification	0x0000
	[31:16]	Subsystem ID	-	R/O	Add-in card or subsystem identification	0x0000
0x30–0x3B		Reserved	-		Reserved	
0x3C	[7:0]	Interrupt Line	-	R/O	Interrupt request line routing information	0x00
	[15:8]	Interrupt Pin	-	R/O	Interrupt request pin number (INTA#)	0x01
	[23:16]	Min_Gnt	-	R/O	Minimum time of how long master needs burst period	0x00
	[31:24]	Max_Lat	-	R/O	Maximum time of how often device needs to gain access	0x00
0x40	[7:0]	TRDY Timeout	-	R/W	Maximum time of master wait for TRDY#	0x80
	[16:8]	Retyr Timeout	-	R/W	Maximum number of master retry	0x80
	[31:17]	Reserved			Reserved	

NOTE: 1. R/O = Read-only, R/W = Read and Write, R/WC = Read and Write 1 to clear.

2. Cannot be accessed via the LB (Local Bus).

PCI Vendor ID & Device ID Register (PCIVDIDR)

This register identifies the manufacture of the device and the particular device.

Register	Address	R/W	Description	Reset Value
PCIVDIDR	0x0000	R	PCI vendor ID and device ID register	0xA010144D

PCIVDIDR	Bit	Description	Initial State
DEVID	[31:16]	Chip device identification (Read-only) This field identifies the particular device. This identifier is allocated by the vendor.	0x A010
VENID	[15:0]	Chip vendor identification (Read-only) This field identifies the manufacturer of the device.	0x144D

PCI Status & Command Register (PCISCR)

The Status register (PCISCR[31:16]) is used to record status information for PCI bus related events. Reserved bits should be read-only and return zero when read. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but no set. A one bit is reset whenever the register is written, and the write data in the corresponding bit location is a 1.

The Command register (PCISCR[15:0]) provide coarse control over a device's ability to generate and respond to PCI cycles. When a 0 is written to this register, the device is logically disconnected from the PCI bus for all accesses except configuration accesses.

Register	Address	R/W	Description	Reset Value
PCISCR	0x0004	R/W	PCI status and command register	0x0280 0000

PCISCR	Bit	Description	Initial State
Detected Parity Error	[31]	Detected parity error status bit (Read or write-1-to-clear) This bit must be set by a device whenever it detects a parity error, regardless of the state of the parity error response bit (PCISCR[6]). This bit is required to be set by the device when any of the following conditions occurs: 1) The device's parity checking logic detects an error in a single address cycle or either address phase of a dual address cycle. 2) The device's parity checking logic detects a data parity error and the device is the target of a write transaction. 3)The device's parity checking logic detects a data parity error and the device is the master of a read transaction.	0
Signaled System Error	[30]	Signaled system error bit (Read or write-1-to-clear) This bit must be set whenever the device asserts **SERR**#.	0

PCISCR	Bit	Description	Initial State
Received Master Abort	[29]	Received master abort bit (Read or write-1-to-clear) This bit must be set by a master device whenever its transaction (except for Special Cycle) is terminated with Master-Abort.	0
Received Target Abort	[28]	Received target abort bit (Read or write-1-to-clear) This bit must be set by a master device whenever its transaction is terminated with Target-Abort.	0
Signaled Target Abort	[27]	Signaled target abort bit (Read or write-1-to-clear) This bit must be set by a target device whenever it terminates a transaction with Target-Abort.	0
DEVSEL timing	[26:25]	DEVSEL# response timing bits (Read or write-1-to-clear) These bits encode the timing of **DEVSEL**#. A specifies three allowable timings for assertion of **DEVSEL**#. 00 = fast timing 01 = medium timing 10 = slow timing 11 = reserved It asserts DEVSEL# on the second clock after FRAME# is assert by a PCI master attempting to access memory. These bits are read-only and must indicate the slowest time that a device asserts **DEVSEL#** for any bus command except Configuration Read and Configuration Write.	01
Master Data Parity Error	[24]	Master data parity error status bit (Read or write-1-to-clear) If the parity response bit(PCISCR[6] is cleared, the master must not set this bit, even if the master detects a parity error or the target asserts PERR#. Targets never set this bit. This bit is only implemented by bus masters. It is set when three conditions are met: 1) the bus agent asserted **PERR#** itself (on a read) or observed **PERR#** asserted (on a write); 2) the agent setting the bit acted as the bus master for the operation in which the error occurred; 3) the Parity Error Response bit (PCISCR[6]) is set.	0
Fast Back-to-Back Capable	[23]	Fast back to back capable bit (Read or write-1-to-clear) This bit indicates whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent. 0 = Not capable the fast back-to-back transaction. 1 = Capable the fast back-to-back transaction.	1
Reserved	[22]	Reserved	0

PCISCR	Bit	Description	Initial State
66MHz Capable	[21]	This bit indicates whether or not this device is capable of running at 66 MHz. (Read only) 0 = Capable 33 MHz. 1 = capable 66 MHz **NOTE** : S5H2000X support only 33MHz capable.	0
Capabilities List	[20]	Capabilities list pointer bit (Read only) This bit indicates whether or not this device implements the pointer for a New Capabilities linked list at offset 34h. 0 = No available New Capabilities linked list. 1 = Available New Capabilities linked list.	0
Reserved	[19:10]	Reserved	
Fast Back-to-Back Enable	[9]	Fast back-to-back write enable bit This bit controls whether or not a master can do fast back-to-back transactions to different devices. Initialization software will set the bit if all targets are fast back-to-back capable. 0 = The master is allowed to generate fast back-to-back transactions to the same agent. 1 = The master is allowed to generate fast back-to-back transactions to different agents.	0
SERR# Enable	[8]	This bit is an enable bit for the **SERR#** driver. 0 = disables the **SERR#** driver when a PCI bus address parity error is detected. 1 = enables the **SERR#** driver when a PCI bus address parity error is detected. All devices that have an **SERR#** pin must implement this bit. Address parity errors are reported only if this bit and parity error response bit (PCISCR[6]) are 1.	0
Stepping Control	[7]	This bit is used to control whether or not a device does address/data stepping. 0 = Devices that never do stepping. 1 = Devices that always do stepping. **NOTE** : S5H2000X is not supported.	0

PCISCR	Bit	Description	Initial State
Parity Error Response	[6]	This bit controls the device's response to parity errors. 0 = The device sets its Detected Parity Error status bit (PCISCR[31]) when an error is detected, but does not assert **PERR#** and continues normal operation. 1 = The device must take its normal action when a parity error is detected.	0
VGA Palette Snoop	[5]	This bit controls how VGA compatible and graphics devices handle accesses to VGA palette registers. 0 = Disable palette snooping. (The device should treat palette write accesses like all other accesses.) 1 = Enable palette snooping. (The device does not respond to palette register writes and snoops the data.) **NOTE** : S5H2000X is not supported.	0
Memory Write and Invalidate Enable	[4]	This is an enable bit for using the Memory Write and Invalidate command. 0 = Disable the command (Memory Write command is used). 1 = Enable the memory write and invalidate command. **NOTE** : S5H2000X is not supported.	0
Special Cycle	[3]	Controls a device's action on Special Cycle operations. 0 = Disable Special Cycle operations. 1 = Enable Special Cycle operations. **NOTE** : S5H2000X is not supported	0
Bus Master	[2]	Controls a device's ability to act as a master on the PCI bus. 0 = Disables the device from generating PCI accesses. 1 = Enable the device to behave as a bus master.	0
Memory space	[1]	Controls a device's response to Memory Space accesses. 0 = Disable master to respond as a PCI memory target. 1 = Enable master to respond as a PCI memory target. If this bit is "1", S5H2000X Memory Space cannot be accessed by a different PCI device. S5H2000X memory space is a type that is set in the Memory Base Address Register(BAR) 0/1,PCIBAR0/1.	0
IO space	[0]	Controls a device's response to I/O Space accesses. 0 = Disable master to respond as a PCI I/O target. 1 = Enable master to respond as a PCI I/O target. **NOTE** : S5H2000X is not supported	0

PCI Class Code & Revision ID Register (PCICRIDR)

The Class Code register (PCICRIDR[31:8]) is read-only and is used to identify the generic function of the device

and, in some case, a specific register-level programming interface, The register is broken into three byte-size fields. The upper byte is a base class code. The middle byte is a sub-class code. The lower byte identifies a specific register-level programming interface.

Register	Address	R/W	Description	Reset Value
PCICRIDR	0x0008	R/W	PCI class code and revision ID register	0x0480 0000

PCICRIDR	Bit	Description	Initial State
BASCLS	[31:24]	Base class code bits These bits indicate that it broadly classifies the type of function the device performs.	0x04
SUBCLS	[23:16]	Sub-class code bits These bits indicate that it identifies more specifically the function of device.	0x80
SRLPI	[15:8]	Specific register-level programming interface bits These bits indicate that it identifies a specific register-level programming interface so that device dependent software can interact with the device.	0x00
REVID	[7:0]	Revision ID bits These bits are used to specifies a device specific revision identifier. The value is chosen by the vendor. Zero is acceptable value.	0x00

PCI General Control Register (PCIGCONR)

Register	Address	R/W	Description	Reset Value
PCIGCONR	0x000C	R/W	PCI general control register	0x0000 0000

PCIGCONR	Bit	Description	Initial State
SUPBIST	[31]	BIST (Built-in Self Test) capable bit (Read-only) 0 = Not BIST capable 1 = Support BIST **NOTE**: S5H2000X is not supported.	0
STRBIST	[30]	BIST (Bulit-in Self Test) start bit (Read-only) Write a 1 to invoke BIST. Device resets the bit when BIST is complete. Software should fail the device if BIST is not complete after 2 seconds. **NOTE**: S5H2000X is not supported.	0
–	[29:28]	Reserved	00
COMCODE	[27:24]	Completion code bits (Read-only) Device-specific failure codes can be encoded in the non-zero value. 0 = The device has passed its test. Non zero values = The device failed. **NOTE**: S5H2000X is not supported.	0x0
HDTYPFUNC	[23]	Multi-function device select bit(Header Type) (Read-only) 0 = single function device 1 = multi function device	0
PREDHD	[22:16]	The layout of the 2nd part of predefined header bits.(Read-only) 00 = Type 00h configuration space header 01 = PCI-to-PCI bridges 1x = Reserved	0x00
LATTIME	[15:8]	Latency timer bits Maximum clocks that master can own the bus. These bits specifies the value of the latency timer for this PCI bus master in units of PCI bus clocks	0x00
CACHELSIZ	[7:0]	System Cache Line size bits These bits specifies the system cache size in units of DWORDs. These bits is used by master devices to determine whether to use Read, Read Line, or Read Multiple commands for accessing memory. A device may limit the number of cache line sizes that it can support. If an unsupported value is written to these bits, the device should behaves as if a value of 0 was written. **NOTE**: S5H2000X is not supported.	0x00

PCI Base Address Registers (PCIBARN)

Register	Address	R/W	Description	Reset Value
PCIBAR0	0x0010	R/W	Memory bar 0 size and location (of fast decode)	0x0000 0000
PCIBAR1	0x0014	R/W	Memory bar 1 size and location (of medium decode)	0x0000 0000

PCIBARn	Bit	Description	Initial State
BASEADDR	[31:4]	PCI base address bits	0x000 0000
ADPREFT	[3]	Prefetchable bit(In case of memory space) (Read-only) 0 = Not prefetchable data 1 = Pre-fetchable data In case of I/O space, this bit is used to base address.	0
ADDRSPS	[2:1]	Base address space select bits (In case of memory space) (Read-only) 00 = Base register is 32 bits wide and can be mapped anywhere in the 32-bit memory space. 10 = Base register is 64 bits wide and can be mapped anywhere in the 64-bit memory space. (Not supported) Other values = Reserved In case of I/O space, Bit 2 is used to base address and Bit 1 is always 0. **NOTE**: S5H2000X is not support I/O space.	00
ADMAPSEL	[0]	Address map select bit. (Read-only) 0 = Memory space indicator (PCIBAR0, PCIBAR1) 1 = I/O space indicator **NOTE**: S5H2000X is not support I/O space.	0

PCI Subsystem & Subsystem Vendor ID Register (PCISSVIDR)

This register is used to uniquely identify the expansion board or subsystem where the PCI device resides.

Register	Address	R/W	Description	Reset Value
PCISSVIDR	0x002C	R/W	PCI subsystem and subsystem vendor ID register	0x0000 0000

PCISUBSYSIDR	Bit	Description	Initial State
SUBSYSID	[31:16]	PCI subsystem ID bits. These bits are used to uniquely identify the subsystem where the PCI device resides. **NOTE**: S5H2000X is not support subsystem ID.	0x0000
SUBSYSVENID	[15:0]	PCI subsystem vendor ID bits. These bits can be obtained from the PCI signal and used to identify the vendor of the expansion board or subsystem. The values are vendor specific. **NOTE**: S5H2000X is not support subsystem vendor ID.	0x0000

PCI Miscellaneous Register (PCIMISCR)

Register	Address	R/W	Description	Reset Value
PCIMISCR	0x003C	R/W	PCI miscelaneous register	0x0000 0100

PCIMISCR	Bit	Description	Initial State
MAX_LAT	[31:24]	Maximum latency timer value bits These bits are used for specifying how often the device needs to gain access to PCI bus. The value specifies a period of time in units of 0.25μs (at 33MHz). Values of 0 indicate that the device has no major requirements for the settings of the latency timers. Values should be chosen assuming that the target does not insert any wait-states.	0x00
MIN_GNT	[23:16]	Minimum grant timer value bits These bits are used for specifying how long a burst period the device needs assuming a clock rate of 33MHz. The value specifies a period of time in units of 0.25μs. Values of 0 indicate that the device has no major requirements for the settings of the latency timers. Values should be chosen assuming that the target does not insert any wait-states.	0x00
INT_PIN	[15:8]	Interrupt pin select bits(Read only) 0x00 = No use interrupt pin 0x01 = INTA# Other values = Reserved	0x01
INT_LINE	[7:0]	Interrupt line bits The value of these bits tells which input of the system interrupt controller the device's interrupt pin is connected to. The device itself does not use this value, rather it is used by device drivers and operating systems. Device drivers and operating systems can use this information to determine priority and vector information. POST software will write the routing information into these bits as it initializes and configures the system.	0x00

PCI Target Ready & Retry Timeout Register (PCITOR)

Register	Address	R/W	Description	Reset Value
PCITOR	0x1008 0040	R/W	PCI target ready and retry timeout register	0x0000 8080

PCITOR	Bit	Description	Initial State
RETRYTOUT	[15:8]	Maximum times of master retry The value specifies a period of time in frame units.	0x80
TRDYTOUT	[7:0]	Maximum time of master wait for TRDY# The value specifies a period of time in units of 30.3ns (at 33MHz).	0x80

MASTER MODULE STATUS REGISTER (MMSR)

This register gives information on which of the 5 modules (that can operate as the bus master) is currently performing a PCI operation with the DMA, when the PCI block operates as the PCI bus master. When the relevant bit is set to 1, it means that the module is currently performing a PCI operation.

GSCR_MMSR register (Global Status & Control Register)

Name	Address	Description	Type	Reset value
GSCR_MMSR	BAR0+0ch	Master Module Status Register	R	0

Bits	Name	Description	Reset value
[0]	DMA1	PCI operating status of pci_w_ts_dpsram 0 = Not operating 1 = Operating	0
[1]	DMA2	PCI operating status of pci_gp_if 0 = Not operating 1 = Operating	0
[2]	DMA3	PCI operating status of pci_hsmb_if 0 = Not operating 1 = Operating	0
[3]	DMA4	PCI operating status of pci_audio_pcm 0 = Not operating 1 = Operating	0
[4]	DMA5	PCI operating status of pci_audio_stream 0 = Not operating 1 = Operating	0
[31:5]	–	Reserved	–

SOFT RESET REGISTER (SRN)

The setting of this register could reset each peripheral.

GSCR_SRN register (Global Status & Control Register)

Name	Address	Description	Type	Reset value
GSCR_SRN	BAR0+14h	Soft Reset_N	R/W	0

Bits	Name	Description	Reset value
[0]	PCI_RESET	PCI Reset (Power On Reset), read only	0
[1]	ARM_RESET	ARM Reset 0 = Reset asserted 1 = Reset Not asserted	0
[5]	SP_HALT	SP Reset 0 = Reset asserted 1 = Reset Not asserted	0
[7]	MMU_RESET	MMU Reset 0 = Reset asserted 1 = Reset Not asserted	0
[8]	MPEG_RESET	MPEG Reset 0 = Reset asserted 1 = Reset Not asserted	0
[9]	DP_RESET	DP Reset 0 = Reset asserted 1 = Reset Not asserted	0
[10]	GA_RESET	GA Reset 0 = Reset asserted 1 = Reset Not asserted	0
[11]	GP_RESET	GP Reset 0 = Reset asserted 1 = Reset Not asserted	0
[31:12]	–	Reserved	–

TS_DPSRAM DMA

TS_DPSRAM consists of three 188-byte buffers and saves the TS stream input from external sources. Then, SAM2K-LITE TS-demux transfers the data to the destination block according to data type by recognizing whether it is section, audio or video data. Section and audio data are transferred to the system memory via the PCI bus so that the CPU can process them. Video data is transferred to the local memory of the S5H2000X via the DMA1. The local TS_DPSRAM control block saves the TS stream and transfers the data via the PCI using the DMA operation.

LTCR1 PCI START ADDRESS REGISTER (PSA)

This register specifies the destination (system memory) address to which the TS stream is transferred. The specified address should be a PCI address. The addressing unit is a byte.

LTCR1_PSA register (Local TS_DPSRAM Control Register 1)

Name	Address	Description	Type	Reset value
LTCR1_PSA	BAR0+c0h	PCI Start Address	R/W	0

Bits	Name	Description	Reset value
[31:0]	PSA	Target start address in the PCI memory System memory address. The addressing unit is a byte.	0

LTCR1 LOCAL START ADDRESS REGISTER (LSA)

This register specifies the address of the source which will be transferred to the destination (system memory) via DMA. The source address should be the start address of a TS_DPSRAM buffer. There are three DPSRAMs and their address can be a location within the addressing space of 0 ~ 188*3. That is, the addressing space of DPSRAM 0 is 0 ~ 187; DPSRAM 1, 188 ~ 375; DPSRAM 2, 376 ~ 563. The addresses of LTCR_LSA should be specified within the above ranges.

LTCR1_PSA register (Local TS_DPSRAM Control Register 1)

Name	Address	Description	Type	Reset value
LTCR1_LSA	BAR0+c4h	Local Start Address	R/W	0

Bits	Name	Description	Reset value
[31:0]	LSA	Local start address in TS_DPSRAM memory	0

TRANSFER BYTE COUNTER REGISTER (TBC)

LTCR1_TBC register (Local TS_DPSRAM Control Register 1)

Name	Address	Description	Type	Reset value
LTCR1_TBC	BAR0+c8h	Transfer Byte-Count	R/W	0

Bits	Name	Description	Reset value
[9:0]	TBC	Transfer byte-count	0
[31:10]	–	Reserved	–

AUXILIARY CONTROL REGISTER (AxC)

LTCR1_AxC register (Local TS_DPSRAM Control Register 1)

Name	Address	Description	Type	Reset value
LTCR1_AxC	BAR0+cch	Auxiliary Control	R/W	0

The Transfer Data Type Selection Bit (LTCR1_AxC[0]) gives the interrupt block the information for the type of data to be transferred and generates the interrupt of the audio DMA done or the section DMA done by differentiating the interrupt source when the data transfer finishes. This bit is set when the DMA transfer finishes. Therefore be careful to note that once a DMA operation has begun, if you select a different data type from the current data type before it finishes, the wrong interrupt will be generated.

The DPSRAM buffer selection should be used with the value fixed to "0".

Bits	Name	Description	Reset value
[0]	SECTION_SEL	Trasnfer data type selection: 0 = section data 1 = audio data	0
[1]	MUX_SEL	DPSRAM Buffer selection: 0 = select buff_0 1 = select buff_1 Should be used with the value fixed to "0".	0
[6:2]	–	Reserved	–
[7]	–	For test only, always "0"	0
[8]	START_DMA	DMA start enable: 0 = no effect 1 = start DMA when write "1" and be cleared by H/W	0
[31:9]	–	Reserved	–

TRANSFERED BYTE COUNTER REGISTER (XBC)

.

LTCR1_XBC register (Local TS_DPSRAM Control Register 1)

Name	Address	Description	Type	Reset value
LTCR1_XBC	BAR0+d0h	Transferred Byte-Count	R	0

Bits	Name	Description	Reset value
[9:0]	XBC	Transferred byte-count	0
[31:10]	–	Reserved	–

ERROR STATUS REGISTER (ESR)

.

LTCR1_ESR register (Local TS_DPSRAM Control Register 1)

Name	Address	Description	Type	Reset value
LTCR1_ESR	BAR0+d4h	Error Status	R	0

Bits	Name	Description	Reset value
[0]	FATAL	Access out of memory (BARs) bound (master abort)	0
[1]	PERR	Parity error	0
[31:2]	–	Reserved	–

GP DMA

PCI START ADDRESS REGISTER (PSA)

.

LGCR_PSA register (Local GP Control Register)

Name	Address	Description	Type	Reset value
LGCR_PSA	BAR0+e0h	PCI Start Address	R	0

Bits	Name	Description	Reset value
[31:0]	PSA	Start address of PCI memory	0

DATA SIZE REGISTER (DSR)

.

LGCR_DSA register (Local GP Control Register)

Name	Address	Description	Type	Reset value
LGCR_DSR	BAR0+e4h	Data Size	R	0

Bits	Name	Description	Reset value
[15:0]	DSR	Word (32bits) data size	0
[31:16]	–	Reserved	–

AUXILIARY CONTROL REGISTER (AxC)

.

LGCR_AxC register (Local GP Control Register)

Name	Address	Description	Type	Reset value
LGCR_AxC	BAR0+e8h	Auxiliary Control	R/W	0

Bits	Name	Description	Reset value
[7:0]	MBS	Minimum block size (for wcount 1)	0
[8]	START_DMA	0 = no effect 1 = start DMA when write "1" and be cleared by H/W	0
[31:9]	–	Reserved	–

TRANSFERRED DATA SIZE REGISTER (TDS)

.

LGCR_TDS register (Local GP Control Register)

Name	Address	Description	Type	Reset value
LGCR_TDS	BAR0+ech	Transferred Data Size	R	0

Bits	Name	Description	Reset value
[15:0]	TDS	Minimum block size (for wcount 1)	0
[31:16]	–	Reserved	–

ERROR STATUS REGISTER (ESR)

.

LGCR_ESR register (Local GP Control Register)

Name	Address	Description	Type	Reset value
LGCR_ESR	BAR0+f0h	Error Status	R	0

Bits	Name	Description	Reset value
[0]	FATAL	Access out of memory (BARs) bound (master abort)	0
[1]	PERR	Parity error	0
[31:2]	–	Reserved	–

AUDIO DMA

PCI START ADDRESS REGISTER 0 (PSA0)

.

LDCR_PSA0 register (Local audio DMA Control Register)

Name	Address	Description	Type	Reset value
LDCR_PSA0	BAR0+100h	Audio DMA Control Register 0	R/W	0

Bits	Name	Description	Reset value
[31:0]	PSA0	Start address of PCI memory for PCM	0

PCI START ADDRESS REGISTER 1 (PSA1)

.

LDCR_PSA1 register (Local audio DMA Control Register)

Name	Address	Description	Type	Reset value
LDCR_PSA1	BAR0+104h	Audio DMA Control Register 1	R/W	0

Bits	Name	Description	Reset value
[31:0]	PSA1	Start address of PCI memory for stream	0

DATA SIZE REGISTER 0(DSA0)

.

LDCR_DSA0 register (Local audio DMA Control Register)

Name	Address	Description	Type	Reset value
LDCR_TWC0	BAR0+108h	Audio DMA Control Register 0	R/W	0

Bits	Name	Description	Reset value
[15:0]	TWC0	Word (32bits) data size for PCM	0
[31:16]	–	Reserved	–

DATA SIZE REGISTER 1(DSA1)

.

LDCR_DSA1 register (Local audio DMA Control Register)

Name	Address	Description	Type	Reset value
LDCR_TWC1	BAR0+10ch	Audio DMA Control Register 1	R/W	0

Bits	Name	Description	Reset value
[15:0]	TWC1	Word (32bits) data size for stream	0
[31:16]	–	Reserved	–

AUXILIARY CONTROL REGISTER (AxC)

.

LDCR_AxC register (Local audio DMA Control Register)

Name	Address	Description	Type	Reset value
LDCR_AxC	BAR0+110h	Audio DMA auxiliary Control Register	R/W	0

Bits	Name	Description	Reset value
[7:0]	MIN_BS_P	Minimum block size for PCM (for **wcount**: default=8)	0
[15:8]	MIN_BS_S	Minimum block size for stream	0
[16]	START_DMA_P	Start DMA for PCM	0
[17]	START_DMA_S	Start DMA for stream	0
[31:18]	–	Reserved	–

TRANSFERRED DATA SIZE REGISTER 0(XWC0)

.

LDCR_XWC0 register (Local audio DMA Control Register)

Name	Address	Description	Type	Reset value
LDCR_XWC0	BAR0+114h	Transferred Data Size for PCM	R	0

Bits	Name	Description	Reset value
[15:0]	XWC0	Transferred word count register for the PCM. The transferred data size is accumulated by the H/W whenever the DMA transfers a unit size, until the total DMA transfer size has been transferred. The S/W can only read this register.	0
[31:16]	–	Reserved	–

TRANSFERRED DATA SIZE REGISTER 1(XWC1)

.

LDCR_XWC1 register (Local audio DMA Control Register)

Name	Address	Description	Type	Reset value
LDCR_XWC1	BAR0+118h	Transferred Data Size for stream	R	0

Bits	Name	Description	Reset value
[15:0]	XWC1	Transferred word count register for streaming. The transferred data size is accumulated by the H/W whenever the DMA transfers a unit size, until the total DMA transfer size has been transferred. The S/W can only read this register.	0
[31:16]	–	Reserved	–

ERROR STATUS REGISTER (ESR)

.

LDCR_ESR register (Local audio DMA Control Register)

Name	Address	Description	Type	Reset value
LDCR_ESR	BAR0+11ch	Error Status Register	R	0

Bits	Name	Description	Reset value
[0]	host1_fatal	host1_fatal for PCM	0
[1]	host1_perr	host1_perr for PCM	0
[31:2]	–	Reserved	–

HSMB DMA

PCI START ADDRESS REGISTER (PSA)

.

LHCR_PSA register (Local HSMB Control Register)

Name	Address	Description	Type	Reset value
LHCR_PSA	BAR0+140h	PCI Start Address	R/W	0

Bits	Name	Description	Reset value
[31:0]	PSA	Start address in PCI memory	0

LOCAL START ADDRESS REGISTER (LSA)

.

LHCR _LSA register (Local HSMB Control Register)

Name	Address	Description	Type	Reset value
LHCR_LSA	BAR0+144h	Local Start Address	R/W	0

Bits	Name	Description	Reset value
[15:0]	LSA	Local start address in HSMB	0
[31:16]	–	Reserved	–

TRANSFER BYTE COUNT REGISTER (TBC)

.

LHCR_TBC register (Local HSMB Control Register)

Name	Address	Description	Type	Reset value
LHCR_TBC	BAR0+148h	Transfer Byte-Count	R/W	0

Bits	Name	Description	Reset value
[1:0]	–	Always 00, read only	0
[22:2]	TDC	Transfer data (8bits)-count	0
[31:23]	–	Reserved	–

AUXILIARY CONTROL REGISTER (AxC)

.

LHCR_AxC register (Local HSMB Control Register)

Name	Address	Description	Type	Reset value
LHCR_AxC	BAR0+14ch	Auxiliary Control	R/W	0

Bits	Name	Description	Reset value
[7:0]	–	Reserved	–
[8]	START_DMA	0 = no effect 1 = start DMA when write "1" and be cleared by H/W	0
[31:9]	–	Reserved	–

TRANSFERRED DATA SIZE REGISTER (XBC)

.

LHCR_XBC register (Local HSMB Control Register)

Name	Address	Description	Type	Reset value
LHCR_XBC	BAR0+150h	Transferred Byte-Count	R	0

Bits	Name	Description	Reset value
[22:0]	XBC	Transferred byte-count	0
[31:23]	–	Reserved	–

ERROR STATUS REGISTER (ESR)

.

LHCR_ESR register (Local HSMB Control Register)

Name	Address	Description	Type	Reset value
LHCR_ESR	BAR0+154h	Error Status	R	0

Bits	Name	Description	Reset value
[0]	FATAL	Access out of memory (BARs) bound (master abort)	0
[1]	PERR	Parity error	0
[31:2]	–	Reserved	–

VIDEO DMA

PCI HEAD ADDRESS REGISTER (PSA)

.

LVCR_PHA register (Local VIDEO Control Register)

Name	Address	Description	Type	Reset value
LVCR_PHA	BAR0+160h	PCI Head Address	R/W	0

Bits	Name	Description	Reset value
[31:0]	PHA	Target start address in PCI memory	0

CIRCULAR QUEUE SIZE REGISTER (CQS)

.

LVCR _CQS register (Local VIDEO Control Register)

Name	Address	Description	Type	Reset value
LVCR_CQS	BAR0+164h	Circular Queue Size	R/W	0

Bits	Name	Description	Reset value
[31:0]	CQS	Circular queue size for PCI tail address	0

AUXILIARY CONTROL REGISTER (AxC)

.

LVCR_AxC register (Local VIDEO Control Register)

Name	Address	Description	Type	Reset value
LVCR_AxC	BAR0+168h	Auxiliary Control	R/W	0

Bits	Name	Description	Reset value
[0]	CC_IND	Channel change indicator	–
[7:1]	–	Reserved	–
[8]	START_DMA	0 = no effect 1 = start DMA when write "1" and be cleared by H/W	0
[31:9]	–	Reserved	–

WRITE POINT ADDRESS REGISTER (WPA)

.

LVCR_XBC register (Local VIDEO Control Register)

Name	Address	Description	Type	Reset value
LVCR_WPA	BAR0+16ch	Write Pointer Address	R	0

Bits	Name	Description	Reset value
[31:0]	WPA	Write pointer address	0

TRANSFERRED DATA SIZE REGISTER (XBC)

.

LVCR_XBC register (Local VIDEO Control Register)

Name	Address	Description	Type	Reset value
LVCR_XBC	BAR0+170h	Transferred Byte-Count	R	0

Bits	Name	Description	Reset value
[31:0]	XBC	Transferred byte-count	0

ERROR STATUS REGISTER (ESR)

.

LHCR_ESR register (Local HSMB Control Register)

Name	Address	Description	Type	Reset value
LVCR_ESR	BAR0+174h	Error Status	R	0

Bits	Name	Description	Reset value
[0]	FATAL	Access out of memory (BARs) bound (master abort)	0
[1]	PERR	Parity error	0
[31:2]	–	Reserved	–

PCI HEADER FIFO REGISTERS (REGn)

.

VFRM_REG register 0 ~ VFRM_REG register 15 (PCI Header FIFO register)

Name	Address	Description	Type	Reset value
VFRM_REGn	BAR0+180h + 4*(n)	Header Register_n	R	0

NOTE: n = 0 ~ 15

Bits	Name	Description	Reset value
[18:0]	VFRM_REGn	Local Video header FIFO value	0
[31:19]	–	Reserved	–

PCI WRITE POINTER FOR HEADER REGISTER (WPTR)

.

HDR_WPTR register (PCI Write Pointer for Header register)

Name	Address	Description	Type	Reset value
HDR_WPTR	BA R0+1c0h	Write Pointer for Header	R	0

Bits	Name	Description	Reset value
[3:0]	HDR_WPTR	Write Pointer for Header	0
[31:4]	–	Reserved	–

NOTE

5 MPEG VIDEO DECODER

OVERVIEW

The video packet data that passes through the TS demux are buffered by the DPSRAM and saved to the external SDRAM via DMA1. Then, that data is transferred to the MPEG video decoder via DMA3. This SDRAM area is called the video stream buffer or the CVD (compressed video data) buffer. The MPEG video decoder consists of two large parts, a syntax processor (henceforth, SP) and a video processor (henceforth, VP). The SP parses the transferred MPEG video data into the necessary format and the VP decodes that parsed data. Then, the decoded data is saved again to the external SDRAM.

The MPEG video decoder supports decoding for MPEG-1, MPEG-2, DSS MPEG-1, and DSS MPEG-2, and also supports all ATSC video formats, DSS SD, and HD video format.

Architecture

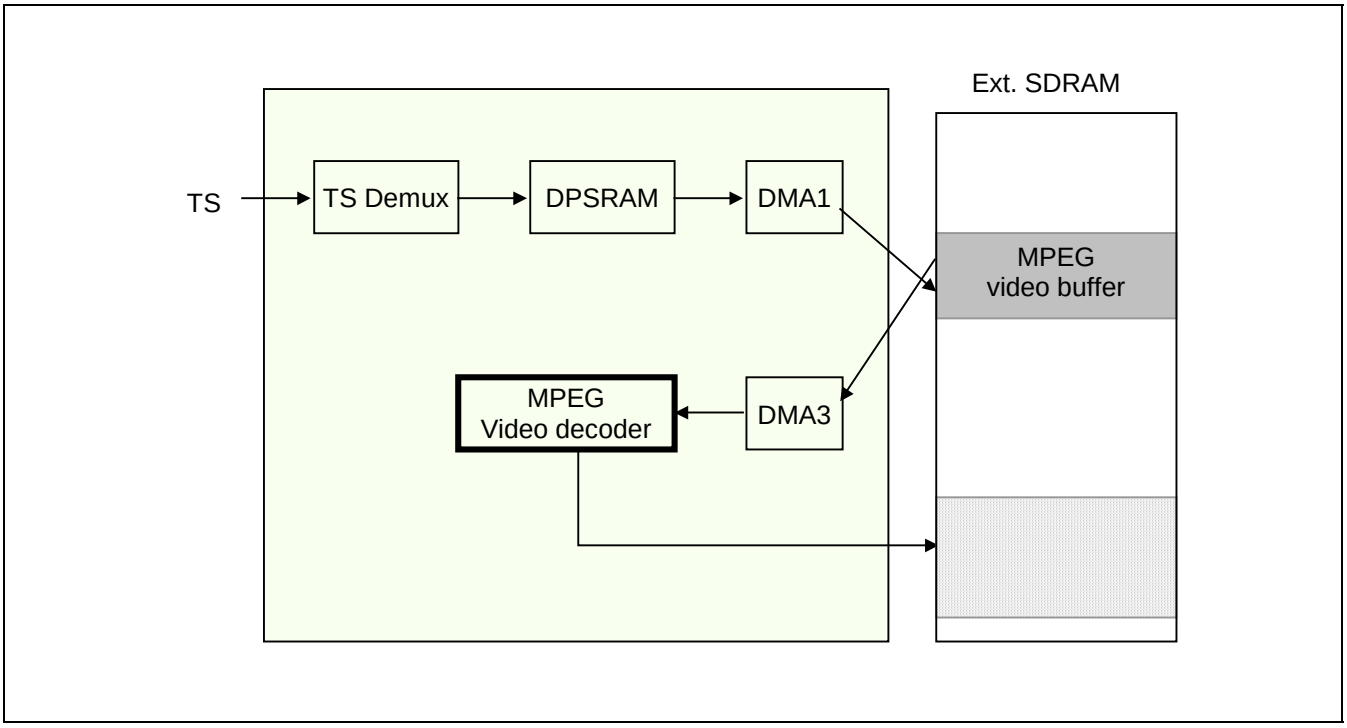

Figure 5-1 Video data flow block diagram

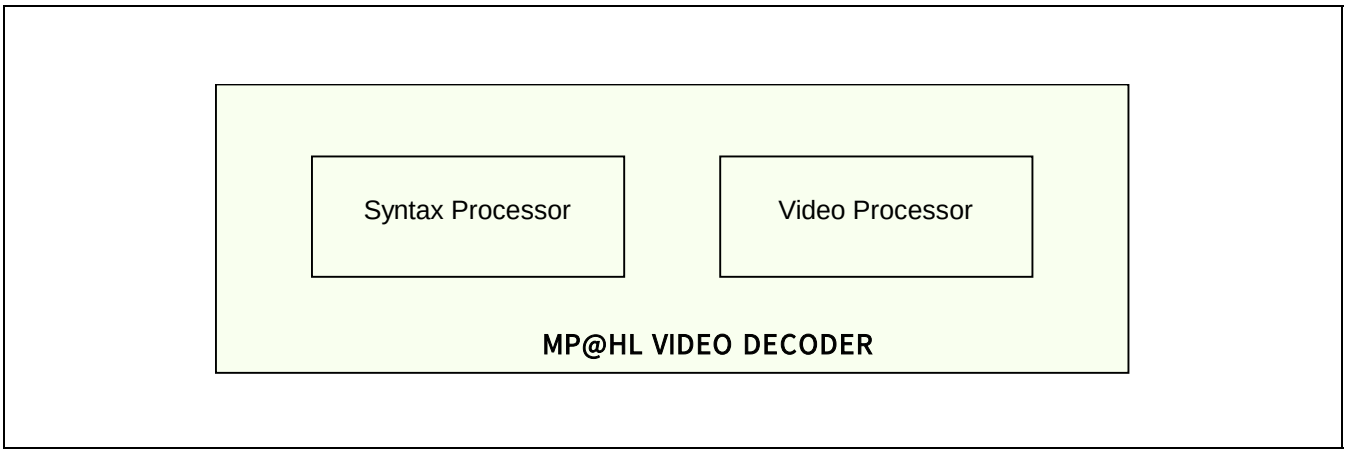

Figure 5-2 MPEG video decoder block diagram

SYNTAX PROCESSOR (SP)

The SP performs three main operations.

First, it decodes compressed video bit streams, extracting the header information, the motion vector, the zero run-length, the DC count, and the AC count and then it transfers that information to the ARM7 system, the CPU and the VP.

Second, it controls the timing operations of the video decoder and the display processor (henceforth, DP) with operation control information such as: 3:2 full-down, frame/field control, and decoding/display timing control (which are transferred on bit stream in accordance with MPEG video specifications).

Third, it performs services for the control commands such as: skip/repeat frame, header scanning, and blocking which have been transferred from the system CPU.

CVD (Compressed Video Data) BUFFER START ADDRESS REGISTER

This register sets the start address offset for the CVD buffer in the memory. The address is a (128-bit) word address and should be a location within the 32 MB address space.

CVDBUF_ST

Name	Address	Description	Type	Reset value
CVDBUF_ST	BAR0+d00h	CVD Buffer Start Address	R/W	0

Bits	Name	Description	Reset value
[20:0]	CVDBUF_START	CVD Buffer Start Address	0
[31:21]	–	Reserved	–

CVD (Compressed Video Data) BUFFER SIZE REGISTER

This register sets the CVD buffer size. It supports up to 18 bits, but because the MSB is needed to present a maximum of 2 MB of data, the maximum value should be limited to 2 MB to ensure normal operation of the VDMA.

CVDBUF_SZ

Name	Address	Description	Type	Reset value
CVDBUF_SZ	BAR0+d04h	CVD Buffer Size	R/W	0

Bits	Name	Description	Reset value
[17:0]	CVDBUF_SIZE		0
[31:18]	–	Reserved	–

CVD CONTROL AND STATUS REGISTER

This register controls some operations of the MPEG video decoder and indicates its status.

CVDBUF_STATUS

Name	Address	Description	Type	Reset value
CVD_STATUS	BAR0+d08h	CVD Status Register	R/W	0

Bits	Name	Description	Reset value
[0]	VDMA_EN	VDMA (= DMA3) Enable. The corresponding VDMA should also be enabled or disabled according to enabling/disabling of the video operation. Before enabling (disabling) the VDMA, ensure that the video decoding is enabled (disabled).	0
[1]	VDMA_CLEN	Set this flag when the VDMA needs to be initialized due to channel switching or other reasons. Because it is cleared automatically after the initialization of the VDMA, it needs not be reset again by the CPU	0
[2]	CVDBUF_UF	CVD buffer underflow flag	0
[3]	EX_WPF	Excessive Write Pointer Flag. This flag is set when the write pointer is out of range on the CVD buffer due to an error of the host CPU S/W or ARM firmware. The corresponding interrupt can be generated by using the interrupt mask flag.	0
[4]	UIM	Underflow interrupt mask	0
[5]	EX_WPIM	Excessive write pointer interrupt mask	0
[31:6]	–	Reserved	–

CVD BUFFER WRITE POINTER REGISTER

The ARM parses the TS packet and then writes the result to the CVD buffer. It also writes the write pointer to this register. Because TS data is made of byte units, the address to write is a 25-bit byte address. The ARM is responsible for the wrap-around of the write pointer on the CVD buffer (which is a circular buffer).

CVDBUF_WRPTR

Name	Address	Description	Type	Reset value
CVD_WRPTR	BAR0+d0ch	CVD Buffer Write Pointer	R/W	0

Bits	Name	Description	Reset value
[24:0]	CVD_WRPTR	CVD Buffer Write Pointer	0
[31:25]	–	Reserved	–

CVD BUFFER READ POINTER REGISTER

This register indicates the location from which the SP starts to read the bit stream. The VDMA checks the underflow using both this register and the write pointer written by ARM7. It is a 21-bit word address.

CVDBUF_WRPTR

Name	Address	Description	Type	Reset value
CVD_RDPTR	BAR0+d10h	CVD Buffer Read Pointer	R	0

Bits	Name	Description	Reset value
[20:0]	CVD_ RDPTR	CVD Buffer Read Pointer	0
[31:21]	–	Reserved	–

SP CONTROL REGISTER 0

The host CPU controls the SP through this control register.

SP_CTRL0

Name	Address	Description	Type	Reset value
SP_CTRL0	BAR0+d80h	SP Control Register 0	R/W	0

Bits	Name	Description	Reset value
[0]	DISCARD_UD	Discard User Data Discards the user data without transferring it to the CPU.	0
[1]	BLOCK_PIC	Block Picture Blocks decoding for the picture header. Video decoding is stopped until this field is reset by the CPU.	0
[2]	BLOCK_GOP	Block GOP Blocks decoding for the GOP header. Video decoding is stopped until this field is reset by the CPU.	0
[3]	BLOCK_SQ	Block Sequence Blocks decoding for the sequence header. Video decoding is stopped until this field is reset by the CPU.	0
[4]	SCAN_IP	Scan I Picture Scans the I picture header and starts decoding from the I picture found. Upper level headers of the picture that can appear during scanning are decoded. The SP generates a start picture signal for the picture header and this flag is reset automatically.	0
[5]	SCAN_GOPH	Scan GOP Header Scans the GOP header and starts decoding from the new GOP found. Upper level headers of the GOP that can appear during scanning are decoded. The SP generates a start GOP signal for the GOP header and this flag is reset automatically.	0
[6]	SCAN_SQH	Scan Sequence Header Scans the sequence header and starts decoding from the new sequence found. The SP generates a start sequence signal for the sequence header and this flag is reset automatically.	0

[7]	REPEAT_F	Repeat_Frame Slows down the decoding speed by stopping the decoding for a time interval of 1 frame. Because this flag is reset automatically when the SP sets repeat acknowledgment during command execution command, it need not be reset by the CPU.	0

SP CONTROL REGISTER 0 (Continued)

Bits	Name	Description	Reset value
[8]	SKIP_F	Skip Frame Speeds up the decoding speed by discarding the bit stream of 1 frame. Because this flag is reset automatically when the SP sets skips acknowledgment during command execution, it need not be reset by the CPU.	0
[9]	D_PAUSE	Decoding Pause Used to stop the video decoding temporarily. Different from the repeat frame, this flag has the advantage that the decoding is stopped until it is reset by the CPU.	0
[10]	D_EN	Video Enable Enables video decoding. When the video is enabled and operated normally, the video enabled flag for the VIDEO_STAT_n register is set. The CPU must check whether the video is enabled normally by checking the VIDEO_STAT_n register after enabling the video.	0
[31:11]	–	Reserved	–

SP CONTROL REGISTER 1

The host CPU controls the SP through this control register.

SP_CTRL1

Name	Address	Description	Type	Reset value
SP_CTRL1	BAR0+d90h	SP Control Register 1	R/W	0

Bits	Name	Description	Reset value
[0]	DBLBUFF_BP	Double Buffer for B Picture While implementing SAM2K_LITE features, you may encounter a situation where the screen is non-functioning due to the difference between the decoding and the display speeds for the B picture which uses only 1 frame buffer. This problem can be solved by using this flag. When enabled, this flag generates two display pointers on the basis of two frame buffers for the B picture. In this case, DP and MMU should use two display pointers accordingly.	0
[1]	DSS_VF	DSS Video Flag This flag should be enabled for DSS video decoding so that the video control parameters transferred on user data are processed by the video decoder.	0
[2]	FREEZE_EN	Freeze Enable Fixes the display pointer to transfer to the DP and continues decoding. The situation is maintained until this flag is reset by the CPU.	0
[3]	UDMC_EN	Uni-Directional Motion Compensation Enable Enables the function that allows motion compensation to be performed using only the forward motion vector when the macro block of the B picture has a bi-directional motion vector.	0
[11:4]	DS_END_ADD	Decoding Slice End Address Sets the end slice address of the decoding range in slice selective decoding.	0
[19:12]	DS_START_ADD	Decoding Slice Begin Address Sets the start slice address of the decoding range in slice selective decoding.	0
[20]	SSD_END	Slice Selective Decoding Enable Enables the function that decodes only a portion of the slice range for the B picture.	0

SP CONTROL REGISTER 1 (Continued)

Bits	Name	Description	Reset value
[22:21]	DECODE_MODE	Decoding mode 0 = Normal decoding 1 = I/P pictures only 2 = I picture only	0
[23]	VP_TOI_EN	VP Time Out Interrupt Enable Enables the VP time out interrupt that notifies the CPU when the VP is stopped for more than a specific cycle.	0
[31:24]	–	Reserved	–

SP STATUS REGISTER

The host CPU can get SP status information through this register.

SP_STATUS

Name	Address	Description	Type	Reset value
SP_STATUS	BAR0+d94h	SP Status Register	R/W	0

Bits	Name	Description	Reset value
[0]	SP_EIM	SP Error Interrupt Mask When set to 1, an interrupt is generated to the CPU at the SP error.	0
[1]	START_PIM	Start Picture Interrupt Mask When set to 1, an interrupt is generated to the CPU at the picture start.	0
[2]	START_GOPIM	Start GOP Interrupt Mask When set to 1, an interrupt is generated to the CPU at the GOP start.	0
[3]	START_SIM	Start Sequence Interrupt Mask When set to 1, an interrupt is generated to the CPU at the sequence start.	0
[4]	REPEAT_AIM	Repeat Ack Interrupt Mask When set to 1, an interrupt is generated to the CPU at the repeat acknowledgment.	0
[5]	SKIP_AIM	Skip Ack Interrupt Mask When set to 1, an interrupt is generated to the CPU at the skip acknowledgment.	0
[6]	DECODE_SIM	Decoding Sync Interrupt Mask When set to 1, an interrupt is generated to the CPU at the decoding sync.	0
[7]	PLE_F	Picture Level Error Flag Indicates an SP error occurred within the macroblock or in its upper level header. If the SP error has occurred in a upper level header, the SP discards all slices and starts decoding from the next higher header. If the SP error has occurred within the macroblock, or a VP error occurs, the SP starts decoding again from the next header including the slice header.	0

SP STATUS REGISTER (Continued)

Bits	Name	Description	Reset value
[8]	SP_ERROR	SP Error Sets to 1 when a VLD error or a VP error occurs. This flag is reset when the CPU writes 1 again.	0
[9]	START_P	Start Picture Sets to 1 when the SP starts decoding the picture start header. This flag is reset when the CPU writes 1 again.	0
[10]	START_GOP	Start GOP Sets to 1 when the SP starts decoding the GOP start header. This flag is reset when the CPU writes 1 again.	0
[11]	START_SQ	Start Sequence Sets to 1 when the SP starts decoding the sequence start header. This flag is reset when the CPU writes 1 again.	0
[12]	REPEAT_ACK	Repeat Ack Sets to 1 when the CPU writes the frame repeat command to the video control register and the SP starts the command. This flag is reset when the CPU writes 1 again.	0
[13]	SKIP_ACK	Skip Ack Sets to 1 when the CPU writes the frame skip command to the video control register and the SP starts the command. This flag is reset when the CPU writes 1 again.	0
[14]	DECODE_SNC	Decoding Sync Sets to 1 when SP starts slice decoding. This flag is reset when the CPU writes 1 again.	0
[16:15]	DISPLY_PNT	Display Pointer The display pointer to transfer to the DP. It is also referenced by the CPU. 0 and 1 are used by the reference frame buffer. 2 and 3 are used by the B frame buffer. If two B frame buffers are used, both 2 and 3 are used. If one frame buffer is used, only 2 is used.	0
[17]	MPEG2_F	MPEG2 Flag Indicates whether the current input video stream is MPEG1 or MPEG2. When set to 1, it means an MPEG2 stream.	0

[18]	VEN_ACK	Video Enable Acknowledge The video enable flag set with the video control register is not sent directly to the video decoder and is only sent when the video process is not being decoded. If the video process which is being decoded is enabled or disabled, the change is transferred to this flag when the decoding finishes. Hence, when the CPU has enabled or disabled video, it should enable or disable the VDMA after checking whether the operation is reflected by this flag.	0
[20:19]	DP_TYPE	Decoding Picture Type 0 = I-picture, 1 = P-picture, 2 = B-picture	0
[31:19]	–	Reserved	–

SP DECIMATION REGISTER

The host CPU controls the SP decimation through this register.

SP_DECM

Name	Address	Description	Type	Reset value
SP_DECM	BAR0+da4h	Decimation Register	R/W	0

Bits	Name	Description	Reset value
[11:0]	–	Reserved	–
[12]	DECIMATION	Decimation decoding 0 = decimation decoding off 1 = decimation decoding on	0
[13]	CF_BUF	Circular/Fixe buffer 0 = fixed buffer 1 = circular buffer	0
[31:19]	–	Reserved	–

VP STATUS REGISTER

The host CPU checks the VP status through this register.

VP_STATUS

Name	Address	Description	Type	Reset value
VP_STATUS	BAR0+da8h	VP Status Register	R	0

Bits	Name	Description	Reset value
[0]	VP_ERROR	VP error	0
[1]	HM_ERROR	0 = Header error 1 = MB error	0
[7:2]	IQ_STATUS	IQ block의 state	0
[12:8]	IDCT_STATUS	IDCT block의 state	0
[31:13]	–	Reserved	–

VP TIME OUT REGISTER

This register is a kind of watch dog timer and safeguards the VP operation against time-out.

VP_TIMER

Name	Address	Description	Type	Reset value
VP_TIMER	BAR0+dach	VP Timer Register	R/W	0

Bits	Name	Description	Reset value
[29:0]	VP_TO_CNT	VP Time Out Counter Sets the VP time-out cycle.	
[30]	VP_TOI	VP Time-Out Interrupt This flag is set when the VP is stopped for more than the time interval specified in VP_TO_CNT. It is reset when the VP timer is disabled with the SP control register.	
[31]	VP_TOIM	VP Time-Out Interrupt Mask When this flag is set, VP time-out interrupt is enabled.	

NOTE

6 DISPLAY PROCESSOR

6.1 OVERVIEW

The Display Processor (henceforth, DP) converts MPEG decoded video and HD and SD video input from an external source in accordance with the output video format and generates the display video that is displayed on display device. Therefore, the DP consists of an Input part that processes the external input and the decoded MPEG input, a Converter part (FC0, FC1) that converts the format of the video saved in the memory into the display format, an Output part that generates the converted video in accordance with the display environment, and a Control part that supports the signals and values for their operation and control.

6.2 Input Part

The input video that the DP processes is largely divided into external video (which is input from the external input port) and the MPEG video (which is decoded by the video processor) (henceforth, VP). The DP has two types of external video input ports to support various PIP formats. An HD video input port is provided to support the DTV ready function. An SD video input port is provided to receive SD video broadcasted in an analog signal. In the Input part, the HD/SD input video is saved to an external memory, in real time, by the HD/SD Input I/F Module. The DP processes all types of output video generated by the VP. However, for MPEG video, it differs from the external input in that the memory write operation does not occur in the Input part because a pointer to the memory space is transferred from the Syntax Processor (henceforth, SP). Table 6-1 shows the input types that are supported by the DP and their characteristics.

Table 6-1 Input Types Supported by the DP

Input	Format	Frame rate	Color (data) format	Description
SD0 SD1	720x480 i	59.94	CCIR656 / CCIR656like	- Uses the external sync and the clock - Saves to memory in 4:2:2 format.
	720x576 i	50	CCIR656 / CCIR656like	
HD (DTV)	1920x1080 i	59.94/60	RGB (4:4:4) YCbCr (4:4:4, 4:2:2)	- Uses the external sync and the clock - Supports the CCIR656 format - For unsupported VGA input formats, a dedicated external chip should be used. - Horizontal 1/2 decimation - Saves to memory in 4:2:2 format.
	1280x720 P	59.94/60	RGB (4:4:4) YCbCr (4:4:4, 4:2:2)	
	720x480 P	59.94	RGB (4:4:4) YCbCr (4:4:4, 4:2:2)	
HD (VGA)	XGA (60~90 Hz) 1024x768P	60~72	RGB (4:4:4)	
	SVGA (56~90 Hz) 800x600P	60~72	RGB (4:4:4)	
	VGA (60~90 Hz) 640x480P	60~72	RGB (4:4:4)	
	640x352P	60~72	RGB (4:4:4)	
MPEG	Supports ATSC 18 format. (See Table 6-2)			

Table 6-2 ATSC 18 FORMATS

Resolution (Width x Height)	Aspect Ratio	Screen Count per Second/Scanning Method				Screen Quality
		60 Screens Twofold Scanning	60 Screens Interlaced Scanning	30 Screens Twofold Scanning	24 Screens Twofold Scanning	
1920 x 1080	16:9	X	O	O	O	HD
1280 x 720	16:9	O	X	O	O	HD
704 x 480	16:9	O	O	O	O	SD
704 x 480	4:3	O	O	O	O	SD
640 x 480	4:3	O	O	O	O	SD
Format count		4	4	5	5	18

6.3 Format Convert Part(FC0, FC1)

The Format Converter part consisting of the FC0 and FC1 modules, converts the format of the video saved in the external memory in accordance with various display features such as PIP support, and transfers it to the Graphic Processor (henceforth, GP) using Disp_Mux_Ctrl. It also receives OSG (On-Screen Graphic) data from the GP as overlay HD video and outputs it to the Output part. On the basis of this data flow, the Format Converter part provides various display features. The following table summarizes the features supported by the Format Converter part.

Table 6-3 Format-converting features

Feature	Description
Letter box / pan-scan display	- Supports letter-box and pan-scan display when a 16:9 format video source is displayed in the 4:3 display mode.
Pillar-box (side-wall) / panorama display	- Supports pillar-box and panorama display when a 4:3 format video source is displayed in the 16:9 display mode. - For panorama display, 2nd order scaling is supported. Linear-scaling and non-linear scaling areas are selected dynamically.
PIP support	- Supports various formats of PIP features for all video.
Flexible video scaling	- Main picture scaling ratio (FC0): Horizontal: 16 ~ 1/4 Vertical: 256 ~ 1/4 - Sub picture scaling ratio (FC1): Horizontal: 4 ~ 1/4 Vertical: 256 ~ 1/4
Poly-phase filtering for horizontal scaling	- Supports 8-tab/16-phase poly-phase filters to provide more enhanced screen quality for the main picture.
Anti-aliasing filter for horizontal scaling	- Enhances video quality by applying an anti-aliasing filter to the 7-tab if the sub-sampling rate is high when implementing PIP features.
3-D IPC for 480I video	- Interlace to progressive conversion using motion detection and directional 2-D filtering.
Flexible color space conversion	- Supports various color space converters to match the color space of all DTV video sources and external HD video input.

Architecture

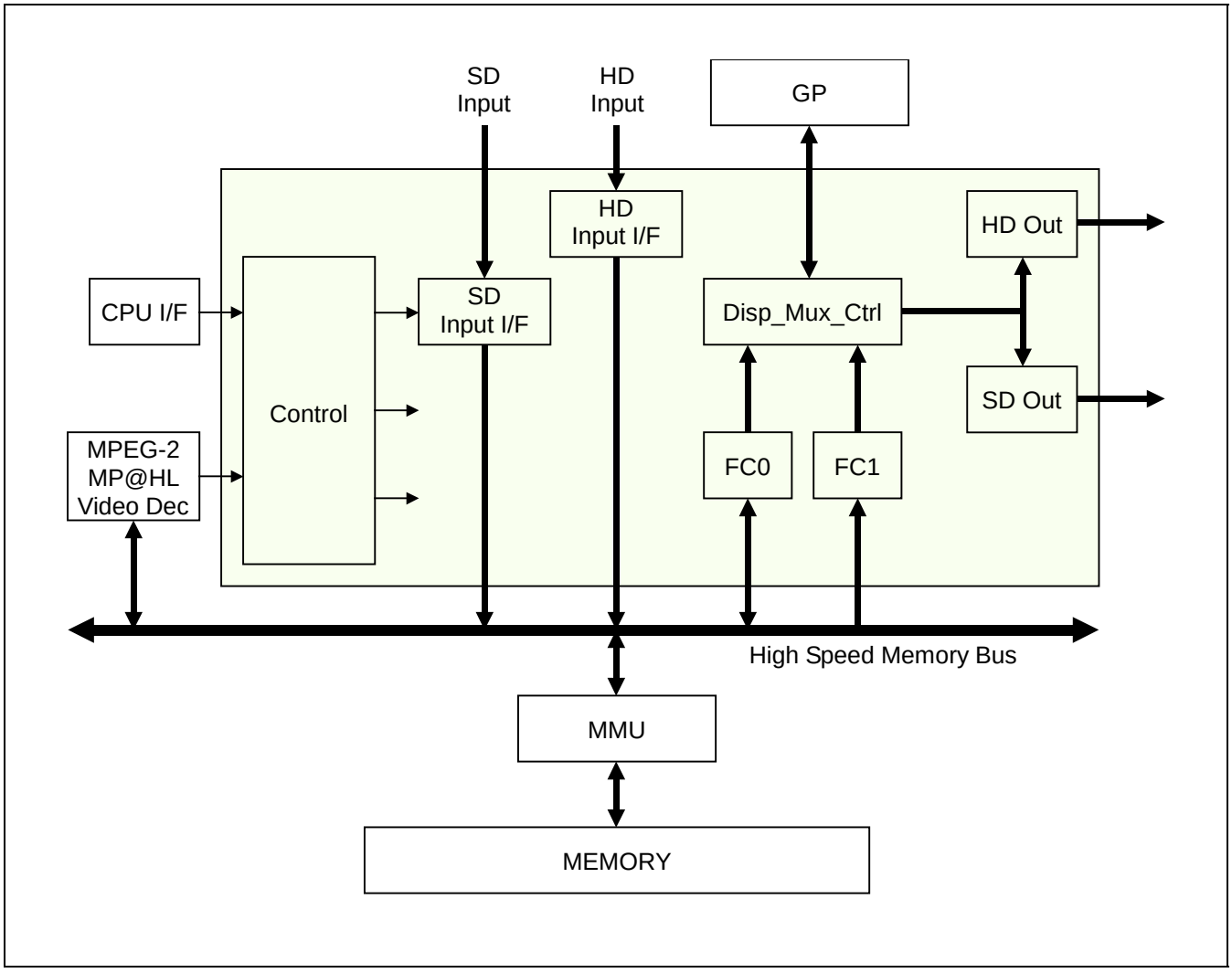

Figure 6-1 Display Processor block diagram

DISPLAY CONTROL REGISTERS: DP_REG_0, DP_REG_1, DP_REG_2, DP_REG_3, DP_REG_4

Display control registers set: video on, video off, display mode, and display size settings.

DP_REG_0

Name	Address	Description	Type	Reset value
DP_REG_0	BAR0+800h	Sync on	R/W	0

Bits	Name	Description	Reset value
[0]	SYNC_ON	0 = sync generation disable 1 = sync generation enable This bit enables/disables the DP operation. If the sync generation is disabled, all video is off on the DP, and the screen is recognized as an H/V blank interval and the blank color (changes green to black on Rev) is output. The ground plane, video plane, OSD plane, and cursor plane are also off.	0
[31:1]	–	Reserved	–

DP_REG_1

Name	Address	Description	Type	Reset value
DP_REG_1	BAR0+804h	Source on / off	R/W	0

Bits	Name	Description	Reset value
[0]	MAIN_ON	Video Mute Enable 0 = video mute enable (video off) 1 = video mute disable (video on) This bit enables/disables only the video output. The purpose of video mute is not only to turn off the video plane but also to operate the OSD and cursor plane. For S5H2000X, all planes are turned off and the following operations are also performed: sync off and DP_REG_0[0]=0.	0
[1]	SD0_ON	External SD Operation Enable 0 = external SD (SD0) operation disable 1 = external SD (SD0) operation enable SD1, is controlled with DP_REG90[1].	0
[2]	HD_ON	External HD operation enable 0 = external HD operation disable 1 = external HD operation enable	0
[4:3]	–	Reserved	–
[5]	MAIN_MUX_ON	Main picture display on/off 0 = main picture display off 1 = main picture display on	0
[6]	SUB_MUX_ON	Sub picture display on/off 0 = sub picture display off 1 = sub picture display on	0
[31:7]	–	Reserved	–

DP_REG_1[6] determines whether the sub picture display is on/off. The following table shows the comparison between DP_REG_1[6] and DP_REG_2[2].

	DP_REG_1[6]=0	DP_REG_1[6]=1
DP_REG_2[2]=0	DP_REG_2[2] turns the sub picture off.	DP_REG_2[2] turns the sub picture off.
DP_REG_2[2]=1	DP_REG_2[2] turns the sub picture on, but, DP_REG_1[6] turns the sub picture display off. The main picture is not displayed in the sub picture area and the sub picture area remains. But, since the sub picture display is off, the sub picture screen will be filled with the previous sub picture or unknown data.	DP_REG_2[2] turns the sub picture on and DP_REG_1[6] turns the sub picture display on, so, the sub picture operates normally.

DISPLAY MODE CONTROL REGISTER

Description

DP_REG_2

Name	Address	Description	Type	Reset value
DP_REG_2	BAR0+808h	Display mode	R/W	0

Bits	Name	Description	Reset value
[0]	MAIN_DISP_MODE	Main picture display mode 0 = normal operation mode 1 = IPC operation mode	0
[1]	–	Reserved	–
[2]	SUB_DISP_MODE	Sub picture display mode 0 = sub picture off 1 = sub picture on (normal PIP)	0
[5:4]	MAIN_SOURCE	Main picture source 0 = MPEG 1 = external HD or external SD1 2 = external SD0 3 = prohibited	0
[7:6]	SUB_SOURCE	Sub picture source 0 = MPEG 1 = external HD or external SD1 2 = external SD0 3 = prohibited	0
[8]	MPEG_PROG	Progressive MPEG Video 0 = When MPEG video is non progressive. 1 = When MPEG video is progressive.	0
[19:9]	–	Reserved	–
[20]	3D_IPC_OFF	0 = 3D_IPC on 1 = 3D_IPC off (2D IPC on)	0
[31:1]	–	Reserved	–

DISPLAY SIZE CONTROL REGISTER

Description

DP_REG_3

Name	Address	Description	Type	Reset value
DP_REG_3	BAR0+80ch	Display size	R/W	0

Bits	Name	Description	Reset value
[0]	DISP_PROG	0 = display with interlace 1 = display with progressive	0
[12:1]	DISP_SIZE_H	Display horizontal size (2200, 1650, 858 pixels)	0
[23:13]	DISP_SIZE_V	Display vertical size (1125, 750, 525 lines)	0
[31:24]	–	Reserved	–

HD OUTPUT H SYNC CONTROL REGISTER

Description

DP_REG_4

Name	Address	Description	Type	Reset value
DP_REG_4	BAR0+810h	HD output H sync location / rate	R/W	0

Bits	Name	Description	Reset value
[8:0]	DISP_HSYNC_POS	Horizontal H sync position	
[10:9]	DISP_4X	Display rate 0 = normal 1 = x 2 2 = x 4 3 = prohibited	
[31:11]	–	Reserved	–

HD OUTPUT H ACTIVE CONTROL REGISTER

Description

DP_REG_5

Name	Address	Description	Type	Reset value
DP_REG_5	BAR0+814h	HD output H active	R/W	0

Bits	Name	Description	Reset value
[8:0]	DISP_START_H	Display active horizontal start	0
[20:9]	DISP_END_H	Display active horizontal end (DISP_END_H - DISP_START_H = 1920, 1280, 720)	0
[31:21]	–	Reserved	–

HD OUTPUT V ACTIVE CONTROL REGISTER

Description

DP_REG_6

Name	Address	Description	Type	Reset value
DP_REG_6	BAR0+818h	HD output v active	R/W	0

Bits	Name	Description	Reset value
[6:0]	DISP_START_V	Display active vertical start	0
[16:7]	DISP_END_V	Display active vertical end (DISP_END_V - DISP_START_V = 720, 540, 480)	0
[31:17]	–	Reserved	–

HD OUTPUT 656 V ACTIVE CONTROL REGISTER

Description

DP_REG_7

Name	Address	Description	Type	Reset value
DP_REG_7	BAR0+81ch	HD output 656 v active	R/W	0

Bits	Name	Description	Reset value
[6:0]	DISP_V_START	656 display active vertical start	0
[16:7]	DISP_V_END	656 display active vertical end	0
[31:17]	–	Reserved	–

SP V SYNC START REGISTER

Description

DP_REG_8

Name	Address	Description	Type	Reset value
DP_REG_8	BAR0+820h	**SP** vsync start 0/1	R/W	0

Bits	Name	Description	Reset value
[9:0]	VSYNC_START	**DS**_VSYNC_START. Vsync start line for MPEG	0
[31:10]	–	Reserved	–

RESERVED REGISTER

Description

DP_REG_9

Name	Address	Description	Type	Reset value
DP_REG_8	BAR0+824h	Reserved	–	0

Bits	Name	Description	Reset value
[31:0]	–	Reserved	–

MAIN / SUB HORIZONTAL PROCESSING CONTROL REGISTER

Description

DP_REG_10

Name	Address	Description	Type	Reset value
DP_REG_10	BAR0+828h	Main / Sub horizontal processing start	R/W	0x0101

Bits	Name	Description	Reset value
[7:0]	MAIN_RD_POS	Main picture read initial position	0
[15:8]	SUB_RD_POS	Sub picture read initial position	0
[31:16]	–	Reserved	–

MAIN / SUB HORIZONTAL PROCESSING CONTROL REGISTER

Description

DP_REG_10

Name	Address	Description	Type	Reset value
DP_REG_10	BAR0+828h	Main / Sub horizontal processing start	R/W	0x0101

Bits	Name	Description	Reset value
[7:0]	MAIN_RD_POS	Main picture read initial position	1
[15:8]	SUB_RD_POS	Sub picture read initial position	1
[31:16]	–	Reserved	–

MAIN / SUB HORIZONTAL PROCESSING CONTROL REGISTER

Description.

DP_REG_11

Name	Address	Description	Type	Reset value
DP_REG_11	BAR0+82ch	Main video enable horizontal	R/W	0

Bits	Name	Description	Reset value
[7:0]	MAIN_RD_POS	Main picture read initial position	0
[15:8]	SUB_RD_POS	Sub picture read initial position	0
[31:16]	–	Reserved	–

MAIN / SUB HORIZONTAL PROCESSING CONTROL REGISTER

Description

DP_REG_12

Name	Address	Description	Type	Reset value
DP_REG_12	BAR0+830h	Main video enable vertical	R/W	0

Bits	Name	Description	Reset value
[9:0]	MAIN_START_V	Main picture video vertical start position	0
[19:10]	SUB_END_V	Sub picture video vertical end position	0
[31:20]	–	Reserved	–

?? CONTROL REGISTER

Description

DP_REG_13

Name	Address	Description	Type	Reset value
DP_REG_13	BAR0+834h	Main2 /PIG / IPC sync	R/W	0

Bits	Name	Description	Reset value
[8:0]	PIG_SIZE_H	Display IPC Horizontal Sync	0
[18:9]	PIG_START_V	Vertical active start of source at Main IPC	0
[28:19]	PIG_END_V	Vertical active end of source at Main IPC	0
[31:29]	–	Reserved	–

SUB VIDEO HORIZONTAL CONTROL REGISTER

Description

DP_REG_14

Name	Address	Description	Type	Reset value
DP_REG_14	BAR0+838h	Sub video enable horizontal	R/W	0

Bits	Name	Description	Reset value
[11:0]	SUB_START_H	PIG or Sub picture horizontal start	0
[23:12]	SUB_END_H	PIG or Sub picture horizontal end	0
[31:24]	–	Reserved	–

SUB VIDEO VERTICAL CONTROL REGISTER

Description

DP_REG_15

Name	Address	Description	Type	Reset value
DP_REG_15	BAR0+83ch	Sub video enable vertical 0	R/W	0

Bits	Name	Description	Reset value
[9:0]	SUB_START_H	Sub picture vertical start 0	0
[19:10]	SUB_END_H	Sub picture vertical end 0	0
[31:20]	–	Reserved	–

MAIN VIDEO HORIZONTAL DISPLAY CONTROL REGISTER

Description

DP_REG_18

Name	Address	Description	Type	Reset value
DP_REG_18	BAR0+848h	Display main video enable horizontal	R/W	0

Bits	Name	Description	Reset value
[11:0]	DISP_MAIN_START_H	Main picture display horizontal active start position	0
[23:12]	DISP_MAIN_END_H	Main picture display horizontal active end position	0
[31:24]	–	Reserved	–

MAIN VIDEO VERTICAL DISPLAY CONTROL REGISTER

Description

DP_REG_19

Name	Address	Description	Type	Reset value
DP_REG_19	BAR0+84ch	Display main video enable vertical	R/W	0

Bits	Name	Description	Reset value
[9:0]	DISP_MAIN_START_V	Main picture display vertical active start position	0
[19:10]	DISP_MAIN_END_V	Main picture display vertical active end position	0
[31:20]	–	Reserved	–

SUB VIDEO HORIZONTAL DISPLAY CONTROL REGISTER

Description

DP_REG_20

Name	Address	Description	Type	Reset value
DP_REG_20	BAR0+850h	Display sub video enable horizontal	R/W	0

Bits	Name	Description	Reset value
[11:0]	DISP_SUB_START_H	Sub picture display horizontal active start position	0
[23:12]	DISP_SUB_END_H	Sub picture display horizontal active end position	0
[31:24]	–	Reserved	–

SUB VIDEO VERTICAL DISPLAY CONTROL REGISTER

Description

DP_REG_21

Name	Address	Description	Type	Reset value
DP_REG_21	BAR0+854h	Display sub video enable vertical	R/W	0

Bits	Name	Description	Reset value
[9:0]	DISP_SUB_START_V	Sub picture display vertical active start position	0
[19:10]	DISP_SUB_END_V	Sub picture display vertical active end position	0
[31:20]	–	Reserved	–

HD SYNC CONTROL REGISTER

Description

DP_REG_22

Name	Address	Description	Type	Reset value
DP_REG_22	BAR0+858h	HD sync	R/W	0

Bits	Name	Description	Reset value
[0]	HDOUT_HSYNC_POLARITY	Hsync polarity selection for HD out 0=Hsync is HIGH active (LOW in horizontal active) 1=Hsync is LOW active (HIGH in horizontal active)	0
[1]	HDOUT_VSYNC_POLARITY	Vsync polarity selection for HD out 0=Vsync is HIGH active (LOW in vertical active) 1=Vsync is LOW active (HIGH in vertical active) Valid only if HDout_Vsync_type=0.	0
[2]	HDOUT_VSYNC_TYPE	Vsync type selection for HD out 0=Sync (Pulse) type 1=Toggle type (Field type)	0
[9:3]	HDOUT_V_SIZE	Size of vertical sync interval (7bit)	0
[21:10]	HDOUT_H_START	Horizontal sync start position (12bit=0~2047)	0
[30:22]	**HDOUT_H_END**	Horizontal sync end position **(12bit=0~2047)**	0
[31:29]	–	Reserved	–

SD SYNC CONTROL REGISTER

Description

DP_REG_23

Name	Address	Description	Type	Reset value
DP_REG_23	BAR0+85ch	SD sync	R/W	0

Bits	Name	Description	Reset value
[0]	SDOUT_MODE_0	SD output mode for last line 0 = last line fit 1 = V blank fit	0
[1]	SDOUT_MODE_1	Output type 0 = NTSC 1 = PAL	0
[2]	SDOUT_SYNC_TYPE_0	Hsync polarity selection for SD out 0 = Hsync is HIGH active (LOW in horizontal active) 1 = Hsync is LOW active (HIGH in horizontal active)	0
[3]	SDOUT_SYNC_TYPE_1	Vsync polarity selection for SD out 0 = Hsync is HIGH active (LOW in horizontal active) 1 = Hsync is LOW active (HIGH in horizontal active) SDout_sync_type_2=0 일 경우만 의미 있음(?)	0
[4]	SDOUT_SYNC_TYPE_2	Vsync type selection for SD out 0 = Sync (Pulse) type 1 = Toggle type (Field type)	0
[12:5]	SDOUT_H_START	Horizontal sync start position (8bit=0~255)	0
[20:13]	SDOUT_H_END	Horizontal sync end position (8bit=0~255)	0
[25:21]	SDOUT_V_START	Vertical sync start position (5bit=0~31)	0
[30:26]	SDOUT_V_SIZE	Size of vertical sync interval (5bit=0~31)	0
[31:29]	–	Reserved	–

EXTENAL SD SYNC CONTROL REGISTER

Description

DP_REG_24

Name	Address	Description	Type	Reset value
DP_REG_24	BAR0+860h	External SD sync	R/W	0x74

Bits	Name	Description	Reset value
[0]	SD0_SAMPLE	External SD sub sample 0 = 1:1 1 = 2:1	0
[6:1]	SD0_SYNC_TYPE	External SD sync type	111010
[7]	SD0_CCIR656	External SD 656 type	0
[11:8]	SD0_BASE_PTR	External SD base frame pointer	0
[20:12]	SD0_FLUSH_CNT	External SD FIFO flush indication	0
[21]	SD0_SYNC_ON	External SD sync detection enable 0 = External SD sync detection disable 1 = External SD sync detection enable	0
[22]	SD0_MUX_ON	SD input muxing 0 = external input 1 = test pattern	0
[31:20]	–	Reserved	–

EXTENAL SD HORIZONTAL ACTIVE CONTROL REGISTER

Description

DP_REG_25

Name	Address	Description	Type	Reset value
DP_REG_25	BAR0+864h	External SD horizontal active	R/W	0

Bits	Name	Description	Reset value
[8:0]	SD_h_start	External SD Horizontal Active Start Position (9bit=0 ~ 511)	0
[19:9]	SD_h_end	External SD Horizontal Active End Position (11bit=0~2043)	0
[31:20]	–	Reserved	–

EXTENAL SD VERTICAL ACTIVE CONTROL REGISTER

Description

DP_REG_26

Name	Address	Description	Type	Reset value
DP_REG_26	BAR0+868h	External SD vertical active	R/W	0

Bits	Name	Description	Reset value
[5:0]	SD_v_start_o	External SD vertical active start position (odd field) (6bit) ???	0
[11:6]	SD_v_start_e	External SD vertical active start position (even field) (6bit) ???	0
[20:12]	SD_v_size	External SD vertical active size(8bit)???	0
[31:21]	–	Reserved	–

EXTENAL HD SYNC CONTROL REGISTER

Description.

DP_REG_27(if external SD1 input enable, DP_REG_89[0]=0)

Name	Address	Description	Type	Reset value
DP_REG_27	BAR0+86ch	External HD sync	R/W	0

Bits	Name	Description	Reset value
[1:0]	–	Reserved	–
[3:2]	EXT_SD1_cpu_mode	External SD1 CPU Mode 00=Normal 3D-IPC 01=Normal 2D-IPC 10=2D-IPC(EOSI) 11=SD1 I/F Auto Detection	0
[8:4]	–	Reserved	–
[9]	EXT_ccir656	External SD1 input Format 0 = Not CCIR-656 Format 1 = CCIR-656 Format	0
[13:10]	EXT_base_ptr	External SD1 Base Frame Pointer (4bti=0~15) Specifies the external memory set by the MMU base register (BASE_ADDR_32~ 37). 0000 = BASE_ADDR_32[11:0] area of memory 0001 = BASE_ADDR_32[23:12] area of memory 0010 = BASE_ADDR_33[11:0] area of memory 1011 = BASE_ADDR_37[11:0] area of memory 1100 = BASE_ADDR_37[23:12] area of memory 1101 - 1111 = Not used	0
[22:14]	EXT_flush_cnt	External SD1 FIFO flush indication(9bit=0~511) ???	0
[23]	EXT_sync_on	External SD1 Sync Detection Enable 0=Disable SD1 sync detection 1=Enable SD1 sync detection Extracts/creates a sync signal from the sync decoder. For CCIR 656 format, creates a sync signal by extracting sync data from the input data.	0
[31:24]	–	Reserved	–

EXTENAL HD SYNC CONTROL REGISTER

Description.

DP_REG_27 (if external HD input enable, DP_REG_89[0]=1)

Name	Address	Description	Type	Reset value
DP_REG_27	BAR0+86ch	External HD sync	R/W	0

Bits	Name	Description	Reset value
[0]	–	Reserved	–
[1]	HD_sample	External HD subsample 0=2:1 1=Normal	0
[3:2]	EXT_color_format	External HD color format 00=YCbCr(4:4:4) 01=YCbCr(4:2:2) 10=:RGB 11=Not used	0
[7:4]	–	Reserved	–
[8]	HD_progressive	External HD input Progressive selection 0=Not progressive(=Interlaced) 0=Progressive	0
[9]	EXT_ccir656	External HD input Format 0=Not CCIR-656 Format 1=CCIR-656 Format	0
[13:10]	EXT_base_ptr	External HD Base Frame Pointer (4bti=0~15) Specifies the external memory set by the MMU base register (BASE_ADDR_32~ 37). 0000 = BASE_ADDR_32[11:0] area of memory 0001 = BASE_ADDR_32[23:12] area of memory 0010 = BASE_ADDR_33[11:0] area of memory 1011 = BASE_ADDR_37[11:0] area of memory 1100 = BASE_ADDR_37[23:12] area of memory 1101 - 1111 = Not used	0
[22:14]	EXT_flush_cnt	External HD FIFO flush indication(9bit=0~511) ???	0

DP_REG_27 (if external HD input enable,DP_REG_89[0]=1) (Continued)

Bits	Name	Description	Reset value
[23]	EXT_sync_on	External HD Sync Detection Enable 0=Disable HD sync detection 1=Enable HD sync detection Extracts/creates a sync signal from the sync decoder. For CCIR 656 format, creates a sync signal by extracting sync data from the input data.	0
[25:24]	HD_3frame_buffer	3frame buffer indicator	0
[26]	HD_mux_on	HD Input Muxing 0=External input 1=Test pattern	0
[31:27]	–	Reserved	–

EXTENAL HD HORIZONTAL ACTIVE CONTROL REGISTER

Description.

DP_REG_28

Name	Address	Description	Type	Reset value
DP_REG_28	BAR0+870h	External HD horizontal active	R/W	0

Bits	Name	Description	Reset value
[8:0]	EXT_h_start	- Horizontal Active Start Position for External HD - Horizontal Active Start Position for External SD1	0
[19:9]	EXT_h_size	- Horizontal Active Size for External HD - Horizontal Active End Position for External SD1	0
[31:20]	–	Reserved	–

EXTENAL HD VERTICAL ACTIVE CONTROL REGISTER

Description

DP_REG_29

Name	Address	Description	Type	Reset value
DP_REG_29	BAR0+874h	External HD vertical active	R/W	0

Bits	Name	Description	Reset value
[7:0]	HD_v_start	External HD vertical active start position	0
[17:8]	EXT_v_size	Vertical Active Size for External HD Vertical Active Size for External SD1	0
[31:18]	–	Reserved	–

EXTENAL BASE DISPLAY POINTER REGISTER

Description.

DP_REG_30

Name	Address	Description	Type	Reset value
DP_REG_30	BAR0+878h	External Base Display Pointer	R/W	0

Bits	Name	Description	Reset value
[3:0]	I_base_ptr	Delay processor base frame pointer	0
[7:4]	R_base_ptr	Read base frame pointer	0
[11:8]	W_base_ptr	Write base frame pointer	0
[31:12]	–	Reserved	–

1Hz SIZE FOR EXTENAL DISPLAY POINTER REGISTER

h_size: means the space occupied by one horizontal line in the memory. It is an integer multiple of 128. 128 is denoted as 0x01. For example, if the input video is 704x480i,

128 * 5 < 704 < 128 * 6, ∴ 1h_size = 0x06

(Note: When writing with MMU at each module in the DP, it will always be performed in 4:2:2 mode regardless of the display mode.)

DP_REG_31

Name	Address	Description	Type	Reset value
DP_REG_31	BAR0+87ch	1h size for External Display Pointer	R/W	0

Bits	Name	Description	Reset value
[5:0]	sub_rd_1h_size	1H size for sub read pointer	0
[11:6]	EXT_1h_size	1H Size External HD or External SD1 (Set by 64-bit units) (6bit: 0~63 * 64 = 0 ~ 4095)	0
[17:12]	SD_1h_size	1H Size for External SD0 (6bit=0~63)	0
[23:18]	rd_1h_size	1H Size for FC0 (Reading Motion Data)	0
[29:24]	I_wr_1h_size	1H Size for Delay processor (Writing Delayed MPEG)	0
[31:30]	–	Reserved	–

SUB SAMPLE MODE AND MMU REQ LENGTH CONTROL REGISTER

A_req_length, B_req_length: Determines the transfer unit of the data to read from the MMU to line memory. Different transfer units are set according to the format of the saved data.
In Req_manager, it means the mmu_length to input to the MMU for the mmu_request. If the addr_diff (rd_addr - wr_addr) is large enough, the corresponding value given in the table below will be transferred. But, for the request at which the addr_diff becomes less than the corresponding value in the table, the remaining value (the value less than the Burst_Length) will be transferred.
*addr_diff: FIFO read address - FIFO write address.

	4:2:0 Normal	4:2:2 Normal	4:2:2 IPC
req_length=0	8	8	8
req_length=1	8	16	16

A_min_req_cycle, B_min_req_cycle: Controls the FIFO so that it cannot read the subsequent data until a specific time interval has passed..

DP_REG_32

Name	Address	Description	Type	Reset value
DP_REG_32	BAR0+880h	Sub sample mode & mmu request length	R/W	0

Bits	Name	Description	Reset value
[0]	subsample_mode_m	Sub sample mode for Main picture 0=1:1(Normal) mode 1=1:2 sub sample mode	0
[1]	–	Reserved	–
[2]	subsample_mode_s	Sub sample mode for Sub picture 0=1:1(Normal) mode 1=1:2 sub sample mode	0
[3]	–	Reserved	–
[4]	A_req_length	Requested data length from A FIFO(line memory) to MMU 0=8 word 1=16 word	0
[5]	B_req_length	Requested data length from B FIFO(line memory) to MMU 0=8 word 1=16 word	0
[12:6]	A_min_req_cycle	Minimum Cycle for the Next Request of FIFO A (7bit=0~127) Unit: ???	0
[19:13]	B_min_req_cycle	Minimum Cycle for the Next Request of FIFO B (7bit=0~127) Unit: ???	0
[31:20]	–	Reserved	–

MAIN PICTURE VERTICAL CONTROL REGISTER

.

DP_REG_33

Name	Address	Description	Type	Reset value
DP_REG_33	BAR0+884h	Main vertical filter coefficient and main video data vertical start location	R/W	0

Bits	Name	Description	Reset value
[9:0]	conv_ratio	Main picture vertical filter coefficient	0
[23:10]	main_v_start	Main picture vertical video data read start	0
[31:24]	–	Reserved	–

MAIN PICTURE HORIZONTAL START AND END CONTROL REGISTER

.

DP_REG_34

Name	Address	Description	Type	Reset value
DP_REG_34	BAR0+888h	Main picture horizontal start and end	R/W	0

Bits	Name	Description	Reset value
[9:0]	main_h_start	Main picture horizontal video data read start	0
[19:10]	main_h_end	Main picture horizontal video data read end	0
[31:20]	–	Reserved	–

MAIN PICTURE HORIZONTAL SIZE CONTROL REGISTER

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DP_REG_35

Name	Address	Description	Type	Reset value
DP_REG_35	BAR0+88ch	Main picture horizontal size and main picture horizontal active size	R/W	0

Bits	Name	Description	Reset value
[9:0]	main_h_size	Main picture horizontal pixel count	0
[19:10]	main_disp_hsize	Main picture horizontal display count(Capture기능에서)	0
[31:20]	–	Reserved	–

IPC THRESHOLD CONTROL REGISTER

.

DP_REG_37

Name	Address	Description	Type	Reset value
DP_REG_37	BAR0+894h	IPC threshold	R/W	0

Bits	Name	Description	Reset value
[1:0]	IPC_th1	IPC threshold for Step 1 in SP (8, 16, 32, 64)	0
[2]	IPC_th2	IPC threshold for Step 2 in SP (16, 32)	0
[3]	IPC_th3	IPC threshold for Step 3 in SP (16, 32)	
[31:4]	–	Reserved	–

PANORAMA CONTROL REGISTER

.

DP_REG_38

Name	Address	Description	Type	Reset value
DP_REG_38	BAR0+898h	Panorama on & Left/Center region Size	R/W	0

Bits	Name	Description	Reset value
[0]	pano_on	Panorama mode	0
[9:1]	L_end	Left region end in Panorama mode	0
[19:10]	C_end	Center region end in Panorama mode	
[31:20]	–	Reserved	–

MAIN PICTURE HORIZONTAL COEFFICIENT CONTROL REGISTER

.

DP_REG_39

Name	Address	Description	Type	Reset value
DP_REG_39	BAR0+89ch	Main picture horizontal coefficient	R/W	0

Bits	Name	Description	Reset value
[10:0]	h_coef	Main picture horizontal filter coefficient	0
[31:11]	–	Reserved	–

PANORAMA COEFFICIENT A AND B CONTROL REGISTER

.

DP_REG_40

Name	Address	Description	Type	Reset value
DP_REG_40	BAR0+8a0h	Panorama coefficient A & B	R/W	0

Bits	Name	Description	Reset value
[9:0]	h_coef_A	Panorama horizontal filter coef A	0
[19:10]	h_coef_B	Panorama horizontal filter coef B	0
[31:20]	–	Reserved	–

POLY PHASE FILTER COEFICIENT CONTROL REGISTER

.

DP_REG_41

Name	Address	Description	Type	Reset value
DP_REG_41	BAR0+8a4h	Poly phase filter coefficient 0	R/W	0x7ff0

Bits	Name	Description	Reset value
[15:0]	poly0	Poly phase filter 0	0x7ff0
[31:16]	–	Reserved	–

POLY PHASE FILTER COEFICIENT CONTROL REGISTER

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DP_REG_42

Name	Address	Description	Type	Reset value
DP_REG_42	BAR0+8a8h	Poly phase filter coefficient 1	R/W	0x66fffa50

Bits	Name	Description	Reset value
[31:0]	poly1	Poly phase filter 1	0x66fffa50

POLY PHASE FILTER COEFICIENT CONTROL REGISTER

.

DP_REG_43

Name	Address	Description	Type	Reset value
DP_REG_43	BAR0+8ach	Poly phase filter coefficient 2	R/W	0x98764310

Bits	Name	Description	Reset value
[31:0]	poly2	Poly phase filter 2	0x98764310

POLY PHASE FILTER COEFICIENT CONTROL REGISTER

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DP_REG_44

Name	Address	Description	Type	Reset value
DP_REG_44	BAR0+8b0h	Poly phase filter coefficient 2	R/W	0x35790bba

Bits	Name	Description	Reset value
[31:0]	poly2	Poly phase filter 2	0x35790bba

POLY PHASE FILTER COEFICIENT CONTROL REGISTER

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DP_REG_45

Name	Address	Description	Type	Reset value
DP_REG_45	BAR0+8b4h	Poly phase filter coefficient	R/W	0x12348100

Bits	Name	Description	Reset value
[31:0]	poly3	Poly phase filter 3	0x12348100

POLY PHASE FILTER COEFICIENT CONTROL REGISTER

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DP_REG_46

Name	Address	Description	Type	Reset value
DP_REG_46	BAR0+8b8h	Poly phase filter coefficient 3	R/W	0x2b688dd6

Bits	Name	Description	Reset value
[31:0]	poly3	Poly phase filter 3	0x2b688dd6

POLY PHASE FILTER COEFICIENT CONTROL REGISTER

.

DP_REG_47

Name	Address	Description	Type	Reset value
DP_REG_47	BAR0+8bch	Poly phase filter coefficient 3	R/W	0xffef3adb

Bits	Name	Description	Reset value
[31:0]	poly3	Poly phase filter 3	0xffef3adb

POLY PHASE FILTER COEFICIENT CONTROL REGISTER

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DP_REG_48

Name	Address	Description	Type	Reset value
DP_REG_48	BAR0+8c0h	Poly phase filter coefficient 4	R/W	0x078f9fc0

Bits	Name	Description	Reset value
[27:0]	poly4	Poly phase filter 4	0x078f9fc0
[31:28]	–	Reserved	–

POLY PHASE FILTER COEFICIENT CONTROL REGISTER

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DP_REG_49

Name	Address	Description	Type	Reset value
DP_REG_49	BAR0+8c4h	Poly phase filter coefficient 4	R/W	0x05ac9b3a

Bits	Name	Description	Reset value
[27:0]	poly4	Poly phase filter 4	0x05ac9b3a
[31:28]	–	Reserved	–

POLY PHASE FILTER COEFICIENT CONTROL REGISTER

.

DP_REG_50

Name	Address	Description	Type	Reset value
DP_REG_50	BAR0+8c8h	Poly phase filter coefficient 4	R/W	0x030751a8

Bits	Name	Description	Reset value
[27:0]	poly4	Poly phase filter 4	0x030751a8
[31:28]	–	Reserved	–

POLY PHASE FILTER COEFICIENT CONTROL REGISTER

.

DP_REG_51

Name	Address	Description	Type	Reset value
DP_REG_51	BAR0+8cch	Poly phase filter coefficient 4	R/W	0x00820692

Bits	Name	Description	Reset value
[27:0]	poly4	Poly phase filter 4	0x00820692
[31:28]	–	Reserved	–

POLY PHASE FILTER COEFICIENT CONTROL REGISTER

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DP_REG_52

Name	Address	Description	Type	Reset value
DP_REG_52	BAR0+8d0h	Poly phase filter coefficient 5	R/W	0xbba97530

Bits	Name	Description	Reset value
[31:0]	poly5	Poly phase filter 5	0xbba97530

POLY PHASE FILTER COEFICIENT CONTROL REGISTER

.

DP_REG_53

Name	Address	Description	Type	Reset value
DP_REG_53	BAR0+8d4h	Poly phase filter coefficient 5	R/W	0x1346789a

Bits	Name	Description	Reset value
[31:0]	poly5	Poly phase filter 5	0x1346789a

POLY PHASE FILTER COEFICIENT CONTROL REGISTER

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DP_REG_54

Name	Address	Description	Type	Reset value
DP_REG_54	BAR0+8d8h	Poly phase filter coefficient 6	R/W	0x166bffa4

Bits	Name	Description	Reset value
[31:0]	poly6	Poly phase filter 6	0x166bffa4

POLY PHASE FILTER COEFICIENT CONTROL REGISTER

.

DP_REG_55

Name	Address	Description	Type	Reset value
DP_REG_55	BAR0+8dch	Poly phase filter coefficient 7	R/W	0x1ffc

Bits	Name	Description	Reset value
[15:0]	poly7	Poly phase filter 7	0x1ffc
[31:16]	–	Reserved	–

MAIN WRITE 1H SIZE CONTROL REGISTER

.

DP_REG_56

Name	Address	Description	Type	Reset value
DP_REG_56	BAR0+8e0h	Main Write 1h size	R/W	0

Bits	Name	Description	Reset value
[5:0]	wr_1h_size	1H write size	0
[31:6]	–	Reserved	–

MAIN COLOR MATRIX CONTROL REGISTER

.

DP_REG_57

Name	Address	Description	Type	Reset value
DP_REG_57	BAR0+8e4h	Main Color matirx	R/W	0

Bits	Name	Description	Reset value
[5:0]	main_yy1	Main picute color matrix : yy1	0
[11:6]	main_yy2	Main picute color matrix : yy2	0
[21:12]	main_cb1	Main picute color matrix : cb1	0
[31:22]	–	Reserved	–

MAIN COLOR MATRIX CONTROL REGISTER

.

DP_REG_58

Name	Address	Description	Type	Reset value
DP_REG_58	BAR0+8e8h	Main Color matirx	R/W	0

Bits	Name	Description	Reset value
[9:0]	main_cb2	Main picute color matrix : cb2	0
[19:10]	main_cr1	Main picute color matrix : cr1	0
[29:20]	main_cr2	Main picute color matrix : cr2	0
[31:30]	–	Reserved	–

MAIN BOUNDARY COLOR CONTROL REGISTER

.

DP_REG_59

Name	Address	Description	Type	Reset value
DP_REG_59	BAR0+8ech	Main boundary color	R/W	0

Bits	Name	Description	Reset value
[15:0]	main_bd_color	Main picture boundary color (6:5:5 YCbCr)	0
[31:16]	–	Reserved	–

SUB MMU REQUEST SIZE CONTROL REGISTER

.

DP_REG_60

Name	Address	Description	Type	Reset value
DP_REG_60	BAR0+8f0h	Sub mmu request size	R/W	0

Bits	Name	Description	Reset value
[0]	sub_req_length	Sub picture request length (1:16 word 0:8 word)	0
[7:1]	sub_min_req_cycle	Sub picture minimum request cycle	0
[31:9]	–	Reserved	–

SUB PICTURE HORIZONTAL SIZE CONTROL REGISTER

.

DP_REG_61

Name	Address	Description	Type	Reset value
DP_REG_61	BAR0+8f4h	Sub display & video data horizontal size	R/W	0

Bits	Name	Description	Reset value
[9:0]	sub_h_size	Sub picture horizontal pixel count	0
[18:10]	sub_disp_hsize	Sub picture horizontal display count	0
[31:19]	–	Reserved	–

SUB PICTURE HORIZONTAL FILTER CONTROL REGISTER

.

DP_REG_62

Name	Address	Description	Type	Reset value
DP_REG_62	BAR0+8f8h	Sub horizontal filter coefficient	R/W	0

Bits	Name	Description	Reset value
[9:0]	sub_req_length	Sub picture horizontal filter coefficient	0
[31:10]	–	Reserved	–

SUB PICTURE COLOR MATRIX CONTROL REGISTER

.

DP_REG_63

Name	Address	Description	Type	Reset value
DP_REG_63	BAR0+8fch	Sub Color matrix	R/W	0

Bits	Name	Description	Reset value
[5:0]	sub_yy1	Sub picute color matrix : yy1	0
[11:6]	sub_yy2	Sub picute color matrix : yy2	0
[21:12]	sub_cb1	Sub picute color matrix : cb1	0
[31:22]	–	Reserved	–

SUB PICTURE COLOR MATRIX CONTROL REGISTER

.

DP_REG_64

Name	Address	Description	Type	Reset value
DP_REG_64	BAR0+900h	Sub Color matrix	R/W	0

Bits	Name	Description	Reset value
[9:0]	sub_cb2	Sub picture color matrix : cb2	0
[19:10]	sub_cr1	Sub picture color matrix : cr1	0
[29:20]	sub_cr2	Sub picture color matrix : cr2	0
[31:30]	–	Reserved	–

SUB PICTURE VERTICAL SIZE CONTROL REGISTER

.

DP_REG_65

Name	Address	Description	Type	Reset value
DP_REG_65	BAR0+904h	Sub vertical filter coefficient / video data vertical start	R/W	0

Bits	Name	Description	Reset value
[9:0]	sub_conv_ratio	Sub picture vertical filter coefficient	0
[23:10]	sub_v_start	Sub picture vertical video data read start	0
[31:24]	–	Reserved	–

SUB PICTURE HORIZONTAL SIZE CONTROL REGISTER

.

DP_REG_66

Name	Address	Description	Type	Reset value
DP_REG_66	BAR0+908h	Sub video data horizontal start & end	R/W	0

Bits	Name	Description	Reset value
[9:0]	sub_h_start	Sub picture horizontal video data read start	0
[19:10]	sub_h_end	Sub picture horizontal video data read end	0
[31:20]	–	Reserved	–

SUB PICTURE BOUNDARY COLOR CONTROL REGISTER

.

DP_REG_67

Name	Address	Description	Type	Reset value
DP_REG_67	BAR0+90ch	Sub boundary color	R/W	0

Bits	Name	Description	Reset value
[15:0]	sub_conv_ratio	Sub picture boundary color (6:5:5 YCbCr)	0
[31:16]	–	Reserved	–

SUB PICTURE HORIZONTAL SIZE CONTROL REGISTER

.

DP_REG_68

Name	Address	Description	Type	Reset value
DP_REG_68	BAR0+910h	Display background color	R/W	0

Bits	Name	Description	Reset value
[15:0]	disp_bg_color	Display background color (6:5:5 YCbCr)	0
[16]	SD_GP-on	SD output uses video with Graphics	0
[17]	clipping	data clipping on	0
[20:18]	chroma_format	HD output Color format [19:18] (0) No Transform (1) 601 (2) RGB [20] (0) 4:2:2 YCbcr (1) 4:4:4 when 709 or 601	0
[21]	hd_656	656 HD digital output	0
[31:22]	–	Reserved	–

SD OUTPUT FILTRE RATIO CONTROL REGISTER

.

DP_REG_70

Name	Address	Description	Type	Reset value
DP_REG_70	BAR0+918h	SD output filter ratio	R/W	0

Bits	Name	Description	Reset value
[7:0]	h_ratio	SDout horizontal ratio	0
[17:8]	v_ratio	SDout vertical ratio	0
[31:18]	–	Reserved	–

DIGITAL ENCODER MODE CONTROL REGISTER

.

DP_REG_71

Name	Address	Description	Type	Reset value
DP_REG_71	BAR0+91ch	Digital Encoder Mode	R/W	0

Bits	Name	Description	Reset value
[0]	sqpx	Input/output data rate	0
[1]	lnfmt	Input/output field rate	0
[2]	phalt	chroma encodeing method	0
[3]	fdrst	enables FSC locked color signal generation	0
[4]	ped	ebalbes pedistal for video output	0
[6:5]	fscsel	color modulation frequency	0
[8:7]	ybw	luma output video bandwidth	0
[10:9]	cbw	chroma output video bandwidth	0
[13:11]	test_obs	test observability points	0
[14]	free_running	free running mode	0
[31:15]	–	Reserved	–

MACROVISION INTERFACE CONTROL REGISTER

.

DP_REG_72

Name	Address	Description	Type	Reset value
DP_REG_72	BAR0+920h	Macrovision interface	R/W	0xd2bd73e

Bits	Name	Description	Reset value
[31:0]	mv_reg0	Macrovision register x0, x1, x2, x3	0xd2bd73e

MACROVISION INTERFACE CONTROL REGISTER

.

DP_REG_73

Name	Address	Description	Type	Reset value
DP_REG_73	BAR0+924h	Macrovision interface	R/W	0x90db665b

Bits	Name	Description	Reset value
[31:0]	mv_reg1	Macrovision register x4, x5, x6, x7	0x90db665b

MACROVISION INTERFACE CONTROL REGISTER

.

DP_REG_74

Name	Address	Description	Type	Reset value
DP_REG_74	BAR0+928h	Macrovision interface	R/W	0x000000ff

Bits	Name	Description	Reset value
[31:0]	mv_reg2	Macrovision register x8, x9, x10, x11	0x000000ff

MACROVISION INTERFACE CONTROL REGISTER

.

DP_REG_75

Name	Address	Description	Type	Reset value
DP_REG_75	BAR0+92ch	Macrovision interface	R/W	0x020df6f0

Bits	Name	Description	Reset value
[31:0]	mv_reg3	Macrovision register x12, x13, x14, x15	0x020df6f0

MACROVISION INTERFACE CONTROL REGISTER

.

DP_REG_76

Name	Address	Description	Type	Reset value
DP_REG_76	BAR0+930h	Macrovision interface	R/W	0x0000f0cf

Bits	Name	Description	Reset value
[23:0]	mv_reg4	Macrovision register x16, x17, x40	0x0000f0cf
[31:24]	–	Reserved	–

MACROVISION INTERFACE CONTROL REGISTER

.

DP_REG_77

Name	Address	Description	Type	Reset value
DP_REG_77	BAR0+934h	Macrovision interface	R/W	0x00000000

Bits	Name	Description	Reset value
[31:0]	mv_reg5	Macrovision register x48, x49, x50, x51	0x000000ff

SD OUTPUT CAPTION CONTROL REGISTER

.

DP_REG_78

Name	Address	Description	Type	Reset value
DP_REG_78	BAR0+938h	SD output Caption Control	R/W	0

Bits	Name	Description	Reset value
[7:0]	cap1_3	caption data CC1(Field 1) or CC3(Field 2)	0
[15:8]	cap2_4	caption data CC2(Field 1) or CC3(Field 2)	0
[17:16]	cap_ctr	caption data validity	0
[31:18]	–	Reserved	–

DAC CONTROL REGISTER

.

DP_REG_79

Name	Address	Description	Type	Reset value
DP_REG_79	BAR0+93ch	DAC Control	R/W	0

Bits	Name	Description	Reset value
[2:0]	cap1_3	SD output DAC control 0 = blank : reset 1 = vsetup : output level shift 2 = sleep mode others = no effect	0
[5:3]	cap2_4	HD output DAC control 0 = blank : reset 1 = vsetup : output level shift 2 = sleep mode others = no effect	0
[31:6]	–	Reserved	–

INTERRUPT FLAG REGISTER

DP_REG_80

Name	Address	Description	Type	Reset value
DP_REG_80	BAR0+940h	Interrupt event register	R/W	0

Bits	Name	Description	Reset value
[0]	interupt_event_SD0	SD0 Interrupt Event 0 = SD0 interrupt is NOT generated 1 = SD0 interrupt is generated	0
[1]	interupt_event_HD	HD Interrupt Event 0 = HD interrupt is NOT generated 1 = HD interrupt is generated	0
[2]	interupt_event_SD1	SD1 Interrupt Event 0=SD1 interrupt is NOT generated 1=SD1 interrupt is generated	0
[31:3]	–	Reserved	–

INTERRUPT MASK REGISTER

Description.

DP_REG_81

Name	Address	Description	Type	Reset value
DP_REG_81	BAR0+944h	Interrupt mask register	R/W	0

Bits	Name	Description	Reset value
[0]	interupt_event_mask_SD0	SD0 Interrupt Event Mask 0=SD0 interrupt is NOT Masked 1=SD0 interrupt is Masked	0
[1]	interupt_event_mask_HD	HD Interrupt Event Mask 0=HD interrupt is NOT Masked 1=HD interrupt is Masked	0
[2]	interupt_event_mask_SD1	SD1 Interrupt Event Mask 0=SD1 interrupt is NOT Masked 1=SD1 interrupt is Masked	0
[31:3]	–	Reserved	–

SD INTERRUPT INPUT CONTROL REGISTER

Description

DP_REG_82

Name	Address	Description	Type	Reset value
DP_REG_82	BAR0+948h	SD interrupt input	R/W	0

Bits	Name	Description	Reset value
[0]	SD0_toggle_cnt_on	The Start of Counting the Field_ID Toggle 0 = Disable SD0 toggle counter operation 1 = Enable SD0 toggle counter operation	0
[2:1]	SD0_cpu_mode	External SD0 CPU Mode 0 = Normal 3D-IPC 1 = Normal 2D-IPC (EOSI) 2 = 2D-IPC 3 = SD I/F Auto Detection	0
[12:3]	SD0_field_num	The Number of Fields for the Counting Field_ID Toggle The number of fields to be tested in order to determine whether the field ID is toggled or not.	0
[31:13]	–	Reserved	–

HD INTERRUPT INPUT CONTROL REGISTER

DP_REG_83

Name	Address	Description	Type	Reset value
DP_REG_83	BAR0+94ch	HD interrupt input	R/W	0

Bits	Name	Description	Reset value
[0]	Sel_HD_SD	Start of Source Format Detection at HD I/F Module	0
[31:1]	–	Reserved	–

SD TOGGLE COUNT REGISTER

.

DP_REG_84

Name	Address	Description	Type	Reset value
DP_REG_84	BAR0+950h	SD toggle count	R	0

Bits	Name	Description	Reset value
[9:0]	SD0_toggle_cnt	The Count of Field_ID Toggling at SD0 I/F Module	0
[19:10]	SD1_toggle_cnt	The Count of Field_ID Toggling at SD1 I/F Module	0
[31:11]	–	Reserved	–

HD PROGRESSIVE COUNT REGISTER

.

DP_REG_85

Name	Address	Description	Type	Reset value
DP_REG_85	BAR0+954h	HD progressive & 4line count at 81MHz	R	0

Bits	Name	Description	Reset value
[0]	prog_inter	Progressive/Interlace Indication at HD I/F	0
[15:1]	clk67p5_cnt	Counting Based on 67.5MHz for 10 Line at HD I/F (The count obtained when the 10 horizontal-line of HD input is counted with 67.5-MHz frequency.)	0
[31:16]	–	Reserved	–

HD VERTICAL AND HORIZONTAL COUNT REGISTER

The pixel count of the HD horizontal 1 line which is counted by clock input (for example,74.25MHz) to the HD input clock pin.

DP_REG_86

Name	Address	Description	Type	Reset value
DP_REG_86	BAR0+958h	HD vertical & horizontal count	R	0

Bits	Name	Description	Reset value
[12:0]	h_cnt	Pixel Count for 1 Line in HD I/F Module	0
[23:13]	v_cnt	Line Count for 1 Frame in HD I/F Module	0
[31:24]	–	Reserved	–

HD OUTPUT ANALOG SYNC CONTROL REGISTER

.

DP_REG_87

Name	Address	Description	Type	Reset value
DP_REG_87	BAR0+95ch	HD output Analog sync control	R/W	0

Bits	Name	Description	Reset value
[1:0]	HDout_insize	HD Format (0:1080i 1:720p 2:480P)	0
[3:2]	HDout_mode	Analog HD Format 0 = YPbPr with 3 Level Sync 2 = RGB with 3 Level Sync 3 = RGB without sync	0
[4]	HDout_RGBY_offset	Setting "1" if Blank Level is 16	0
[11:5]	HDout_hsync_pos	Analog H Sync Tip	0
[20:12]	HDout_v_h_start	Analog V Start	0
[31:21]	–	Reserved	–

HD AND SD OUTPUT DAC CONTROL REGISTER

.

DP_REG_88

Name	Address	Description	Type	Reset value
DP_REG_88	BAR0+960h	HD out & SD out DAC Connection status	R	0

Bits	Name	Description	Reset value
[0]	SDout_DAC_sensez	0 = Hi-Z 1 = SD out DAC Connection	0
[1]	HDout_DAC_sensez	0 = Hi-Z 1 = HD out DAC Connection	0
[31:2]	–	Reserved	–

SD HORIZONTAL CONTROL REGISTER

.

DP_REG_89

Name	Address	Description	Type	Reset value
DP_REG_89	BAR0+964h	SD horizontal start & end	R/W	0

Bits	Name	Description	Reset value
[7:0]	SDout_h_act_st	Horizontal Active Start for SD Output Generation	0
[18:8]	SDout_h_act_end	Horizontal Active End for SD Output Generation	0
[29:19]	SDout_denc_delay	Sync Delay for DENC(NTSC-Encoder)	
[31:30]	–	Reserved	–

HD AND SD SELECTION CONTROL REGISTER

.

DP_REG_90

Name	Address	Description	Type	Reset value
DP_REG_90	BAR0+968h	HD/SD select	R/W	0

Bits	Name	Description	Reset value
[0]	Sel_HD_SD	External input muxing 0=SD1 input enable 1=HD input enable	0
[1]	SD1_on	Operation enable for SD1 I/F module???	0
[7:2]	Ext_sync_type	Input Sync Polarity for External SD1 See also Sync_type.	
[13:8]	SD1_v_start_o	External SD1 vertical active start position (odd field) ???	
[19:14]	SD1_v_start_e	External SD1 vertical active start position (even field) ???	
[20]	SD1_toggle_cnt_on	The start of counting the Field_ID toggle 0=Disable SD1 toggle counter operation 1=Enable SD1 toggle counter operation	
[31:21]	–	Reserved	–

POLY PHASE FILTER SIGN REGISTER

.

DP_REG_91

Name	Address	Description	Type	Reset value
DP_REG_91	BAR0+96ch	Poly phase filter sign	R/W	0

Bits	Name	Description	Reset value
[20:0]	–	Reserved	–
[30:21]	SD1_field_num	The Number of Field for Counting Field_ID_Toggle	0
[31]	–	Reserved	–

POLY PHASE FILTER SIGN REGISTER

.

DP_REG_92

Name	Address	Description	Type	Reset value
DP_REG_92	BAR0+970h	Poly phase filter sign	R/W	0

Bits	Name	Description	Reset value

Table 2-1. S5H2000X Register map (continued: DP control register)

Name	Address	Description	Type	Reset value
DP_REG_93	BAR0+974h	Polyphase filter sign	R/W	0
DP_REG_94	BAR0+978h	Polyphase filter sign	R/W	0
DP_REG_95	BAR0+97ch	SD output vertical position	R/W	0
DP_REG_96	BAR0+980h	SD output vertical position	R/W	0
DP_REG_93	BAR0+974h	Polyphase filter sign	R/W	0
DP_REG_94	BAR0+978h	Polyphase filter sign	R/W	0
DP_REG_95	BAR0+97ch	SD output vertical position	R/W	0

NOTE

7 GRAPHIC PROCESSOR

7.1 OVERVIEW

The Graphic Module consists of 3 sub-modules: the GP (Graphic Processor), the GA (Graphic Accelerator), and the memory bank. The GP reads graphic data on local memory via the MMU and mixes it with video signals input from the DP. The GA quickly transfers the graphic data on the system memory to the local memory via the PCI interface and performs various quick pixel operations with the H/W. The Memory Bank is a module that contains the line memory and CLUT used by the GP.

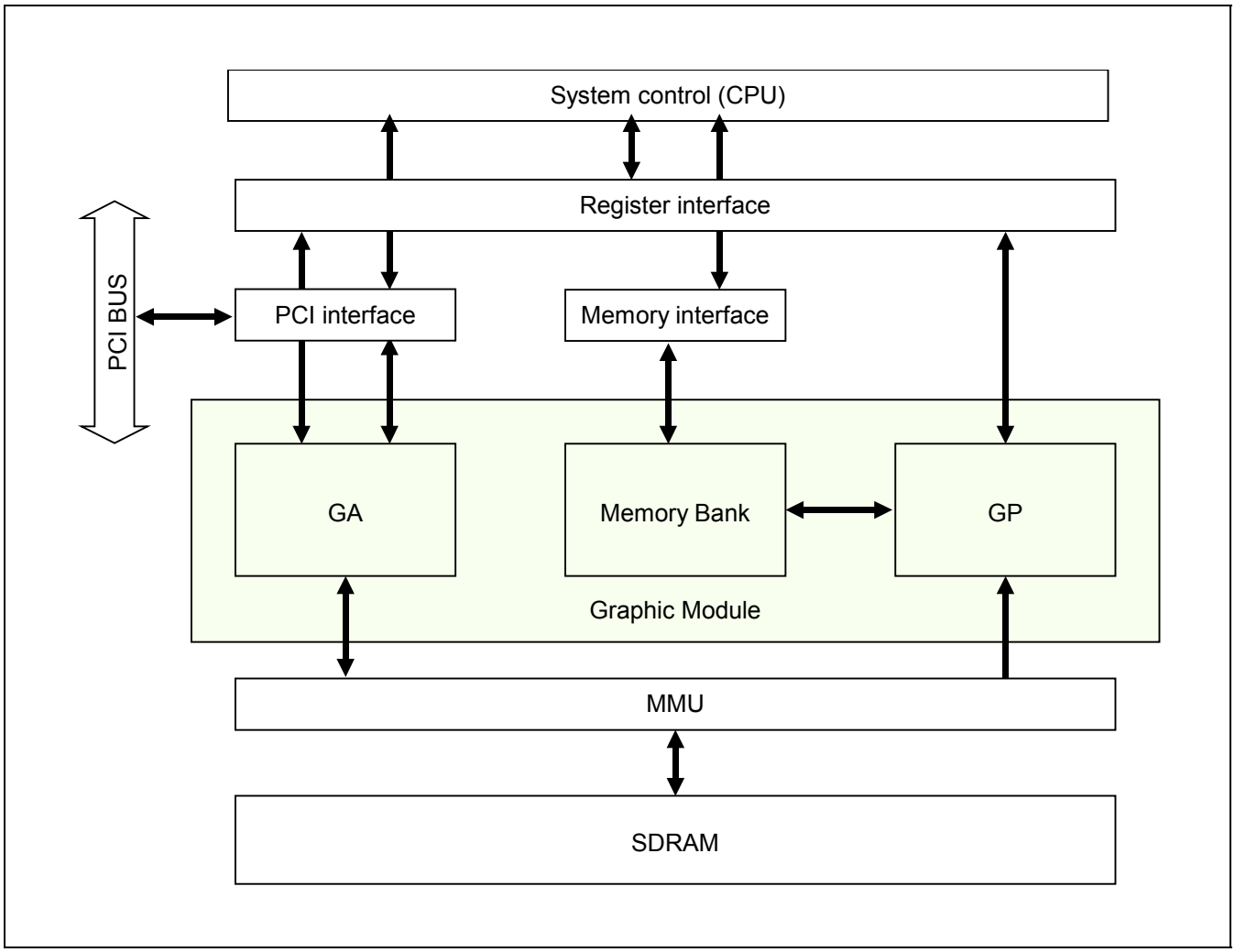


Figure 7-1 Graphic Processor block diagram

7.2 Feature

- Graphic Windows
- Graphic Windows
  - Up to 4 windows can be displayed on the screen at the same time.
  - A window has an arbitrary size within the screen size. However, the width should be an even number.
  - A window has an arbitrary position regardless of the screen size. That is, it can be located outside the screen. The regions outside the screen are automatically clipped.
  - Each window can have its own graphic format.
  - Each window has a priority of 0 to 3. Priority 0 is the highest and 3 is the lowest. The higher priority window is displayed as the foreground window and the lower priority window is overlaid by the higher priority window.
  - A window can be zoomed-in twice its size horizontally and vertically.
  - Each window has the sub-window display function that displays a small rectangle area within the window.

- Window Graphic Formats: Each window can have one of the following graphic formats.
  - 8bit bitmap RGB 565
  - 8bit bitmap RGBα 5551
  - 8bit bitmap RGBα 4444
  - 16bit graphic RGB 565
  - 16bit graphic RGBα 5551
  - 16bit graphic RGBα 4444

- Blending
  - Window Blending: 32-level window blending can be applied to each window. It is a blending mode that can be applied to all pixels of a window regardless of its graphic format.
  - Pixel Blending: A 16-level blending factor that can be applied to each pixel of a window.
    - ▸ RGBα 5551: LSB 0 bit is used as the index of the 4-bit blending factor table.
    - ▸ RGBα 4444: LSB 3~0 bits are the 4-bit blending factor.

      For a window that has pixel blending, both window blending and pixel blending can be applied at the same time. The blending factor is obtained by multiplying the two blending factors.

- Blending Layer
  - There is a blending layer composed of video and graphic layers.
  - An arbitrary sized video input from the display processor is mapped to the video layer.
  - Four windows are overlaid in the order of their priority.
  - Vertical hierarchy can be applied for 2 blending layers in an arbitrary order. That is, the video layer can be positioned above or below the graphic layer.
  - Blending is performed to the lower layer using the blending factor of the upper layer.

- H/W Cursor
  - Always positioned on the upper layer.
  - Can have a maximum width of 128 pixels (horizontal) and the maximum screen size height (vertical).
  - 4 bits/pixel bitmap (16 colors).
  - Supports YCbCr655 color format only.
  - Color value 0 is transparent.
  - H/W blinking is supported with 1 ~ 64 frames period.

- Graphic Accelerator
  - Supports 8-bit bitmap, 16-bit true color.
  - Block transfers the 8-bit/16-bit data of the 32-bit width which is being transferred to the CPU memory (source) and to the external SDRAM via the MMU interface. (block copy)
  - Can block transfer the data which has a smaller width than the source block data.

7.3 Function Spec

7.3.1 H/W Window

The S5H2000X graphic processor (henceforth, GP) supports 4 graphic planes. The graphic plane need not be the same size as the screen and can be smaller than the screen and a different size than the existing graphic H/W. The graphic plane can be positioned outside the screen. However, the plane region outside the screen will be clipped. Due to these characteristics, the graphic plane is named a window. A window (i.e., a graphic plane) is an H/W window different than an S/W window on a Windows PC system.

The GP has four H/W windows and each window can have the following attributes.

7.3.1.1 Window ID (Priority)

A priority is assigned to determine the order in which the H/W windows are displayed on the screen when overlaid partly or entirely. An H/W window has a unique ID that ranges from 0 to 3. This window ID represents the priority of the window. 0 means the highest priority and 3 means the lowest priority. When there is more than one window created and they have been overlaid, the window that has higher priority is displayed on top of the lower priority window.

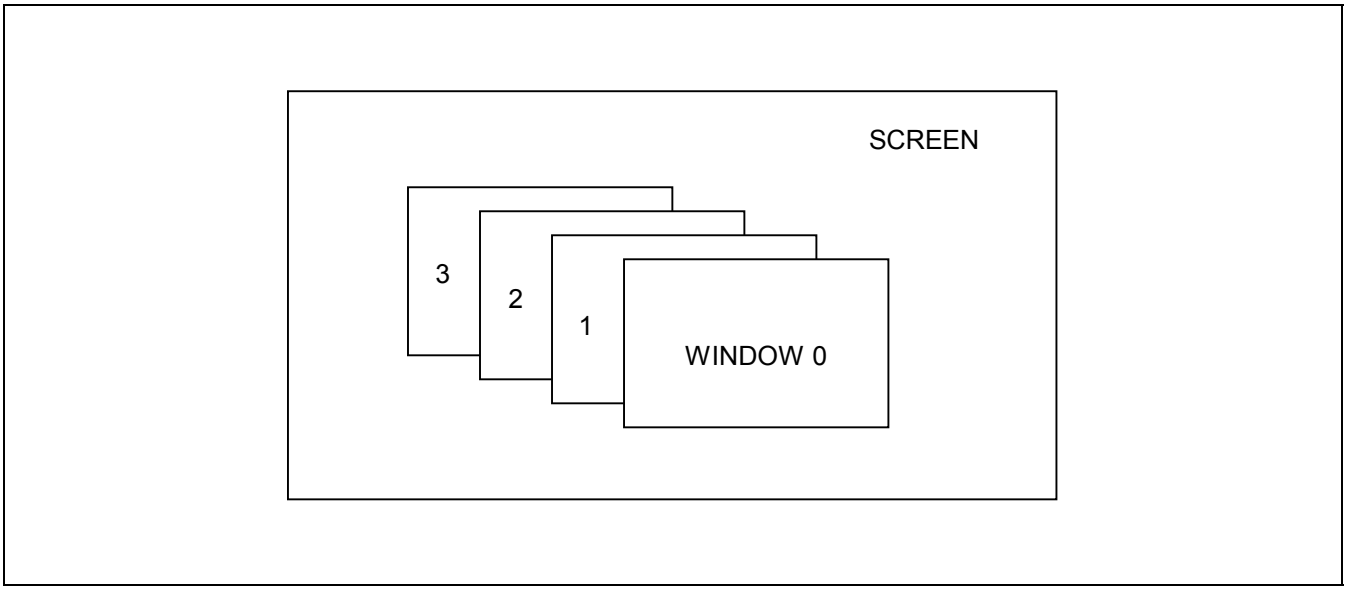


Figure 7-1 WINDOW ID ON SCREEN

7.3.1.2 Window Position & Size

Window Position and Size indicates the position, width (horizontal size) and height (vertical size) of the window on the screen. A window can be any size smaller than the screen, and need not be the same size as the screen. However, for the 8-bit/pixel format, the window must have a width of pixels equaling a multiple of an even integer due to the characteristics of a 4:2:2 display. For the 16-bit format, a window can have a size equal to or less than 1/2 the size of the screen. But, a window that is 1/2 size of the screen can be enlarged to screen size with the horizontal 2X zoom-in function. Therefore, a window displayed on the screen always has pixels equaling the

multiple of an even integer, but the actual width (horizontal size) need not be an even number.

The position of a window is represented by the coordinates of its upper-left pixel of the screen. The origin (0, 0) is located at the upper-left pixel of the screen. The position of a window need not be limited to the inside of the screen. Part or the entire area can be positioned outside the screen. A window (graphic plane) can also have a negative position and can be positioned at a coordinate completely outside the screen.

Due to the characteristics of a 4:2:2 display, a window should be positioned on a horizontal coordinate pixel equaling a multiple of an even integer. The area outside the screen will be clipped. By using these functions, the auto-hiding function that slides in the task bar when the cursor positions over it, as in Microsoft Windows, can be implemented simply without the burden of S/W.

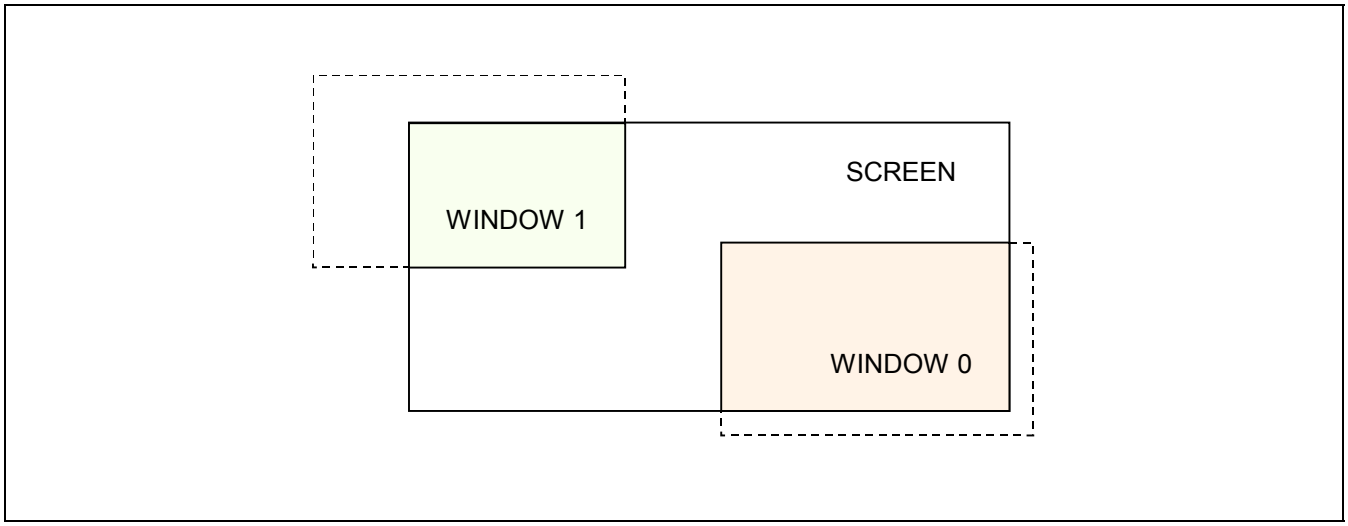


Figure 7-2 WINDOWS POSITION AND SIZE ON SCREEN

7.3.1.3 Horizontal Byte Size of a Window

For each window, the horizontal byte size of its actual window on the screen should be specified. This is necessary because the sub-window display function that implements the display of the actual window larger than the actual window requires that the H/W has to know the actual window's horizontal byte size to calculate the start address of the next line. In the sub-window function, the horizontal size of the window is calculated with the horizontal size of the sub-window and has no relationship with the horizontal byte size of the actual window. As shown in the following figure, a sub-window can be implemented by assigning a parameter less than the size of the actual pixel data of the window on local memory. In this case, the horizontal byte size of the actual window should be set the horizontal size of the original window on the memory.

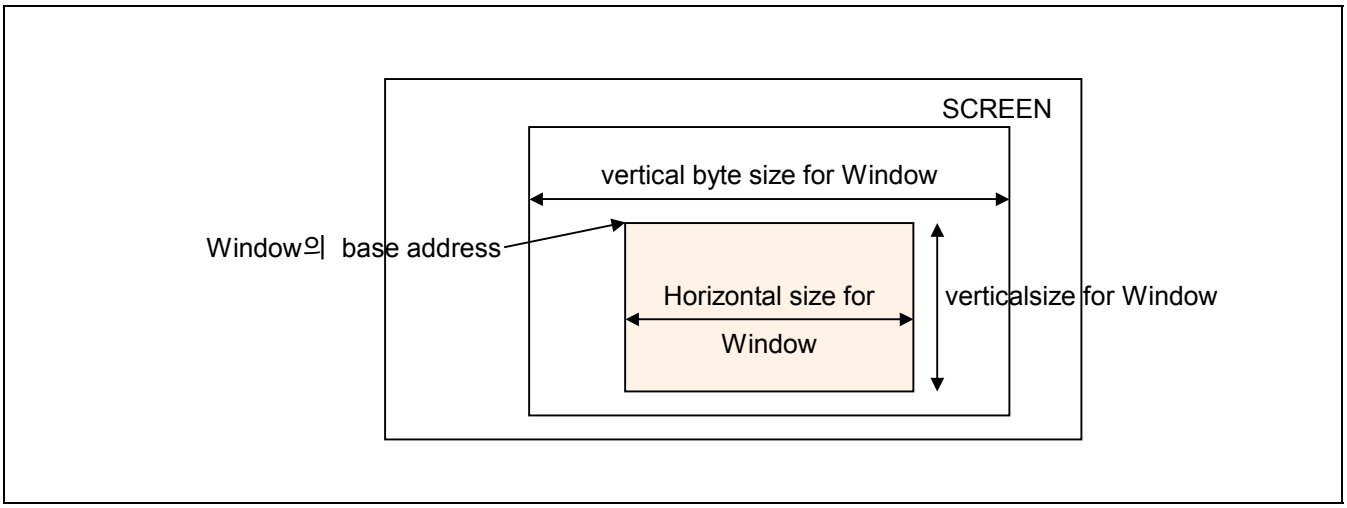


Figure 7-2 WINDOWS POSITION AND SIZE ON SCREEN

7.3.1.4 Layer ID

The GP has 2 blending layers: a video and a graphic layer. The Video layer is made of the signals transferred to the GP from the MPEG video output or the external input video via the Display Processor (DP). The Graphic layer is the blending layer for graphic images. The windows that belong to the graphic layer are overlaid according to their priority and they is no blending between them. The vertical hierarchy of the two layers is variable. That is, the video layer need not always be positioned over the graphic layer, but can be positioned over graphic layer.

7.3.1.5 Visibility

This parameter controls whether to show or hide a window on the screen.

7.3.1.6 Window Color Format

This attribute represents the color format of a window. Both 8-bit bitmap and 16-bit high color modes are supported. Each window can have a separate color format, and more than one window with different color formats can be displayed on the screen at the same time. However, 8-bit bitmap windows share a common color look up table (CLUT). The following table shows the supported types of color formats.

Table 7-1 color formats

Color Format	Blending mode
8bit index RGB 5:6:5	no blending
8bit index RGBa 5:5:5:1	1bit index for 4bit pixel blending table
8bit index RGBa 4:4:4:4	4bit pixel blending factor
16bit RGB 5:6:5	no blending
16bit RGBa 5:5:5:1	1bit index for 4bit pixel blending table
16bit RGBa 4:4:4:4	4bit pixel blending factor

A window is specified in RGB format. The actual color that the GP H/W processes is YCbCr. In this format, the low bits of each color component are filled with 0 to make 8 bits and then the color is processed. Hence, the 6, 5, and 4 bits shown in the table above represent the high bits of 8-bit color. RGB is also filled with 0 to make 8 bits and then converted to YCbCr before processing.

7.3.1.7 Window Blend Enable & Blend factor

Window Blend is a common mode that applies the 5 bit (32 level) blending factor to all pixels of a window. The window blending factor can be specified separately for each window. It applies the 32 level blending factor specified to all pixels of a window regardless of its color format. The window blending mode can be enabled/disabled with the window blend enable flag.

7.3.1.8 Pixel Blend Enable

For a window that has the color format RGBa 5551 or RGBa 4444, the bend factor can be specified for each pixel. Each window has a blend table that represents a 4-bit blending factor. The index of this blend table is used as the blending factor for 1 bit pixel blending, while, the entire table is used as the blending factor for 4-bit pixel blending. Pixel blending can be enabled/disabled with the pixel blend enable flag.

7.3.1.9 Blend enable

This flag determines whether to apply the blending mode to the window. When set to On, the current blending mode specified to the window is applied..

At this time, if both Window Blend and Pixel Blend are enabled, the two blending modes will be applied at the same time. Therefore, the blending factor is obtained by multiplying the two blending factors. When the blend enable flag is set to Off, the window becomes an opaque window regardless of its blending mode(s).

7.3.1.10 Window Horizontal Doubling

This function displays the window by enlarging it 2 times in a horizontal direction. This is implemented by pixel replication. For the 8-bit bitmap mode, both normal display and horizontal doubling can be selected. But, for the 16-bit color format mode, only the horizontal doubling mode should be used for the architectural reason that the H/W and is enabled automatically by the API. Therefore, for a 16-bit color format window, its horizontal size should be 1/2 of the pixel size of the actual window to be displayed on the screen.

7.3.1.11 Window Vertical Doubling

When set to ON, the window is displayed enlarged 2 times vertically. This function is implemented with line duplication. As opposed to horizontal doubling, both normal display and vertical doubling can be selected for 8-bit and 16-bit formats.

7.3.1.12 Window Base Address

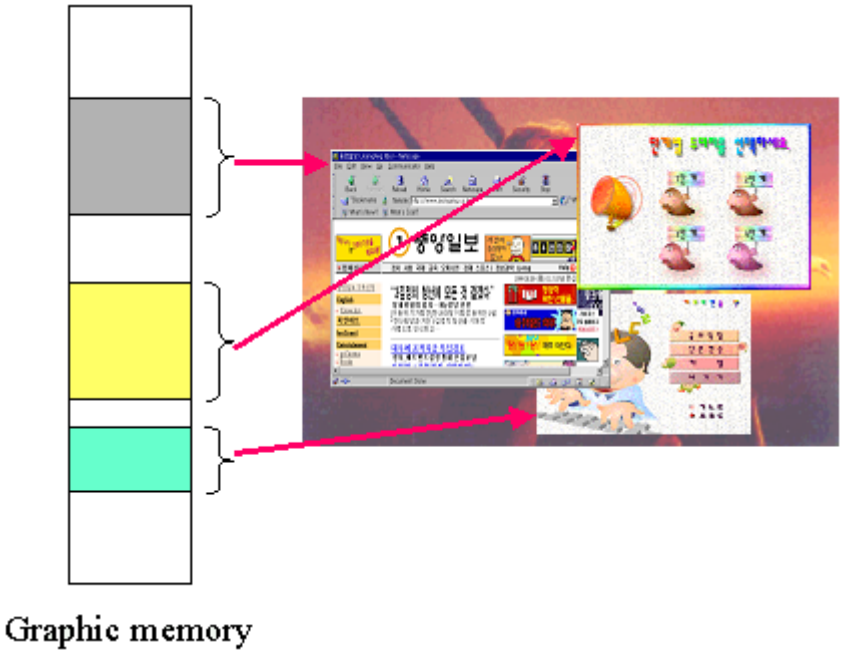
The Window Base Address is the pointer to the frame buffer allocated to a window. The unit is a byte. It means the offset to the local memory base address on the system memory map. A virtual window frame buffer can exist any place, either in the system memory or the local memory. But, the frame buffer which is registered to the H/W window and displayed on the screen must always exist in the local memory.

7.3.1.13 Transparent Color Enable

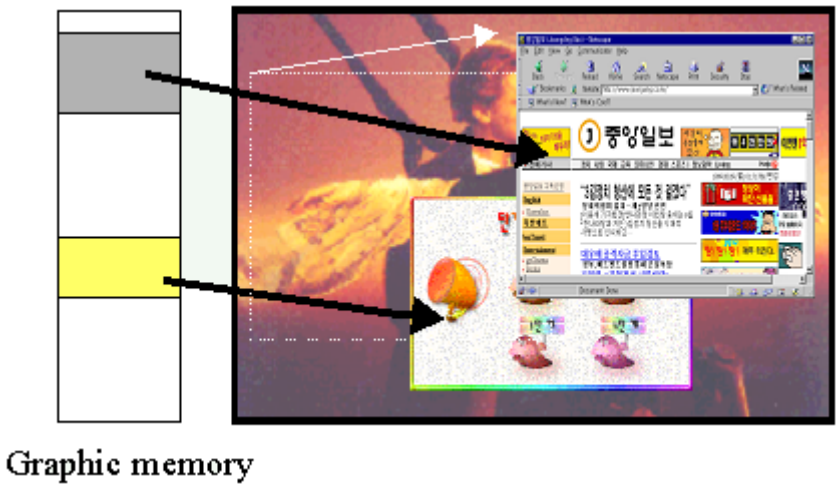
When enabled, a pixel is processed as a transparent color when its RGB value is 0. When disabled, it is processed as black.

7.3.1.14 Window Examples

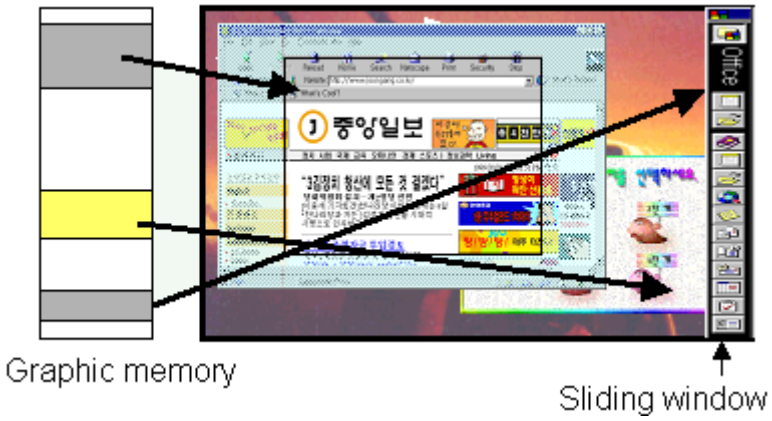
- Windows overlay



- Windows location & priority change



- Sub-window & out of screen location



7.3.2 Blending

Basically, blending is performed between the layers that have vertical hierarchy. Assuming that Pixel A is on the upper layer and has the blending factor á, and Pixel B is on the lower layer, the blending result X is obtained as shown in the following formula:

$$X = á*A + (1-á)*B \quad (0 < á < 1)$$

As mentioned above, there are two blending modes: Window Blending and Pixel Blending.

For Window Blending, a 5-bit blending factor is allocated for each window and is applied to all pixels on a window. Pixel Blending is applied to only the pixels of the color format which have the specified pixel blending factor. If both of the blending modes are enabled, they are applied at the same time.

7.3.2.1 Blending Layers

Windows have their own priority and construct a vertical hierarchy. But this means only a vertical overlay of windows and does not mean a blending hierarchy. That is, it means simply that a lower priority window is overlaid by a higher priority window. When they are overlaid, the blending factor of the overlaid area is always that of the higher priority window. For blending, the S5H2000X GP provides a separate graphic layer which is different from the window hierarchy.

A window must belong to this layer. Window overlay according to priority is performed between the windows that belong to the graphic layer. Blending is performed between the video and the graphic layer, and the vertical hierarchy between both layers is variable. As described above, video need not always be lower than the graphic layer and can be positioned over the graphic layer. In this case, the video size should be less than the screen size to display the lower graphic layer. The area out of the video area is processed as transparent color. Blending is performed between the windows that belong to different layers. Assuming that A is a pixel on the lower layer, B is a pixel on the upper layer, and the blending factor is â, the blending result X is:

$$X = (B*â + (1-â)*A) \quad (0 < â < 1)$$

7.3.2.2 Blending Factor

Window blending factor is composed of 5-bits and has the range of 0 to 31. 0 indicates that the pixel is transparent, and 31, opaque. In actual calculations, blending factor â is obtained with the following statements.

```
if (factor == 0) {
    α = 0;
} else {
    α = (factor + 1) / 32;
}
```

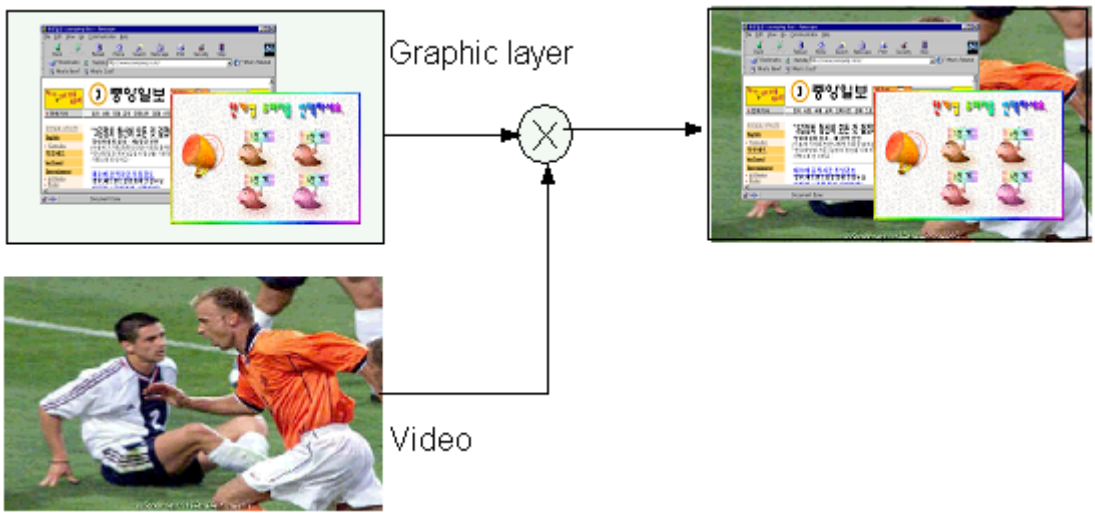
Pixel blending factor is composed of 4-bits and has the range of 0 to 15. 0 indicates that the pixel is transparent, and 15, opaque. Opaque level increases linearly from 0 to 15. In actual calculations, blending factor â is obtained with the following statements.

```
if (factor == 0) {
    α = 0;
} else {
    α = 2*(factor + 1) / 32;
}
```

Depending on color format, either 1- or 4-bit blending factor is used for pixel blending. In case of 4-bit factor type, all 4 bits are used as pixel blending factor as they are. In case of 1-bit factor type, the bit is used as the index to the 4-bit blending factor table. Each window has a blending factor table that has two entries, and the bit is used as the index to that table. Therefore, though there are two blending factor types available for 1-bit pixel blending mode, both factors have the same 16 factor levels (0 to 15).

7.3.2.3 Blending Example

- Blending Layers



7.3.3 Graphic Effects

7.3.3.1 Background Color

This function replaces the video layer with a specified color. It can be turned on/off and any color can be set as the background color.

7.3.3.2 Progressive/Interlace Display

When saving graphic data to the graphic frame buffer allocated to a window, it should always be saved in the progressive display order.

But, video output should satisfy both the interlaced and progressive output to comply with MPEG video MP@HL specifications. To satisfy this specification, the GP needs to access graphic data on a frame buffer in accordance with video output. Then, when the video output method changes, it only has to modify the progressive/interlaced parameter of the GP according to the changes.

7.3.4 H/W Cursor

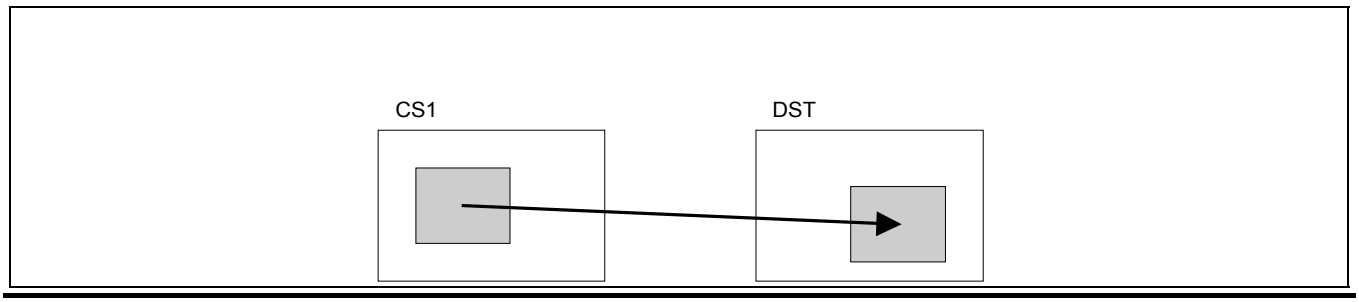
The GP supports the H/W cursor. The cursor is positioned on the uppermost layer of vertical hierarchy. The size of cursor is 128 pixels horizontally and equal to the vertical screen size vertically. Only 4-bit bitmap (16 colors) is supported for each pixel as a data format. YCbCr655 format is supported as a color format. If the color value of a pixel is 0, it is processed as transparent color. The cursor is basically a rectangle, but it can be formed into any shape using transparent color. It should exist in the local memory and the base address and horizontal byte size should be registered with the API. A feature of the GP cursor is blinking. The cursor blinks according to the specified frame cycle. The blinking cycle can be 1 frame to 64 frames.

7.3.5 Graphic Accelerator

The Graphic Accelerator (henceforth, GA) is the module that quickly processes block copy between windows using a BitBLT engine without intervention of the CPU. This is not the processing between the video and graphic layers but the processing between the graphic data of the two windows. The window that the GA processes need not be the active window, and it could be a virtual window buffer unregistered as a H/W window. But, a virtual window should have 8- or 16-bit color format which is a possible format for an H/W window.

7.3.5.1 BitBLT Type

For block copy, only one source block can be specified and it should exist in the system memory area.



The above figure shows block copy from the system memory area to the frame buffer of a window.

WINDOW HORIZONTAL POSIOTION REGISTER 0 ~ 3

There are 4 horizontal position registers for each window. They specify the horizontal start and end points of a window.

WHPR_0 ~ WHPR_3

Name	Address	Description	Type	Reset value
WHPR_n	BAR0+a00h + 4*n	Horizontal position register for window n	R/W	0

Bits	Name	Description	Reset value
[10:0]	WHEP	Window Horizontal End Point Indicates the horizontal end point of a window on the screen. In API, the horizontal start point and the horizontal pixel count are used as input parameters for convenience. Then, the horizontal end point is calculated and set to this field. Be careful that the end point is not calculated as (start point + size -1) but as (start point + size) due to architectural reasons of the H/W. The end point represents the actual pixel position on the screen. So, if the window is in the Horizontal Doubling mode, the end point should be calculated as (start point + size * 2).	0
[15:11]	–	Reserved	–
[26:16]	WHSP	Window Horizontal Start Point Indicates the horizontal start point of a window assuming that the upper-left pixel of the screen is (0, 0). The value should be always an even value due to the 4:2:2 characteristics of the video.	
[31:27]	–	Reserved	–

* n = 0 ~ 3

WINDOW VERTICAL POSIOTION REGISTER 0 ~ 3

There are 4 vertical position registers for each window. They specify the vertical start and end points of a window.

WVPR_0 ~ WVPR_3

Name	Address	Description	Type	Reset value
WVPR_n	BAR0+a20h +4*n	Vertical position register for window n	R/W	0

Bits	Name	Description	Reset value
[10:0]	WVEP	Window Vertical End Point Indicates the vertical end point of a window on the screen. In API, the vertical start point and the vertical pixel count are used as input parameters for convenience. Then, the vertical end point is calculated and set to this field. Be careful that the end point is not calculated as (start point + size -1) but as (start point + size) due to architectural reasons of the H/W. The end point represents the actual pixel position on the screen. So, if the window is in Vertical Doubling mode, the end point should be calculated as (start point + size * 2).	0
[15:11]	–	Reserved	–
[26:16]	WVSP	Window Vertical Start Point Indicates the vertical start point of a window assuming that the upper-left pixel of the screen is (0, 0).	
[31:27]	–	Reserved	–

* n = 0 ~ 3

WINDOW MODE REGISTER 0 ~ 3

There are 4 mode registers for each window. They specify the operational characteristics of a window.

WMR_0 ~ WMR_3

Name	Address	Description	Type	Reset value
WMR_n	BAR0+a40h + 4*n	Mode register for window n	R/W	0

Bits	Name	Description	Reset value
[4:0]	WBF	Window Blending Factor Defines 32 window blending levels. The value range is 0 to 31. 0 means transparent and 31 means opaque.	0
[5]	HDE	Horizontal Doubling Enable 0 = Displays the window normally. 1 = Repeats each horizontal pixel twice so that the horizontal size of the window displayed on the screen is two times the size of the window in memory. For 16-bit true color format, this flag must be set to enable (1).	0
[6]	VDE	Vertical Doubling Enable 0 = Displays the window normally. 1 = Repeats each vertical pixel twice so that the vertical size of the window displayed on the screen is two times the size of the window in memory. As opposed to Horizontal Doubling, this flag need not be set to enable (1) for 16-bit true color format.	0
[10:7]	WOSGF	Window OSG Format Defines the OSG format of the window. Supported formats are: 0 = bit bitmap, RGB 5:6:5 1 = bit bitmap, RGBá 5:5:5:1 2 = bit bitmap, RGBá 4:4:4:4 3 ~ 7 = reserved 8 = bit graphic, RGB 5:6:5 9 = bit graphic, RGBá 5:5:5:1 10 = bit graphic, RGBá 4:4:4:4 11 ~ 15 = reserved	0

*n = 0 ~ 3

WMR_0 ~ WMR_3 (Continued)

Bits	Name	Description	Reset value
[11]	PBE	Pixel Blending Enable 0 = Does not apply pixel blending. 1 = Applies pixel blending when the format of a pixel has a pixel blending factor. * If both window blending and pixel blending are enabled, the window blending factor * and pixel blending factor will be applied.	0
[12]	WBE	Window Blending Enable 0 = Does not apply window blending. 1 = Applies window blending to the all pixels of the window.	0
[13]	BE	Blending Enable 0 = Blending off. 1 = Applies the blending mode(s) specified for the window.	0
[14]	WV	Window Visibility 0 = Hides the window from the screen. 1 = Shows the window on the screen.	0
[15]	–	Reserved	–
[26:16]	WHBS	Window Horizontal Byte Size Indicates the horizontal byte size of the window mapped in the memory. It can be calculated from the horizontal pixel size of the window. But, it has no relationship with the horizontal pixel size when displaying a sub-window which is smaller that the size of the actual window in the memory. Hence, the horizontal byte size of the actual window should be set separately for correct calculation of the start address of each line of the window.	0
[27]	TCE	Transparent Color Enable Specifies whether to process the pixel whose color Y component is 0 or RGB is 0 as transparent color or black.	0
[31:28]	–	Reserved	–

*n = 0 ~ 3

WINDOW BASE ADDRESS REGISTER 0 ~ 3

These registers indicate the start byte address offset of the window. Be careful that the value is not a value in the system memory map but the offset to the local memory start address. The value range is 0 to 32 MB.

WMR_0 ~ WMR_3

Name	Address	Description	Type	Reset value
WAR_n	BAR0+a60h +4*n	Base address register for window n	R/W	0

Bits	Name	Description	Reset value
[24:0]	WBA	Window base address	0
[31:25]	–	Reserved	–

*n = 0 ~ 3

BACKGROUND COLOR AND BLINK CONTROL REGISTER

This register specifies the background color, controls the OSG, and controls the cursor enable/disable and blinking.

BCR

Name	Address	Description	Type	Reset value
BCR	BAR0+a80h	Background color/blink control register	R/W	0

Bits	Name	Description	Reset value
[5:0]	CBP	Cursor Blink Period Indicates the cursor blink cycle (6 bits). When set to 0, it is same as blink disable. The cycle range is 1 to 63 (unit: frame). For example, 10 means that the cursor blinks (on and off) every 10 frames.	0
[6]	BLINK_E	Blink Enable 0 = blink disable 1 = blink enable When set to 'Enable (1)', the cursor blinks (on and off) according to the cycle set in the cursor blink period field.	0
[7]	CURSOR_E	Cursor Enable 0 = cursor disable 1 = cursor enable Turns the cursor ON/OFF .	0
[8]	OSG_E	OSG Enable 0 = OSG disable 1 = OSG enable This flag turns on/off all OSG functions. All the OSG functions can be implemented on the screen when this flag is set to 1.	0
[9]	BC_E	Background Color Enable 0 = Uses video on the video layer. 1 = Uses background color instead of the video signal on the video layer.	0
[15:10]	–	Reserved	–
[20:16]	BCR	Background Color (Cr) Indicates the 5-bit Cr value of the background color.	0
[25:21]	BCB	Background Color (Cb) Indicates the 5-bit Cb value of the background color.	0

BCR (Continued)

Bits	Name	Description	Reset value
[31:26]	BCY	Background Color (Y) If there is no video signal or it is not displayed, the background color can be shown instead. YCbCr 655 is used in the color format and this field indicates the 6-bit Y value of YCbCr 655.	0

VIDEO EFFECT CONTROL REGISTER

This register controls whether to use progressive scan for video effects. It also controls the graphic plane order.

VER

Name	Address	Description	Type	Reset value
VER	BAR0+a84h	Video effect register	R/W	0

Bits	Name	Description	Reset value
[8:0]	–	Reserved	–
[9]	PROG_E	Progressive Scan 0 = interlace 1 = progressive Should be set to 1 for progressive video output. Should be set to 0 for interlaced video ouput.	0
[21:10]	–	Reserved	–
[22]	PLANE_O	Plane Order 0 = Graphic over video 1 = Video over graphic	0
[31:23]	–	Reserved	–

PIXEL ALPHA VALUE REGISTER

This register is the alpha-look up table used in the 1-bit pixel blending mode. The 1-bit pixel blending value is used as the index of this table, and converted into a 4-bit blending factor. The 4 look up tables for a window are packed in the 32-bit register.

PAR

Name	Address	Description	Type	Reset value
PAR	BAR0+a8ch	Pixel á value register	R/W	0

Bits	Name	Description	Reset value
[3:0]	PBLDIF1_W3	Pixel blending factor 1 for window3	0
[7:4]	PBLDF0_W3	Pixel blending factor 0 for window3	0
[11:8]	PBLDF1_W2	Pixel blending factor 1 for window2	0
[15:12]	PBLDF0_W2	Pixel blending factor 0 for window2	0
[19:16]	PBLDF1_W1	Pixel blending factor 1 for window1	0
[23:17]	PBLDF0_W1	Pixel blending factor 0 for window1	0
[27:24]	PBLDF1_W0	Pixel blending factor 1 for window0	0
[31:28]	PBLDF0_W0	Pixel blending factor 0 for window0	0

HORIZONTAL CURSOR POSITION CONTROL REGISTER

This register specifies the horizontal start and end points of the cursor. In API, h_start and h_size are input as parameters and h_end is calculated as h_start + h_size. The pixel position on the screen is used as the origin of the coordinates. Because the OSG has an 8-pixel delay to the cursor, 8 is added to compensate the position offset by the OSG.

CHPR

Name	Address	Description	Type	Reset value
CHPR	BAR0+aa4h	Horizontal cursor position register	R/W	0

Bits	Name	Description	Reset value
[10:0]	h_end	Cursor horizontal end point	0
[15:11]	–	Reserved	–
[26:16]	h_start	Cursor horizontal start point	0
[31:27]	–	Reserved	–

VERTICAL CURSOR POSITION CONTROL REGISTER

This register specifies the vertical start and end points of the cursor. In API, v_start and v_size are input as parameters and v_end is calculated as v_start + v_size.

CVPR

Name	Address	Description	Type	Reset value
CVPR	BAR0+aa8h	Vertical cursor position register	R/W	0

Bits	Name	Description	Reset value
[10:0]	v_end	Cursor vertical end point	0
[15:11]	–	Reserved	–
[26:16]	v_start	Cursor vertical start point	0
[31:27]	–	Reserved	–

CURSOR ADDRESS AND SIZE CONTROL REGISTER

This register controls the cursor address in the memory and the cursor's horizontal size.

CASR

Name	Address	Description	Type	Reset value
CASR	BAR0+aach	Cursor address & size register	R/W	0

Bits	Name	Description	Reset value
[24:0]	CBA	Cursor Base Address Base address of the cursor in the memory.	0
[31:25]	CHBS	Cursor Horizontal Byte Size The actual horizontal byte size of the cursor in the memory. Because the cursor can have a maximum 126 -pixel width, the max value is 64 bytes (7 bits).	0

CURSOR COLOR INDEX REGISTERS

These registers are the color loop tables for the cursor. Two colors are packed in a register. A total of 8 registers are used to support 16 colors. The color format is always YCbCr 655.

CASR_n

Name	Address	Description	Type	Reset value
CCR_n	BAR0+ab0h + 4*n	Cursor color register for index n	R/W	0

Bits	Name	Description	Reset value
[4:0]	CE115CR	Cr of Color Entry 1/3/5/7/9/11/13/15	0
[9:5]	CE115CB	Cb of Color Entry 1/3/5/7/9/11/13/15	0
[15:10]	CE115Y	Y of Color Entry 1/3/5/7/9/11/13/15	0
[20:16]	CE114CR	Cr of Color Entry 0/2/4/6/8/10/12/14	0
[25:21]	CE114CB	Cb of Color Entry 0/2/4/6/8/10/12/14	0
[31:26]	CE114Y	Y of Color Entry 0/2/4/6/8/10/12/14	0

*n = 0 ~ 7

GA DESTINATION SIZE CONTROL REGISTER

GA의 destination size.

GA_SIZE

Name	Address	Description	Type	Reset value
GA_SIZE	BAR0+b04h	BLT hor./ver. pixel size register	R/W	0

Bits	Name	Description	Reset value
[11:0]	BLT_H	Block Height Specifies the height (pixel) of the destination block.	0
[15:12]	–	Reserved	–
[27:16]	BLT_W	Block Width Specifies the width (pixel) of the destination block.	0
[31:28]	–	Reserved	–

GA SYSTEM SOURCE SIZE REGISTER

The horizontal byte size of the system source window that contains the block to transfer to the system memory. This value is required so that the H/W can calculate the start address of each line of the block.

GA_CS1_0

Name	Address	Description	Type	Reset value
GA_CS1_0	BAR0+b10h	Source1 BLT mode register in cpu memory	R/W	0

Bits	Name	Description	Reset value
[11:0]	HBS_SW	Horizontal byte size of the source window on system memory.	0
[31:12]	–	Reserved	–

GA SYSTEM SOURCE SIZE REGISTER

Start address of the block to local memory. The address should be an address of byte units in the system memory map. Be careful that, the window base address and the target block coordinate for the target block on the window are specified in order to specify a local memory block, while, the block base address is directly specified in order to specify a system memory block.

GA_CS1_1

Name	Address	Description	Type	Reset value
GA_CS1_1	BAR0+b14h	Source1 BLT start address in cpu memory	R/W	0

Bits	Name	Description	Reset value
[31:0]	BA_SW	Base address of block of the source window on system memory to transfer.	0

GA DESTINATION WINDOW HORIZONTAL SIZE REGISTER

The byte size of the vertical line of the destination window. Because a block transfer is performed against the specified block inside a window and a window varies in the screen area, the horizontal byte size of (not the block but) the window to which the block belongs should be specified in order to know the start address of each line of the block.

GA_DST_0

Name	Address	Description	Type	Reset value
GA_DST_0	BAR0+b30h	Destination BLT mode register in local memory	R/W	0

Bits	Name	Description	Reset value
[11:0]	DHBS	Destination horizontal byte size	0
[31:12]	–	Reserved	–

GA DESTINATION WINDOW BASE ADDRESS REGISTER

Base address of the DST window in the local memory. It is a 128-bit word address. While the system block base address represents the address on the system memory map, it represents the offset to the local memory base address.

GA_DST_1

Name	Address	Description	Type	Reset value
GA_DST_1	BAR0+b34h	Destination window base address in local memory	R/W	0

Bits	Name	Description	Reset value
[20:0]	DSTW_BA	DST window base address	0
[31:21]	–	Reserved	–

GA DESTINATION WINDOW BASE ADDRESS REGISTER

This register represents the vertical start and horizontal start points of the destination block.

GA_DST_2

Name	Address	Description	Type	Reset value
GA_DST_2	BAR0+b38h	Destination BLT start point in local memory	R/W	0

Bits	Name	Description	Reset value
[10:0]	DBVS	Destination Block Vertical Start The y coordinate of the start point (upper left point) of the destination block on the destination window.	0
[15:11]	–	Reserved	–
[26:16]	DBHS	Destination Block Horizontal Start The x coordinate of the start point (upper left point) of the destination block on the destination window.	0
[31:27]	–	Reserved	–

GA FORMAT SELECTION CONROL REGISTER

This register controls the starting of the BitBLT operation. BitBLT starts when a BitBLT format is written to the format flag.

GA_START

Name	Address	Description	Type	Reset value
GA_START	BAR0+ba8h	BLT start register	R/W	0

Bits	Name	Description	Reset value
[0]	BLT_FORMAT	BLT format 0 = 8 bit/pixel 1 = 16 bit/pixel	0
[31:1]	–	Reserved	–

GA RESET CONTROL REGISTER

This register is used to stop the BitBLT operation being performed. For example, in an interactive application, if the BitBLT being performed is too large the operation can be stopped with this register. Once this register is set, the following BitBLT commands are also masked and the BitBLT engine performs no operation and writes the command finish signal to the GA_STAT register. The CPU has the responsibility to clear the GA reset bit once it is set.

GA_RST

Name	Address	Description	Type	Reset value
GA_RST	BAR0+bach	GA reset register	R/W	0

Bits	Name	Description	Reset value
[0]	GA_RST	GA reset	0
[31:1]	–	Reserved	–

GA STATUS REGISTER

This register indicates whether the GA is idle or busy.

GA_STAT

Name	Address	Description	Type	Reset value
GA_STAT	BAR0+bb0h	GA status register	R/W	0

Bits	Name	Description	Reset value
[0]	GA_STAT	GA status 0 = GA idle 1 = GA busy	0
[31:1]	–	Reserved	–

NOTE

8 MMU

8.1 OVERVIEW

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- **Architecture**

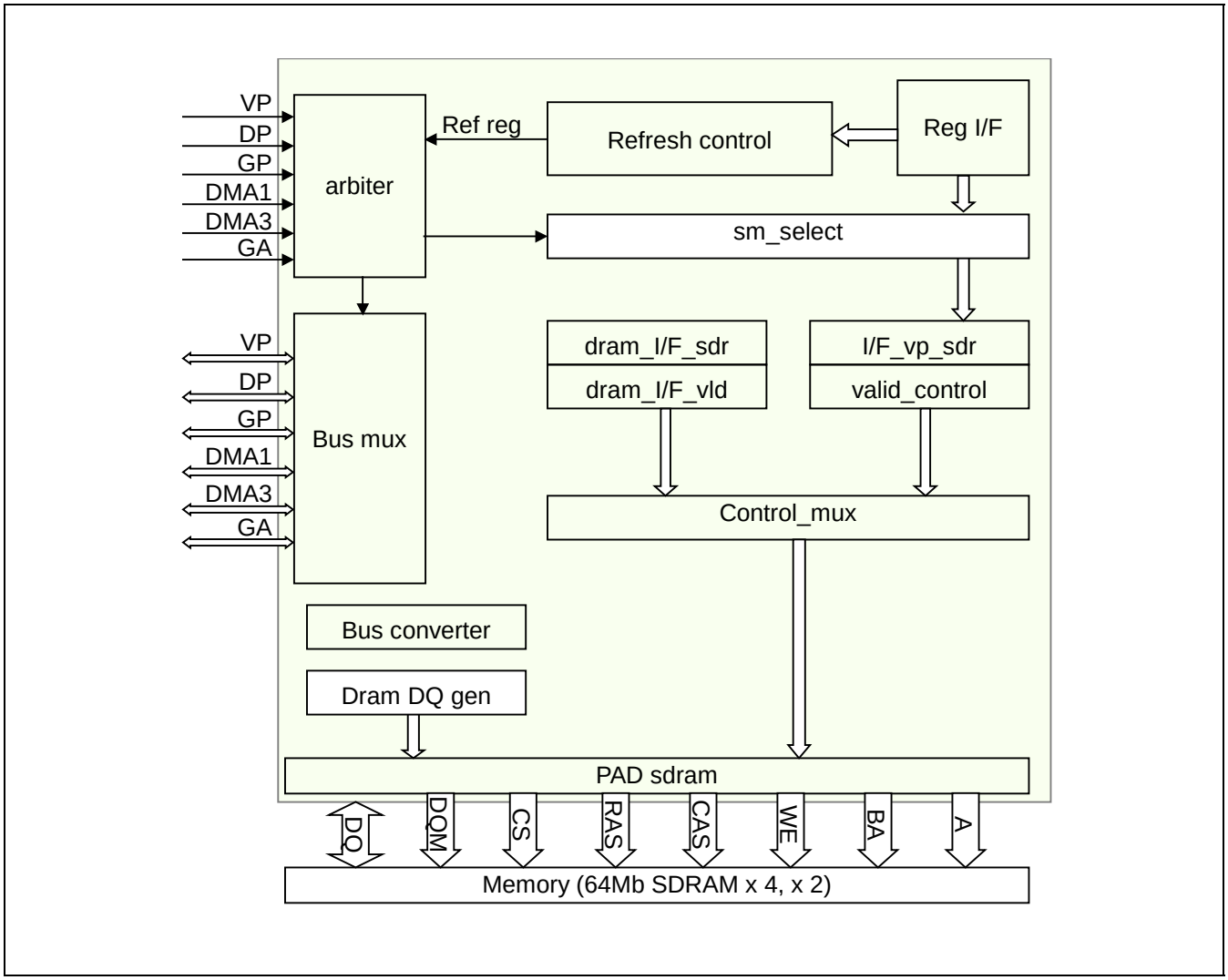

Figure 8-1 MMU diagram

8.2 Feature

- M SDRAM Memory Support (32bit Bus-SDRAM)
- Multiple Memory Configuration Support (x4 and x2 modes supported)
- CAS Latency 3 Support (135MHz target)
- Up to 11 Clients Supported
- Twofold Arbitration Support for Real-Time Service and Non-Real-Time Service
- Guaranteed Maximum Waiting Time (165) Clock

8.3 Operating Flow

SAM2K-Lite MMU uses SDRAM as memory. This memory requires initialization and MMU performs that initialization. During initialization of the memory, the system and the MMU divide the work for which they will take charge. Thus, the system supplies a stable voltage and clock, and when a specific time interval (about 200 usec) has passed the external CPU sets the environment registers inside the MMU and then the MMU performs the remaining initializations.

For SDRAM

1. Supplies the power and clock. CKE="H" (Provided by @System), DQM="H" (@mmu), NOP (@mmu)
2. Supplies stable power and clock (@system); NOP (@mmu)

=> The system sets the mmu_conf_done register. (mmu_reg: 39th register)

3. Pre-Charges all Banks.
4. Auto-Refreshes more than twice.
5. Performs MRS.

BASE ADDRESS REGISTER

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BASE_ADDR_0

Name	Address	Description	Type	Reset value
BASE_ADDR_0	BAR0+c00h	Base address register 0, 1 for MPEG memory 0: MPEG/T/Y/I, 1: MPEG/T/Y/P	R/W	0x000 0x088

Bits	Name	Description	Reset value
[11:0]	M_TYI	MPEG/T/Y/I (12:LSB)	0x000
[23:12]	M_TYP	MPEG/T/Y/P (0:LSB)	0x088
[31:24]	–	Not used	–

BASE ADDRESS REGISTER

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BASE_ADDR_1

Name	Address	Description	Type	Reset value
BASE_ADDR_1	BAR0+c04h	Base address register 2, 3 for MPEG memory 2: MPEG/T/Y/B0, 3: MPEG/T/Y/B1	R/W	0x110 0x198

Bits	Name	Description	Reset value
[11:0]	M_TYB0	MPEG/T/Y/B0 (12:LSB)	0x110
[23:12]	M_TYB1	MPEG/T/Y/B1 (0:LSB)	0x198
[31:24]	–	Not used	–

BASE ADDRESS REGISTER

.

BASE_ADDR_4

Name	Address	Description	Type	Reset value
BASE_ADDR_4	BAR0+c10h	Base address register 8, 9 for MPEG memory 8: MPEG/T/C/I, 9: MPEG/T/C/P	R/W	0x440 0x484

Bits	Name	Description	Reset value
[11:0]	M_TCI	MPEG/T/C/I (12:LSB)	0x440
[23:12]	M_TCP	MPEG/T/C/P (0:LSB)	0x484
[31:24]	–	Not used	–

BASE ADDRESS REGISTER

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BASE_ADDR_5

Name	Address	Description	Type	Reset value
BASE_ADDR_5	BAR0+c14h	Base address register 10, 11 for MPEG memory 10: MPEG/T/C/B0, 11: MPEG/T/C/B1	R/W	0x4C8 0x50C

Bits	Name	Description	Reset value
[11:0]	M_TCB0	MPEG/T/C/B0 (12:LSB)	0x4C8
[23:12]	M_TCB1	MPEG/T/C/B1 (0:LSB)	0x50C
[31:24]	–	Not used	–

BASE ADDRESS REGISTER

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BASE_ADDR_8

Name	Address	Description	Type	Reset value
BASE_ADDR_8	BAR0+c20h	Base address register 16, 17 for MPEG memory 16: MPEG/B/Y/I, 17: MPEG/B/Y/P	R/W	0x220 0x2A8

Bits	Name	Description	Reset value
[11:0]	M_BYI	MPEG/B/Y/I (12:LSB)	0x220
[23:12]	M_BYP	MPEG/B/Y/P (0:LSB)	0x2A8
[31:24]	–	Not used	–

BASE ADDRESS REGISTER

.

BASE_ADDR_9

Name	Address	Description	Type	Reset value
BASE_ADDR_9	BAR0+c24h	Base address register 18, 19 for MPEG memory 18: MPEG/B/Y/B0, 19: MPEG/B/Y/B1	R/W	0x330 0x3B8

Bits	Name	Description	Reset value
[11:0]	M_BYB0	MPEG/B/Y/B0 (12:LSB)	0x330
[23:12]	M_BYB1	MPEG/B/Y/B1 (0:LSB)	0x3B8
[31:24]	–	Not used	–

BASE ADDRESS REGISTER

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BASE_ADDR_12

Name	Address	Description	Type	Reset value
BASE_ADDR_12	BAR0+c30h	Base address register 24, 25 for MPEG memory 24: MPEG/B/C/I, 25: MPEG/B/C/P	R/W	0x550 0x594

Bits	Name	Description	Reset value
[11:0]	M_BCI	MPEG/B/C/I (12:LSB)	0x550
[23:12]	M_BCP	MPEG/B/C/P (0:LSB)	0x594
[31:24]	–	Not used	–

BASE ADDRESS REGISTER

.

BASE_ADDR_13

Name	Address	Description	Type	Reset value
BASE_ADDR_13	BAR0+c34h	Base address register 26, 27 for MPEG memory 26: MPEG/B/C/B0, 27: MPEG/B/C/B1	R/W	0x5d8 0x61C

Bits	Name	Description	Reset value
[11:0]	M_BCB0	MPEG/B/C/B0 (12:LSB)	0x5d8
[23:12]	M_BCB1	MPEG/B/C/B1 (0:LSB)	0x61C
[31:24]	–	Not used	–

BASE ADDRESS REGISTER

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BASE_ADDR_32

Name	Address	Description	Type	Reset value
BASE_ADDR_32	BAR0+c80h	Base address register 64, 65 for DP memory 64: 0x000, 65: external memory 1	R/W	0 0x2C0

Bits	Name	Description	Reset value
[11:0]	EXT_0	External/0 (12:LSB) recommend value : 0x000 absolute base address register of modules except VP,DP	0
[23:12]	EXT_1	External/1 (0:LSB)	0x2C0
[31:24]	–	Not used	–

BASE ADDRESS REGISTER

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BASE_ADDR_33

Name	Address	Description	Type	Reset value
BASE_ADDR_33	BAR0+c84h	Base address register 66, 67 for DP memory 66: external memory 2, 67: external memory 3	R/W	x2ED x31A

Bits	Name	Description	Reset value
[11:0]	EXT_2	External/2 (12:LSB)	x2ED
[23:12]	EXT_3	External/3 (0:LSB)	x31A
[31:24]	–	Not used	–

BASE ADDRESS REGISTER

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BASE_ADDR_34

Name	Address	Description	Type	Reset value
BASE_ADDR_34	BAR0+c88h	Base address register 68, 69 for DP memory 68: external memory 4, 69: external memory 5	R/W	x347 x347

Bits	Name	Description	Reset value
[11:0]	EXT_4	External/4 (12:LSB)	x347
[23:12]	EXT_5	External/5 (0:LSB)	x374
[31:24]	–	Not used	–

BASE ADDRESS REGISTER

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BASE_ADDR_35

Name	Address	Description	Type	Reset value
BASE_ADDR_35	BAR0+c8ch	Base address register 70, 71 for DP memory 70: external memory 6, 71: external memory 7	R/W	0

Bits	Name	Description	Reset value
[11:0]	EXT_6	External/6 (12:LSB)	x3A1
[23:12]	EXT_7	External/7 (0:LSB)	0
[31:24]	–	Not used	–

BASE ADDRESS REGISTER

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BASE_ADDR_36

Name	Address	Description	Type	Reset value
BASE_ADDR_36	BAR0+c90h	Base address register 72, 73 for DP memory 72: external memory 8, 73: external memory 9	R/W	0

Bits	Name	Description	Reset value
[11:0]	EXT_8	External/8 (12:LSB)	0
[23:12]	EXT_9	External/9 (0:LSB)	0
[31:24]	–	Not used	–

BASE ADDRESS REGISTER

.

BASE_ADDR_37

Name	Address	Description	Type	Reset value
BASE_ADDR_37	BAR0+c94h	Base address register 66, 67 for DP memory 74: external memory 10, 75: external memory 11	R/W	0

Bits	Name	Description	Reset value
[11:0]	EXT_10	External/10 (12:LSB)	0
[23:12]	EXT_11	External/11 (0:LSB)	0
[31:24]	–	Not used	–

REFRESH COUNTER REGISTER

.

REFRESH_COUNT

Name	Address	Description	Type	Reset value
REFRESH_COUNT	BAR0+c98h	Refresh Counter	R/W	0x3FF

Bits	Name	Description	Reset value
[10:0]		DRAM Refresh rate count value (64ms/4096=15.6us needed => 15.6us/14.8ns=1054 under, clock needed	0x3FF
[13:11]		SDRAM ADDR Delay Control 0 = 0ns 4 = 4ns 1 = 2ns 5 = 5ns 2 = 2ns, 6 = 6ns 3 = 3ns, 7 = 7ns	0
[16:14]		SDRAM BA Delay Control 0 = 0ns, 4 = 4ns 1 = 2ns, 5 = 5ns 2 = 2ns, 6 = 6ns 3 = 3ns, 7 = 7ns	0
[19:17]		SDRAM CS Delay Control 0 = 0ns, 4: 4ns 1 = 2ns, 5: 5ns 2 = 2ns, 6: 6ns 3 = 3ns, 7: 7ns	0
[31:20]	–	Not used	–

MMU CONFIGURATION REGISTER

.

MMU_CONF

Name	Address	Description	Type	Reset value
MMU_CONF	BAR0+c9ch	MMU Configuration Register	R/W	???

Bits	Name	Description	Reset value
[0]	CONF_DONE	Configuration Done Bit 0 = MMU Configuration is not done. 1 = MMU Configuration is done.	0
[3:1]	RVLDLY	Read Valid Delay Control for Bus Converting 0 = 0ns 4 = 1ns 1 = 2ns 5 = 3ns 2 = 4ns, 6 = 5ns 3 = 6ns, 7 = 7ns	2
[6:4]	DQMDLY	SDRAM DQM Delay Control 0 = 0ns 4 = 1ns 1 = 2ns 5 = 3ns 2 = 4ns, 6 = 5ns 3 = 6ns, 7 = 7ns	0
[9:7]	ENBDLY	SDRAM DQ PAD Enable Delay Control 0 = 0ns 4 = 1ns 1 = 2ns 5 = 3ns 2 = 4ns, 6 = 5ns 3 = 6ns, 7 = 7ns	0
[12:10]	DQODLY	SDRAM DQ Delay Control 0 = 0ns 4 = 1ns 1 = 2ns 5 = 3ns 2 = 4ns, 6 = 5ns 3 = 6ns, 7 = 7ns	0
[15:13]	CTLDLY	SDRAM Control Signal(CKE,CS,RAS,CAS,WE,BA,A) Delay Control 0 = 0ns 4 = 1ns 1 = 2ns 5 = 3ns 2 = 4ns, 6 = 5ns 3 = 6ns, 7 = 7ns	0

MMU_CONF(continued)

Bits	Name	Description	Reset value
[18:16]	CKODLY	SDRAM DQO Latch Clock Delay Control 0 = 0ns 4 = !ck 1 = 1ns 5 = !ck+1ns 2 = 2ns, 6 = !ck+2ns 3 = 3ns, 7 = !ck+3ns	0
[21:19]	CKIDLY	SDRAM DQI Latch Clock Delay Control 0 = 0ns 4 = !ck 1 = 1ns 5 = !ck+1ns 2 = 2ns, 6 = !ck+2ns 3 = 3ns, 7 = !ck+3ns	0
[22]	SZRECOVER	State Machine Size Recovery in case i_XM_sz=0 1: Enable(if sz:0->2), 0: Disable	0
[23]	ARBSEL	Arbiter State-Machine Select 1: Priority-Based 0: FCFS	0
[31:24]	–	Not used	–

REFRESH CYCLE CONTROL REGISTER

.

REF_CYCLE

Name	Address	Description	Type	Reset value
REF_CYCLE	BAR0+ca0h	Refresh Cycle Register	R/W	0xA

Bits	Name	Description	Reset value
[3:0]	Refresh_Cycle_Time	Memory Refresh Cycle Time (tRFC/tCK) (in clock unit) => tRFC:72ns/tCK:7.4ns	0xA
[31:4]	–	Not used	–

HALT LIMIT CONTROL REGISTER

.

HALT_LIMIT

Name	Address	Description	Type	Reset value
HALT_LIMIT	BAR0+ca4h	Halt Limit Register	R/W	0x64

Bits	Name	Description	Reset value
[9:0]	ARBITER_HALT_LIMIT	ARBITER HALT Decision Time (in clock unit)	0x64
[31:10]	–	Not used	–

MMU ERROR STATUS INFORMATION REGISTER

.

MMU_ERR_INFO

Name	Address	Description	Type	Reset value
MMU_ERR_INFO	BAR0+ca8h	MMU Error Status Information Register	R	0

Bits	Name	Description	Reset value
[0]	SM_SEL_ERROR	0 = no error 1 = VP State-Machine Selection Error	0
[1]	ARBITER_HALT	0 = no error 1 = Arbitration Error	0
[5:2]	HALT_INDEX	Arbitration Error Client Index Number	0
[6]	SIZE_ZERO	0 = no error 1 = State Machine Size Zero Error	0
[31:7]	–	Not used	–

NOTE

9 IIC

9.1 OVERVIEW

The S5H2000X has a built-in IIC to enable serial interface with an external source. The IIC supports master transmitter and master receiver modes. The clock receives clock signals from the system clock (67.5MHz) and branches them to the slave.

- **Architecture**

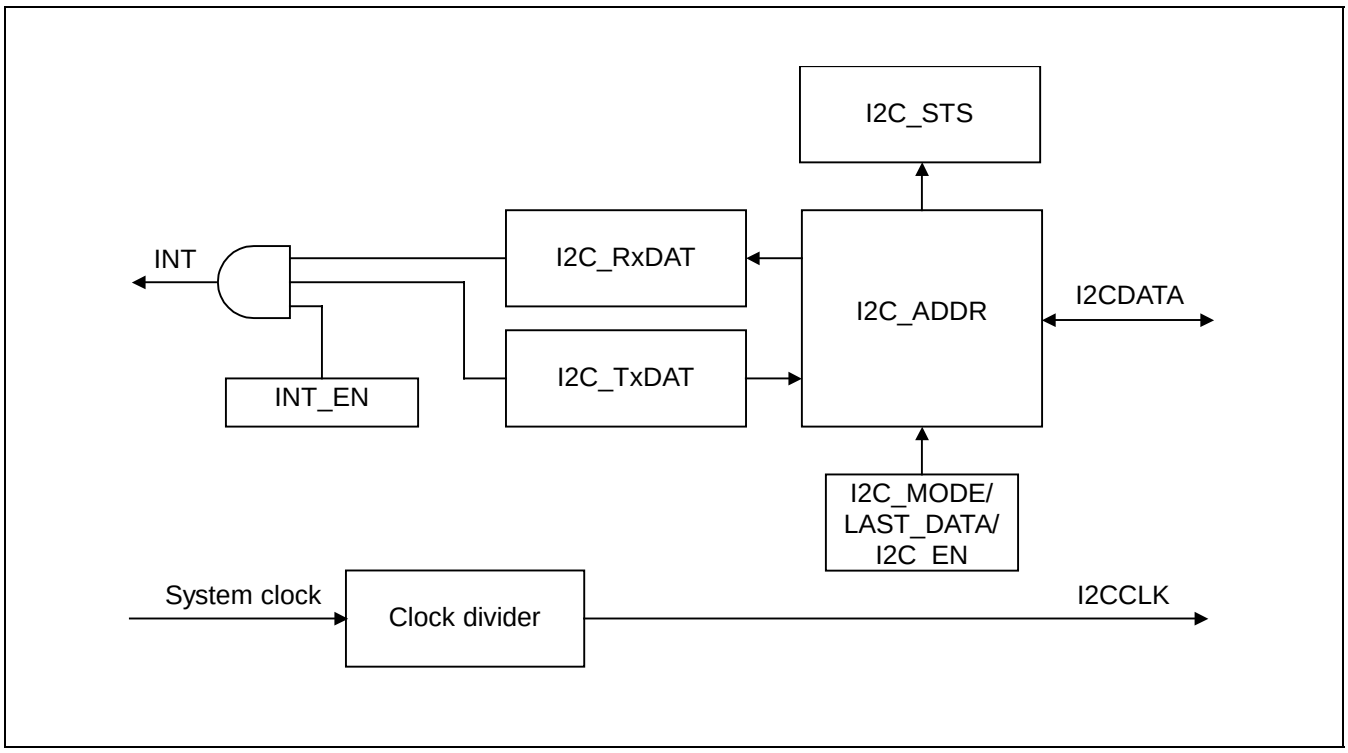

Figure 9-1 IIC block diagram

BASE ADDRESS REGISTER

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BASE_ADDR_0

Name	Address	Description	Type	Reset value
BASE_ADDR_0	BAR0+c00h	Base address register 0, 1 for MPEG memory 0: MPEG/T/Y/I, 1: MPEG/T/Y/P	R/W	0x000 0x088

Bits	Name	Description	Reset value
[11:0]	M_TYI	MPEG/T/Y/I (12:LSB)	0x000
[23:12]	M_TYP	MPEG/T/Y/P (0:LSB)	0x088
[31:24]	–	Not used	–

BASE ADDRESS REGISTER

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BASE_ADDR_1

Name	Address	Description	Type	Reset value
BASE_ADDR_1	BAR0+c04h	Base address register 2, 3 for MPEG memory 2: MPEG/T/Y/B0, 3: MPEG/T/Y/B1	R/W	0x110 0x198

Bits	Name	Description	Reset value
[11:0]	M_TYB0	MPEG/T/Y/B0 (12:LSB)	0x110
[23:12]	M_TYB1	MPEG/T/Y/B1 (0:LSB)	0x198
[31:24]	–	Not used	–

BASE ADDRESS REGISTER

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BASE_ADDR_4

Name	Address	Description	Type	Reset value
BASE_ADDR_4	BAR0+c10h	Base address register 8, 9 for MPEG memory 8: MPEG/T/C/I, 9: MPEG/T/C/P	R/W	0x440 0x484

Bits	Name	Description	Reset value
[11:0]	M_TCI	MPEG/T/C/I (12:LSB)	0x440
[23:12]	M_TCP	MPEG/T/C/P (0:LSB)	0x484
[31:24]	–	Not used	–

BASE ADDRESS REGISTER

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BASE_ADDR_5

Name	Address	Description	Type	Reset value
BASE_ADDR_5	BAR0+c14h	Base address register 10, 11 for MPEG memory 10: MPEG/T/C/B0, 11: MPEG/T/C/B1	R/W	0x4C8 0x50C

Bits	Name	Description	Reset value
[11:0]	M_TCB0	MPEG/T/C/B0 (12:LSB)	0x4C8
[23:12]	M_TCB1	MPEG/T/C/B1 (0:LSB)	0x50C
[31:24]	–	Not used	–

BASE ADDRESS REGISTER

.

BASE_ADDR_8

Name	Address	Description	Type	Reset value
BASE_ADDR_8	BAR0+c20h	Base address register 16, 17 for MPEG memory 16: MPEG/B/Y/I, 17: MPEG/B/Y/P	R/W	0x220 0x2A8

Bits	Name	Description	Reset value
[11:0]	M_BYI	MPEG/B/Y/I (12:LSB)	0x220
[23:12]	M_BYP	MPEG/B/Y/P (0:LSB)	0x2A8
[31:24]	–	Not used	–

BASE ADDRESS REGISTER

.

BASE_ADDR_9

Name	Address	Description	Type	Reset value
BASE_ADDR_9	BAR0+c24h	Base address register 18, 19 for MPEG memory 18: MPEG/B/Y/B0, 19: MPEG/B/Y/B1	R/W	0x330 0x3B8

Bits	Name	Description	Reset value
[11:0]	M_BYB0	MPEG/B/Y/B0 (12:LSB)	0x330
[23:12]	M_BYB1	MPEG/B/Y/B1 (0:LSB)	0x3B8
[31:24]	–	Not used	–

BASE ADDRESS REGISTER

.

BASE_ADDR_12

Name	Address	Description	Type	Reset value
BASE_ADDR_12	BAR0+c30h	Base address register 24, 25 for MPEG memory 24: MPEG/B/C/I, 25: MPEG/B/C/P	R/W	0x550 0x594

Bits	Name	Description	Reset value
[11:0]	M_BCI	MPEG/B/C/I (12:LSB)	0x550
[23:12]	M_BCP	MPEG/B/C/P (0:LSB)	0x594
[31:24]	–	Not used	–

BASE ADDRESS REGISTER

.

BASE_ADDR_13

Name	Address	Description	Type	Reset value
BASE_ADDR_13	BAR0+c34h	Base address register 26, 27 for MPEG memory 26: MPEG/B/C/B0, 27: MPEG/B/C/B1	R/W	0x5d8 0x61C

Bits	Name	Description	Reset value
[11:0]	M_BCB0	MPEG/B/C/B0 (12:LSB)	0x5d8
[23:12]	M_BCB1	MPEG/B/C/B1 (0:LSB)	0x61C
[31:24]	–	Not used	–

BASE ADDRESS REGISTER

.

BASE_ADDR_32

Name	Address	Description	Type	Reset value
BASE_ADDR_32	BAR0+c80h	Base address register 64, 65 for DP memory 64: 0x000, 65: external memory 1	R/W	0 0x2C0

Bits	Name	Description	Reset value
[11:0]	EXT_0	External/0 (12:LSB) recommend value : 0x000 absolute base address register of modules except VP,DP	0
[23:12]	EXT_1	External/1 (0:LSB)	0x2C0
[31:24]	–	Not used	–

BASE ADDRESS REGISTER

.

BASE_ADDR_33

Name	Address	Description	Type	Reset value
BASE_ADDR_33	BAR0+c84h	Base address register 66, 67 for DP memory 66: external memory 2, 67: external memory 3	R/W	x2ED x31A

Bits	Name	Description	Reset value
[11:0]	EXT_2	External/2 (12:LSB)	x2ED
[23:12]	EXT_3	External/3 (0:LSB)	x31A
[31:24]	–	Not used	–

BASE ADDRESS REGISTER

.

BASE_ADDR_34

Name	Address	Description	Type	Reset value
BASE_ADDR_34	BAR0+c88h	Base address register 68, 69 for DP memory 68: external memory 4, 69: external memory 5	R/W	x347 x347

Bits	Name	Description	Reset value
[11:0]	EXT_4	External/4 (12:LSB)	x347
[23:12]	EXT_5	External/5 (0:LSB)	x374
[31:24]	–	Not used	–

BASE ADDRESS REGISTER

.

BASE_ADDR_35

Name	Address	Description	Type	Reset value
BASE_ADDR_35	BAR0+c8ch	Base address register 70, 71 for DP memory 70: external memory 6, 71: external memory 7	R/W	0

Bits	Name	Description	Reset value
[11:0]	EXT_6	External/6 (12:LSB)	x3A1
[23:12]	EXT_7	External/7 (0:LSB)	0
[31:24]	–	Not used	–

BASE ADDRESS REGISTER

.

BASE_ADDR_36

Name	Address	Description	Type	Reset value
BASE_ADDR_36	BAR0+c90h	Base address register 72, 73 for DP memory 72: external memory 8, 73: external memory 9	R/W	0

Bits	Name	Description	Reset value
[11:0]	EXT_8	External/8 (12:LSB)	0
[23:12]	EXT_9	External/9 (0:LSB)	0
[31:24]	–	Not used	–

BASE ADDRESS REGISTER

.

BASE_ADDR_37

Name	Address	Description	Type	Reset value
BASE_ADDR_37	BAR0+c94h	Base address register 66, 67 for DP memory 74: external memory 10, 75: external memory 11	R/W	0

Bits	Name	Description	Reset value
[11:0]	EXT_10	External/10 (12:LSB)	0
[23:12]	EXT_11	External/11 (0:LSB)	0
[31:24]	–	Not used	–

REFRESH COUNTER REGISTER

.

REFRESH_COUNT

Name	Address	Description	Type	Reset value
REFRESH_COUNT	BAR0+c98h	Refresh Counter	R/W	0x3FF

Bits	Name	Description	Reset value
[10:0]		DRAM Refresh rate count value (64ms/4096=15.6us needed => 15.6us/14.8ns=1054 이하 clock needed	0x3FF
[13:11]		SDRAM ADDR Delay Control 0 = 0ns 4 = 4ns 1 = 2ns 5 = 5ns 2 = 2ns, 6 = 6ns 3 = 3ns, 7 = 7ns	0
[16:14]		SDRAM BA Delay Control 0 = 0ns, 4 = 4ns 1 = 2ns, 5 = 5ns 2 = 2ns, 6 = 6ns 3 = 3ns, 7 = 7ns	0
[19:17]		SDRAM CS Delay Control 0 = 0ns, 4: 4ns 1 = 2ns, 5: 5ns 2 = 2ns, 6: 6ns 3 = 3ns, 7: 7ns	0
[31:20]	–	Not used	–

MMU CONFIGURATION REGISTER

.

MMU_CONF

Name	Address	Description	Type	Reset value
MMU_CONF	BAR0+c9ch	MMU Configuration Register	R/W	???

Bits	Name	Description	Reset value
[0]	CONF_DONE	Configuration Done Bit 0 = MMU Configuration is not done. 1 = MMU Configuration is done.	0
[3:1]	RVLDLY	Read Valid Delay Control for Bus Converting 0 = 0ns 4 = 1ns 1 = 2ns 5 = 3ns 2 = 4ns, 6 = 5ns 3 = 6ns, 7 = 7ns	2
[6:4]	DQMDLY	SDRAM DQM Delay Control 0 = 0ns 4 = 1ns 1 = 2ns 5 = 3ns 2 = 4ns, 6 = 5ns 3 = 6ns, 7 = 7ns	0
[9:7]	ENBDLY	SDRAM DQ PAD Enable Delay Control 0 = 0ns 4 = 1ns 1 = 2ns 5 = 3ns 2 = 4ns, 6 = 5ns 3 = 6ns, 7 = 7ns	0
[12:10]	DQODLY	SDRAM DQ Delay Control 0 = 0ns 4 = 1ns 1 = 2ns 5 = 3ns 2 = 4ns, 6 = 5ns 3 = 6ns, 7 = 7ns	0
[15:13]	CTLDLY	SDRAM Control Signal(CKE,CS,RAS,CAS,WE,BA,A) Delay Control 0 = 0ns 4 = 1ns 1 = 2ns 5 = 3ns 2 = 4ns, 6 = 5ns 3 = 6ns, 7 = 7ns	0

MMU_CONF(continued)

Bits	Name	Description	Reset value
[18:16]	CKODLY	SDRAM DQO Latch Clock Delay Control 0 = 0ns 4 = !ck 1 = 1ns 5 = !ck+1ns 2 = 2ns, 6 = !ck+2ns 3 = 3ns, 7 = !ck+3ns	0
[21:19]	CKIDLY	SDRAM DQI Latch Clock Delay Control 0 = 0ns 4 = !ck 1 = 1ns 5 = !ck+1ns 2 = 2ns, 6 = !ck+2ns 3 = 3ns, 7 = !ck+3ns	0
[22]	SZRECOVER	State Machine Size Recovery in case i_XM_sz=0 1: Enable(if sz:0->2), 0: Disable	0
[23]	ARBSEL	Arbiter State-Machine Select 1: Priority-Based 0: FCFS	0
[31:24]	–	Not used	–

REFRESH CYCLE CONTROL REGISTER

.

REF_CYCLE

Name	Address	Description	Type	Reset value
REF_CYCLE	BAR0+ca0h	Refresh Cycle Register	R/W	0xA

Bits	Name	Description	Reset value
[3:0]	Refresh_Cycle_Time	Memory Refresh Cycle Time (tRFC/tCK) (in clock unit) => tRFC:72ns/tCK:7.4ns	0xA
[31:4]	–	Not used	–

HALT LIMIT CONTROL REGISTER

.

HALT_LIMIT

Name	Address	Description	Type	Reset value
HALT_LIMIT	BAR0+ca4h	Halt Limit Register	R/W	0x64

Bits	Name	Description	Reset value
[9:0]	ARBITER_HALT_LIMIT	ARBITER HALT Decision Time (in clock unit)	0x64
[31:10]	–	Not used	–

MMU ERROR STATUS INFORMATION REGISTER

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MMU_ERR_INFO

Name	Address	Description	Type	Reset value
MMU_ERR_INFO	BAR0+ca8h	MMU Error Status Information Register	R	0

Bits	Name	Description	Reset value
[0]	SM_SEL_ERROR	0 = no error 1 = VP State-Machine Selection Error	0
[1]	ARBITER_HALT	0 = no error 1 = Arbitration Error	0
[5:2]	HALT_INDEX	Arbitration Error Client Index Number	0
[6]	SIZE_ZERO	0 = no error 1 = State Machine Size Zero Error	0
[31:7]	–	Not used	–

NOTE

10 AUDIO

AUDIO DMA CONTROL REISTER (PSA0)

.

PCM DMA Source Address Register(LDCR_PSA0)

Name	Address	Description	Type	Reset value
LDCR_PSA0	BAR0+100h	PCI Start Address to read PCM data	R/W	0

Bits	Name	Description	Reset value
[31:0]	PSA0	This is source address for PCM Read-DMA. This is PCI address of system memory.	0

Stream DMA Source Address Register(LDCR_PSA1)

Name	Address	Description	Type	Reset value
LDCR_PSA1	BAR0+104h	PCI Start Address to read STREAM data	R/W	0

Bits	Name	Description	Reset value
[31:0]	PSA1	This is source address for STREAM Read-DMA. This is PCI address of system memory.	0

Transfer Word Count Register for PCM DMA(LDCR_TWC0)

Name	Address	Description	Type	Reset value
LDCR_TWC0	BAR0+108h	Transfer word count register for PCM DMA	R/W	0

Bits	Name	Description	Reset value
[15:0]	TWC0	Word (32bits) data size for PCM	0
[31:16]	–	Reserved	–

Transfer Word Count Register for Stream DMA(LDCR_TWC1)

Name	Address	Description	Type	Reset value
LDCR_TWC1	BAR0+10Ch	Transfer word count register for STREAM DMA	R/W	0

Bits	Name	Description	Reset value
[15:0]	TWC1	Word (32bits) data size for stream	0
[31:16]	–	Reserved	–

AUDIO DMA Auxiliary Control Register(LDCR_AxC)

Name	Address	Description	Type	Reset value
LDCR_AxC	BAR0+110h	Audio DMA auxiliary Control Register	R/W	0

Bits	Name	Description	Reset value
[7:0]	MIN_BS_P	Minimum Block Size for the PCM It is the size of data that the audio DMA requests the PCI bus to transfer. When set to 4, the size of a frame that the PCI transfers is a 4-word unit. If the size of data transferred from the DMA is 64 bytes, LDCR_TWC0 is 16, and MIN_BS_P is 4, the DMA requests the PCI bus 4 times, 4-words at a time. The range of values is 1 ~ 8. The unit is 1 word (4 bytes). This value is cleared to 0 (LDCR_AxC[16]=0) when the DMA operation finishes. Therefore, the user has to write the desired value whenever he starts the DMA.	0
[15:8]	MIN_BS_S	Minimum Block Size for Stream It is the size of data that the audio DMA requests the PCI bus to transfer. When set to 4, the size of a frame that the PCI transfers is a 4-word unit. If the size of data to transmit from the DMA is 64 bytes, LDCR_TWC1 is 16, and MIN_BS_S is 4, the DMA requests the PCI bus 4 times, 4-words at a time. The range of values is 1 ~ 8. The unit is 1 word (4 bytes). This value is cleared to 0 (LDCR_AxC[17]=0) when the DMA operation finishes. Therefore, the user has to write the desired value whenever he starts the DMA.	0
[16]	START_DMA_P	Starts DMA for PCM 0 = Finishes the PCM DMA 1 = Starts and operates the PCM DMA When set to 1, PCM DMA starts. When the DMA operation finishes, it is cleared to 0 automatically.	0

[17]	START_DMA_S	Start DMA for STREAM 0 = Ends or finishes STREAM DMA 1 = Starts and operates STREAM DMA When set to 1, STREAM DMA starts. When the DMA operation finishes, it is cleared to 0 automatically.	0
[31:18]	–	Reserved	–

Transferd Data Size for PCM Register (LDCR_XWC0)

Name	Address	Description	Type	Reset value
LDCR_XWC0	BAR0+114h	Transferred Data Size for PCM	R	0

Bits	Name	Description	Reset value
[15:0]	XWC0	Transferred Word Count Register for PCM (Read-Only) When the total stream DMA transfer size and LDCR_TWC0 are transferred, the transfer size is written to this register. It is read-only and should be read after the DMA operation is finished (LDCR_AxC[16]=0). The transferred size cannot be known during the DMA operation, because it is different from other DMA operations in that the total transfer size is accumulated with each transfer unit.	0
[31:16]	–	Reserved	–

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Transferd Data Size for Stream Register (LDCR_XWC1)

Name	Address	Description	Type	Reset value
LDCR_XWC1	BAR0+118h	Transferred Data Size for stream	R	0

Bits	Name	Description	Reset value
[15:0]	XWC1	Transferred Word Count Register for Stream (Read-Only) When the total stream DMA transfer size and LDCR_TWC1 are transferred, the transfer size is written to this register. It is read-only and should be read after the DMA operation is finished (LDCR_AxC[17]=0). The transferred size cannot be known during the DMA operation, because it is different from other DMA operations in that the total transfer size is accumulated with each transfer unit.	0

[31:16]	–	Reserved	–

Audio DMA Error Status Register(LDCR_ESR)

Name	Address	Description	Type	Reset value
LDCR_ESR	BAR0+11ch	Audio DMA Error Status Register	R	0

Bits	Name	Description	Reset value
[0]	PCM_host1_fatal	host1_fatal for PCM	0
[1]	PCM_host1_perr	host1_perr for PCM	0
[7:2]	–	Reserved	–
[8]	Stream_host1_fatal	host1_fatal for Stream	0
[9]	Stream _host1_perr	host1_perr for Stream	0
[31:10]	–	Reserved	–

AUDIO CONTROL REGISTER

AUDIO IO CONTROL REGISTER (LACR_IO)

Name	Address	Description	Type	Reset value
LACR_IO	BAR0+124h	Audio INOUT Setting Register	R/W	0

These registers set the operation mode of the SAM2K-LITE audio I/F module, including I/O related items.

Bits	Name	Description	Reset value
[0]	SEL_BCLK	Select bclk 0 = 32fs (16-bit output) 1 = 64fs (32-bit output)	0
[1]	SEL_PCM	Select PCM 0 = dec_pcm 1 = ext_pcm	0
[2]	OUT_FORMAT	Output format (to DAC) 0 = I2S 1 = MSB first	0
[3]	IN_FORMAT	Input port (from DAC) 0: I2S 1: MSB first	0
[4]	POLARITY	polarity (input data clocking position) 0 = rising (out at falling) 1 = falling (out at rising)	0
[31:5]	–	Reserved	–

This register controls transfers according to the IEC958 format.

AUDIO VAL CONTROL REGISTER (LACR_VAL)

Name	Address	Description	Type	Reset value
LACR_VAL	BAR0+128h	Audio IEC958 Control Register	R/W	0

This register controls transfers according to IEC958 format.

Bits	Name	Description	Reset value
[0]	SPDIF_O_FORMAT	SPDIF output format: 0 = stream 1 = PCM	0
[3:1]	CD_TYPE	Compressed data type : (Only used Stream format(LACR_VAL[0]=0)) 0 = Pause (Not supported in S5H2000X) 1 = AC-3 2 = MPEG1 (layer-1) 3 = MPEG1 (layer-2, -3), MPEG-2-BC 4 = MPEG2-Extension 5 = MPEG2 (lay1-lsf) 6 = MPEG2 (lay2, lay3-lsf) 7 = Reserved	0
[11:4]	CT_CODE	IEC958 Category Code: This value depends on the equipment type which is set on bit[15:8] of the IEC958 channel status bits (192 bits)	0x00
[27:12]	ES_SIZE	ES size in bits: Burst data length bit	0
[28]	COPY_BIT	IEC958 Copyright Bit: This value is applied to bit[15:8] of the IEC958 channel status bits (192 bits) 0 = Asserted 1 = Not asserted	0
[31:29]	–	Reserved	–

AUDIO STATUS CONTROL REGISTER (LACR_STATUS)

Name	Address	Description	Type	Reset value
LACR_STATUS	BAR0+12ch	Audio Channel Status Register	R	0

This register sets the IEC958 channel status value.

In the consumer mode, frames 0-31 is used and frames 32-191(all 0's) are not used. The value of this register put in the C bit at SPDIF formatting. Please refer to IEC958 spec for more information.

Bits	Name	Description	Reset value
[0]	channel status block	0 = consumer use 1 = professional	0
[1]	audio sample word	0 = linear pcm 1 = non-linear pcm	0
[2]	copyright assertion	0 = copyright 1 = no copyright	0
[5:3]	Data type	000 = digital data or 2ch audio others = don't care	0
[7:6]	mode	00 = mode 0 others = reserved	0
[15:8]	catagory code	00000000 = category code others = don't care	0
[19:16]	source number	0000 = don't care others are the value of source number	0
[23:20]	channel number	0000 = don't care others are the value of source number	0
[27:24]	sampling frequency	Sampling frequency select 0000 = 44.1KHz 0100 = 48KHz 1100 = 32KHz	0
[31:28]	clock accuracy	Clock accuracy select 00 = level 2 01 = level 3 10 = level 1	0

11 INTERRUPT CONTROLLER (Preliminary)

OVERVIEW

Interrupt controller in S5H2000X receives 14 interrupt requests from interrupt sources such as DMA, CPU, etc.

The role of the interrupt controller is to generate interrupt request to the PCI INTA pin out after the arbitration process when there are multiple interrupt requests from internal peripherals and/or external interrupt request pins.

The arbitration process is performed by Interrupt enable logic and the result is written to the interrupt pending register that can be read by the users in the interrupt service routine..

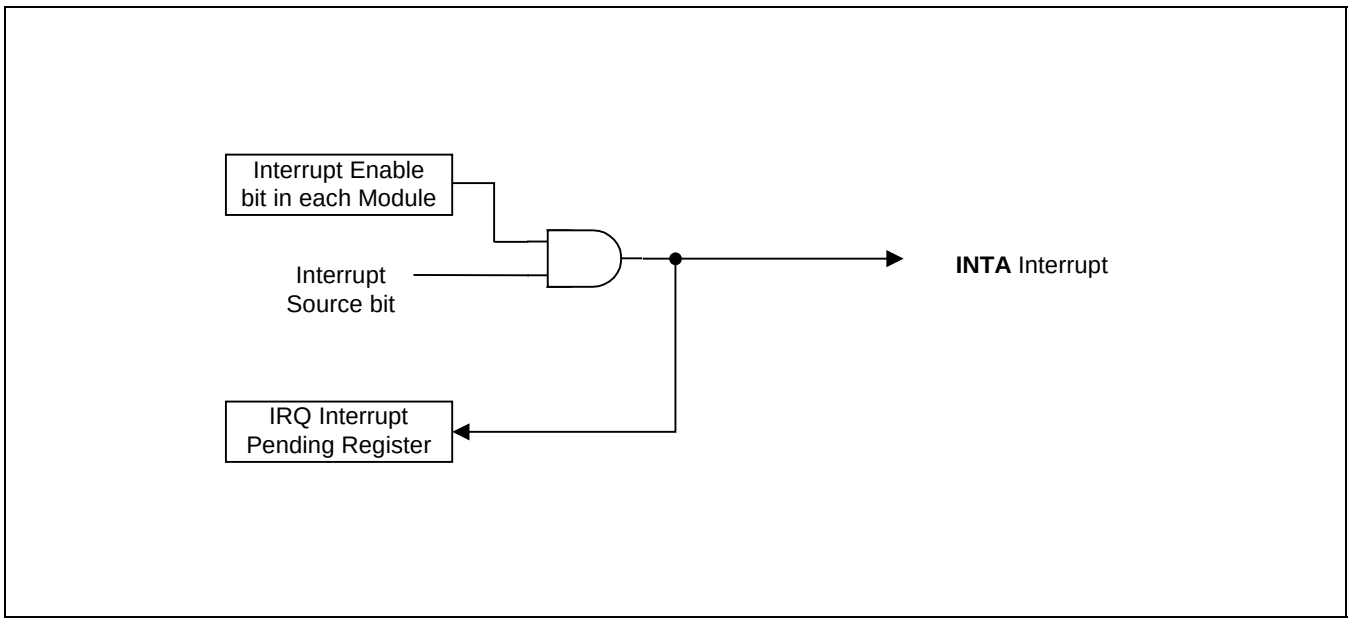


Figure 11-1. Interrupt Controller Block Diagram

INTERRUPT CONTROLLER OPERATION

Interrupt generation

The S5H2000X receives interrupt service by notifying the external CPU of the interrupt generated in inside via the INTA pin. The INTA pin is the way for the PCI device requests to interrupt the host CPU.

CONTROL REGISTERS

There are two control registers in the interrupt controller: enable register**(GSCR_IER)**, and interrupt pending registers(**GSCR_IPCR**).

All the interrupt requests from the interrupt sources are first registered in the source pending register and generate interrupt to INTA pin. There is no Interrupt Mask regiseter, requested interrpt source is directly showed INTA pin. So you can not polling interrupt by interrupt pending regiseter.The details of each control registers are as follows.

INTERRUPT ENABLE REGISTER (GSCR_IER)

Each of the 14 bits in the interrupt enable register is related to an interrupt source. If you clear a specific bit to 0, the interrupt request from the corresponding interrupt source is not serviced by the CPU. If the mask bit is 1, the interrupt request can be serviced.

INTERRUPT PENDING AND CLEAR REGISTER (GSCR_IPCR)

The GSCR_IPCR contain one flag per interrupt (14 total) that indicates an interrupt request has been made by a unit. Inside the interrupt service routine, the GSCR_IPCR are read to determine the interrupt source.

Bits within the IPCR are read only. Once an interrupt has been serviced, the handler clears the pending bit at the interrpt service routine by writing a one to the necessary bit in the source pendign register(GSCR_IPCR).

This is a read-only register.

INTERRUPT SOURCES

Interrupt controller supports 14 interrupt sources as follows table 11-1. User can get to know the interrupt source in the interrupt service routine by reading GSCR_IPCR register.

Table 11-1. Interrupt Source & Corresponding Bit

Corresponding bit	Sources	Descriptions
[0]	EN_SEC_WR_INT	Write-done (pci_ts_dpsram_if : section) interrupt
[1]	EN_AUD_WR_INT	Write-done (pci_ts_dpsram_if : audio) interrupt
[2]	EN_GP_RD_INT	Write-done _1(pci_gp_if) interrupt
[3]	EN_SP_WR_INT	Write-done _0(pci_sp_if) interrupt
[4]	EN_HSMB_WR_INT	Write-done _1(pci_hsmb_if) interrupt
[5]	EN_PCM_RD	Write-done _1(pci_audio_pcm) interrupt
[6]	EN_STM_RD_INT	Write-done (pci_audio_stream) interrupt
[15:7]	–	Reserved
[16]	EN_EXT0	Inform Queue0 that PID filtering data is arrived
[17]	RESERVED	Reserved
[18]	EN_EXT1	Interrupt from ARM7TDMI
[21:19]	–	Reserved
[22]	EN_EXT4	Interrupt from VDMA
[23]	EN_EXT5	Interrupt from VSYNC_EVEN
[24]	EN_EXT6	Interrupt from VSYNC ODD
[25]	EN_EXT7	Interrupt from DP
[26]	EN_EXT8	Interrupt from SP
[31:27]	–	Reserved

INTERRUPT CONTROLLER SEPCIAL REGISTERS

INTERRUPT ENABLE REGISTER (GSCR_IER)

Each of the 14 bits in the interrupt enable register, GSCR_IER, corresponds to an interrupt source (**Refer to Table 11-1**). When a source interrupt enable bit is 0 and the corresponding interrupt event occurs, the interrupt dose not generate interrut request and dose not set interrupt pending and clear regiseter (GSCR_IPCR). If the mask bit is 1, the interrupt generate a request and set interrupt pending and clear regiseter(GSCR_IPCR).

Name	Address	Description	Type	Reset value
GSCR_IER	BAR0+04h	Interrupt Enable Register	R/W	0

Bits	Name	Description	Reset value
[0]	EN_SEC_WR_INT	Enable write-done (pci_ts_dpsram_if : section) interrupt	0
[1]	EN_AUD_WR_INT	Enable write-done (pci_ts_dpsram_if : audio) interrupt	–
[2]	EN_GP_RD_INT	Enable write-done_1(pci_gp_if) interrupt	0
[3]	EN_SP_WR_INT	Enable write-done_0(pci_sp_if) interrupt	0
[4]	EN_HSMB_WR_INT	Enable write-done_1(pci_hsmb_if) interrupt	0
[5]	EN_PCM_RD	Enable write-done_1(pci_audio_pcm) interrupt	0
[6]	EN_STM_RD_INT	Enable write-done (pci_audio_stream) interrupt	0
[15:7]	–	Reserved	–
[16]	EN_EXT0	Queue0에 PID filtering된 data가 도착함을 알려줌	0
[17]	-	Reserved	-
[18]	EN_EXT1	Interrupt from ARM7TDMI	0
[21:19]	-	Reserved	-
[22]	EN_EXT4	Interrupt from VDMA	0
[23]	EN_EXT5	Interrupt from VSYNC_EVEN	0
[24]	EN_EXT6	Interrupt from VSYNC ODD	0
[25]	EN_EXT7	Interrupt from DP	0
[26]	EN_EXT8	Interrupt from SP	0
[31:27]	–	Reserved	–

INTERRUPT PENDING AND CLEAR REGISTER (GSCR_IPCR)

The GSCR_IPCR contain one flag per interrupt (14 total-refer to Table 11-1) that indicates an interrupt request has been made by a unit. Inside the interrupt service routine, the GSCR_IPCR are read to determine the interrupt source.

Name	Address	Description	Type	Reset value
GSCR_IPCR	BAR0+08h	Interrupt Pending & Clear Register	R/W	0

Bits	Name	Description	Reset value
[0]	EN_SEC_WR_INT	Pending & clear (pci_ts_dpsram_if : section) interrupt	0
[1]	EN_AUD_WR_INT	Pending & clear (pci_ts_dpsram_if : audio) interrupt	0
[2]	EN_GP_RD_INT	Pending & clear (pci_gp_if) interrupt	0
[3]	EN_SP_WR_INT	Pending & clear (pci_sp_if) interrupt	0
[4]	EN_HSMB_WR_INT	Pending & clear (pci_hsmb_if) interrupt	0
[5]	EN_PCM_RD	Pending & clear (pci_audio_pcm) interrupt	0
[6]	EN_STM_RD_INT	Pending & clear (pci_audio_stream) interrupt	0
[15:7]	–	Reserved	–
[16]	EN_EXT0	Notification that PID Filtered Data has Arrived at Queue0.	0
[17]	RESERVED	Reserved	0
[18]	EN_EXT1	Pending & clear Interrupt from ARM7TDMI	0
[21:19]	-	Reserved	-
[22]	EN_EXT4	Pending & clear Interrupt from VDMA	0
[23]	EN_EXT5	Pending & clear Interrupt from VSYNC_EVEN	0
[24]	EN_EXT6	Pending & clear Interrupt from VSYNC ODD	0
[25]	EN_EXT7	Pending & clear Interrupt from DP	0
[26]	EN_EXT8	Pending & clear Interrupt from SP	0
[31:27]	–	Reserved	–

R&D SPECIFICATION	
SPEC	S3C2800X

1 PRODUCT OVERVIEW

INTRODUCTION

SAMSUNG's S3C2800X 32-bit RISC microprocessor is designed to provide a cost-effective and high performance micro-controller solution for hand-held devices and general applications. To reduce total system cost, S3C2800X also provides the following: 16KB I/D cache,internal SRAM, 2-ch UART with handshake, 4-ch DMA, System manager (chip select logic, FP/ EDO/SDRAM controller), 3-ch timers, I/O ports, RTC, 2-ch I2C-BUS interface and PLL for clock.

The S3C2800X was developed using a ARM920T core, 0.18 um CMOS standard cells, and a memory compiler. Its low-power, simple, elegant and fully static design is particularly suitable for cost-sensitive and power sensitive applications. Also S3C2800X adopts a new bus architecture, Harvard BUS architecture.

An outstanding feature of the S3C2800X is its CPU core, a 32-bit ARM920T RISC processor (165Mips @150MHz) designed by Advanced RISC Machines, Ltd. The architectural enhancements of ARM920T include the Thumb de-compressor, an on-chip ICE breaker debug support, and a 32-bit hardware multiplier.

By providing a complete set of common system peripherals, the S3C2800X minimizes overall system costs and eliminates the need to configure additional components. The integrated on-chip functions that are described in this document include:

- PCI Host Bridge intrface (32-bit, 33MHz)
- 1.8V Static ARM920T CPU core with 16KB I/D cache . (Harvard bus architecture up to 150MHz)
- External memory controller. (FP/EDO/SDRAM Control, Chip Select logic)
- 4-ch general DMAs with external request pins
- 2-ch UART with handshake (IRDA1.0, 16-byte FIFO) ,Modem Interface
- 2-ch multi-master I2C-BUS controller
- 3-ch 16-bit interval timers
- 16-bit Watch Dog Timer
- 48 general purpose I/O ports / 8-ch external interrupt source
- Power control: Normal, Slow, Idle mode.
- RTC with calendar function.
- On-chip clock generator with PLL.

FEATURES

Architecture

- ARM920T CPU core supports the ARM and Thumb instruction set, core debug,
- Enhanced multiplier, JTAG and the embedded ICE
- Support boundary scan.
- Memory Menagement (support virtual memory)
- Internal AMBA bus architecture (AMBA2.0, AHB/APB)
- Maximum CPU clock frequency 150MHz@1.8v

System Manager

- Little/Big endian support for external memory.
- Internal Special Function Registers(SFRs)are Little endian only.
- Address space: 32Mbytes per each bank. (Total 256Mbyte)
- Supports programmable 8/16/32-bit data bus width for each memory bank.
- All Fixed bank start address(Static memory & Dynamic memory banks)
- 8 memory banks.
  - 4 memory banks for static memory (ROM, SRAM ,FLASH etc).
  - 4 memory banks for Dynamic memory (Fast Page, EDO, and Synchronous DRAM)
- Fully Programmable access cycles for all static memory banks.
- 16-word embedded SRAM.
- Supports external wait signal to expend the bus cycle.
- Supports self-refresh mode in DRAM/SDRAM for power-down.
- Supports asymmetric/symmetric address of DRAM.

I/D Cache Memory

- 64-way set-associative cache with I-Cache(16KB) & D-Cache(16KB)
- 8 words per line with one valid bit and two dirty bits per line
- Pseudo-random or round-robin replacement algorithm
- Write-through and Write-back cache operation.
- The write buffer can hold 16 word of data and four address
- Low voltage cache to reduce power consumption

Clock & Power Manager

- The on-chip PLL generates the necessary clock for the operation of MCU at maximum 150MHz@1.8V.
- Input frequency (Fin) = 4MHz ~ 10MHz.
- Output frequency (Fout) = 20MHz ~ 150MHz.
- Clock can be fed selectively to each function block by software
- Power mode : Normal, Slow, Idle mode
  - Normal mode : Normal operating mode.
  - Slow mode : Low frequency clock without PLL
  - Idle mode : Clock stopping to CPU, only.

PCI Interface

- Internal PCI Host Bridge
- 32-bit data bus / 33MHz

Interrupt Controller

- 29 Interrupt sources
  (3 Timers, 6 UART, 8 External interrupts, 4 DMA ,2 RTC,
  2 I2C, 2 RMT, *2 PCI*).
- Software polling Interrupt mode.
- Level/edge sensitive triggering on the external interrupts source
- Programmable IRQ/FIQ for each interrpt request
- Supports FIQ (Fast Interrupt request) for very urgent interrupt request

Timers

- 3-ch 16 bit interval Timer with DMA-based or interrupt-based operation

Watch-dog Timer

- 16-bit Watchdog Timer

Remocon Receiver

- FIFO 8 steps
- FIFO interrupt is full(8) step overfllow

RTC (Real Time Clock)

- Full clock feature: msec, sec, min, hour, day, week, month, year.
- 32.768 KHz operation.
- Alarm interrupt for CPU wake-up.
- Time tick interrupt

General purpose input/output ports

- 8 external interrupt ports
- 48 multiplexed input/output ports

UART

- 2-channel UART with DMA-based or interrupt based operation
- Supports 5-bit, 6-bit, 7-bit, or 8-bit serial data transmit/receive
- Supports H/W handshaking during transmit/receive
- Programmable baud rates (up to 230.4Kbps)
- Supports IrDA 1.0 (230.4Kbps)
- Loop back mode for testing
- Program accessible 16-byte FIFO (2x16 byte FIFO for transmit/receive data)

DMA Controller

- 4 channel general purpose Direct Memory Access controller without CPU intervention.
- Support IO to memory, memory to IO, IO to IO with the DMA which has 6 type's DMA requestor: Software, 3 internal function blocks (UART0, UART1, Timer), and 2 External pins.
- Burst transfer mode to enhance the transfer rate on the FPDRAM, EDODRAM and SDRAM.

IIC-BUS Interface

- 2-ch Multi-Master I2C-Bus with interrupt-based operation.
- Serial, 8-bit oriented, bi-directional data transfers can be made at up to 100 Kbit/s in the standard mode or up to 400 Kbit/s in the fast mode.

Operating Voltage Range

- Core : 1.8V I/O : 3.0 V to 3.6 V

Operating Frequency

- Up to 150 MHz

Package

- 240 QFP

BLOCK DIAGRAM

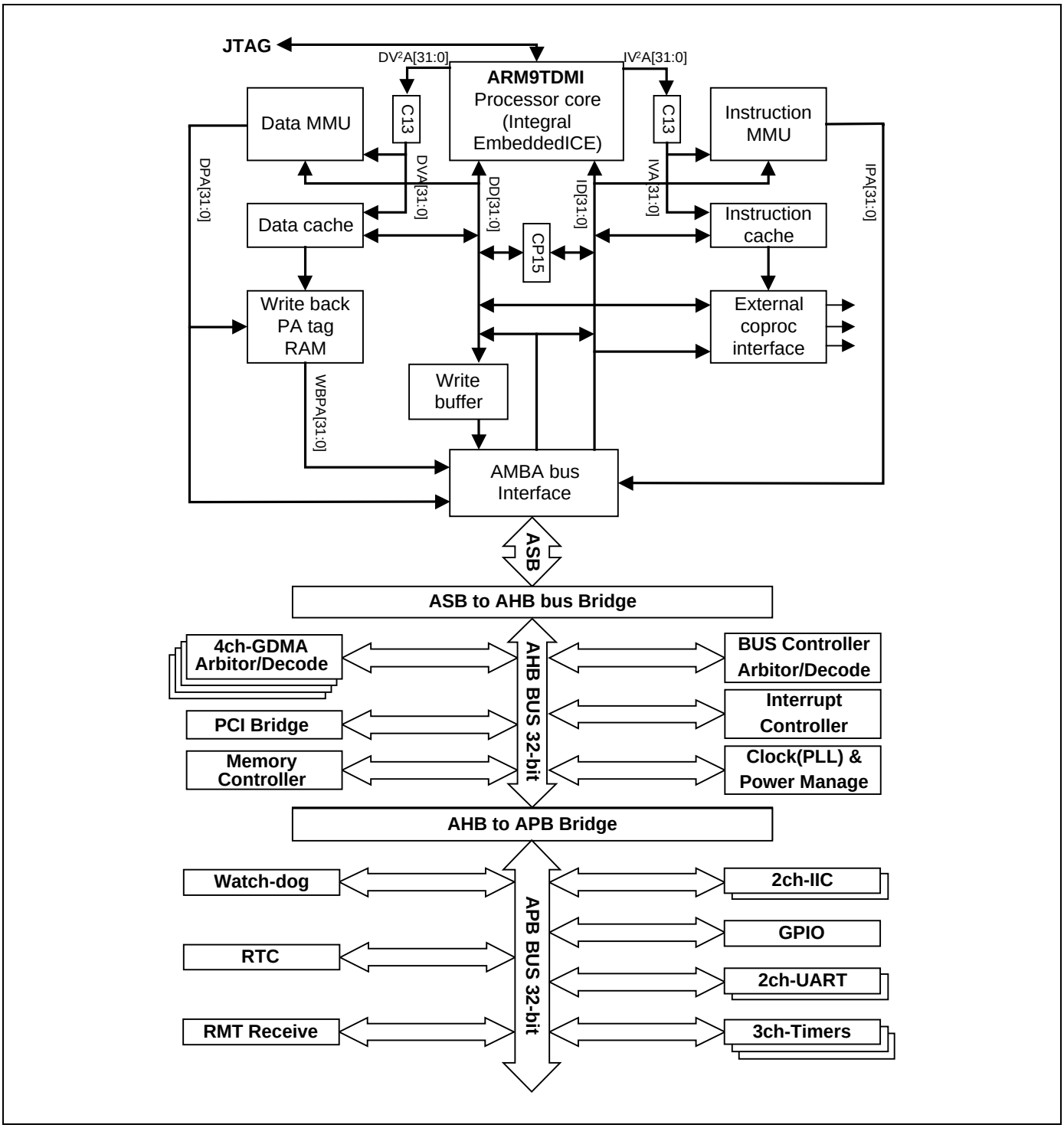


Figure 1-1. S3C2800X Block Diagram

OVERVIEW OF THE ARM920T

The ARM920T is a member of the ARM9 Thumb family of general-purpose microprocessors. The ARM920T is targeted at embedded control applications where high performance, low die size, and low power are all-important. The ARM920T supports both the 32-bit ARM and 16-bit Thumb instruction sets, allowing the user to trade off between high performance and high code density. The ARM920T supports the ARM debug architecture and includes logic to assist in both hardware and software debug. The ARM920T also includes support for coprocessors.

The ARM920T is a Harvard cache architecture processor. The separate instruction and data caches in this design are 16KB each in size, with an 8-word line length. The ARM920T implements an enhanced ARM Architecture V4 MMU to provide translation and access permission checks for instruction and data addresses.

The processor core within ARM920T is an ARM9TDMI. This processor core is a Harvard architecture device implemented using a five-stage pipeline consisting of fetch, decode, execute, memory and write stages, and can be provided as a stand-alone core which can be embedded into more complex devices.

The ARM920T interface to the rest of the system is via unified address and data buses. This interface is scompatible with the *Advanced Microcontroller Bus Architecture* (AMBA) bus scheme. For coprocessor support, the instruction and data buses are exported along with simple handshaking signals. The ARM920T also has a *TrackingICE* mode which allows an approach similar to a conventional ICE mode of operation.

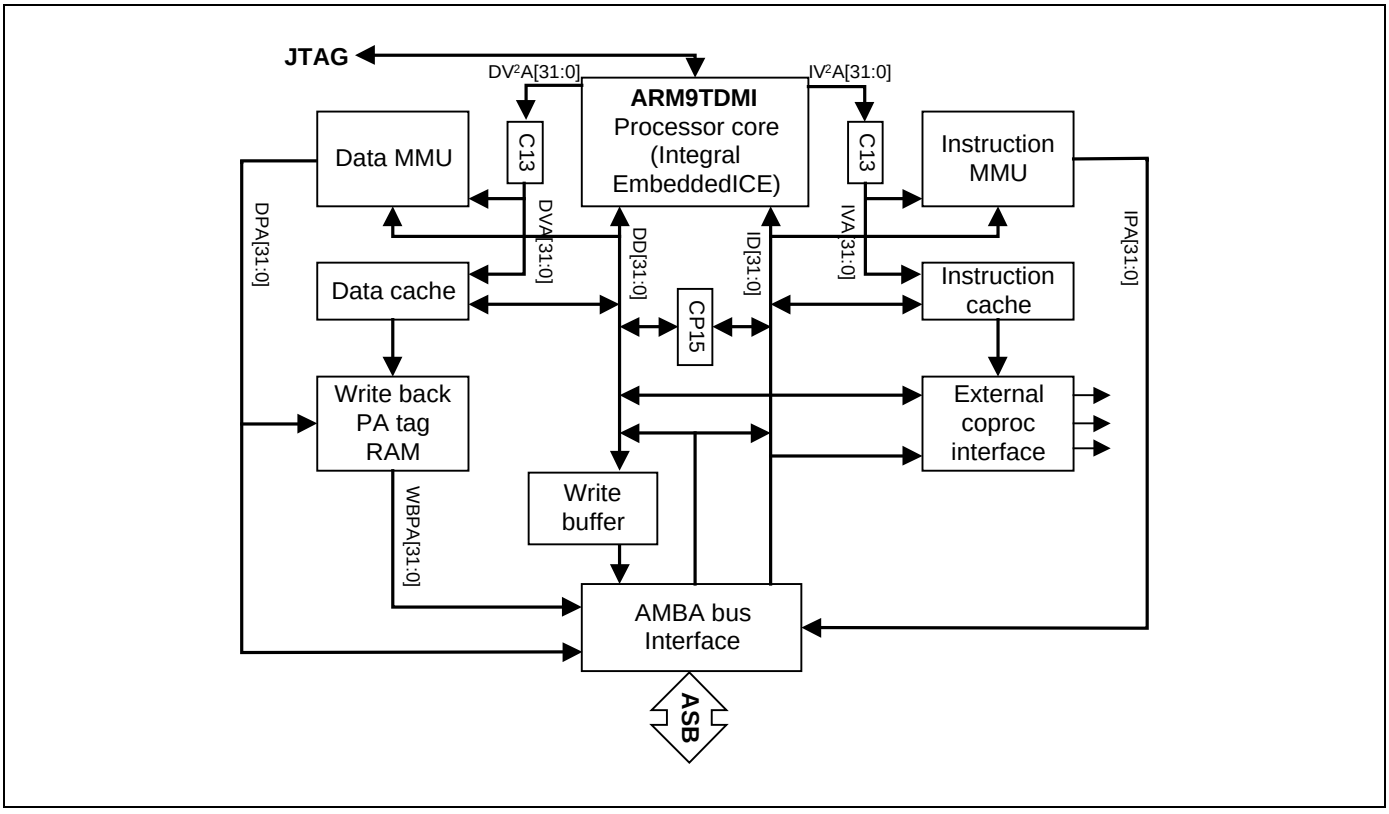


Figure 1-2. ARM920T Functional Block Diagram

PIN ASSIGNMENTS

NOTES :

1. OM[3:0] and ENDIAN value are latched only at the rising edge of nRESET. So, when nRESET is L, the pins of OM[3:0] and ENDIAN are in input state.

2. IICSDA,IICSCL pins are open-drain type.

3. AI/AO means analog input/output.

I/O Type	Descriptions
vdd18i, vss18i	1.8V Vdd/Vss for internal logic
vdd3op, vss3op	3.3V Vdd/Vss for external interface logic
vdd18t, vss18t	1.8V Vdd/Vss for analog circuitry
phsoscm16	Oscillator cell with enable and feedback resister(4M~10MHz)
phbsu50ct12sm	bi-directional pad, CMOS schmit-trigger, 50Kohm pull-up resister with control, tri-state, Io=12mA
phbsu50ct8sm	bi-directional pad, CMOS schmit-trigger, 50Kohm pull-up resister with control, tri-state, Io=8mA
phbsu50cd4sm	bi-directional pad, CMOS schmit-trigger, 50Kohm pull-up resister with control, tri-state, Io=4mA
phot6	output pad, tri-state, Io=6mA
phot8	output pad, tri-state, Io=8mA
phot10	output pad, tri-state, Io=10mA
phis	input pad, CMOS schmitt-trigger
phnc50, phnc50_option	pad for analog pin

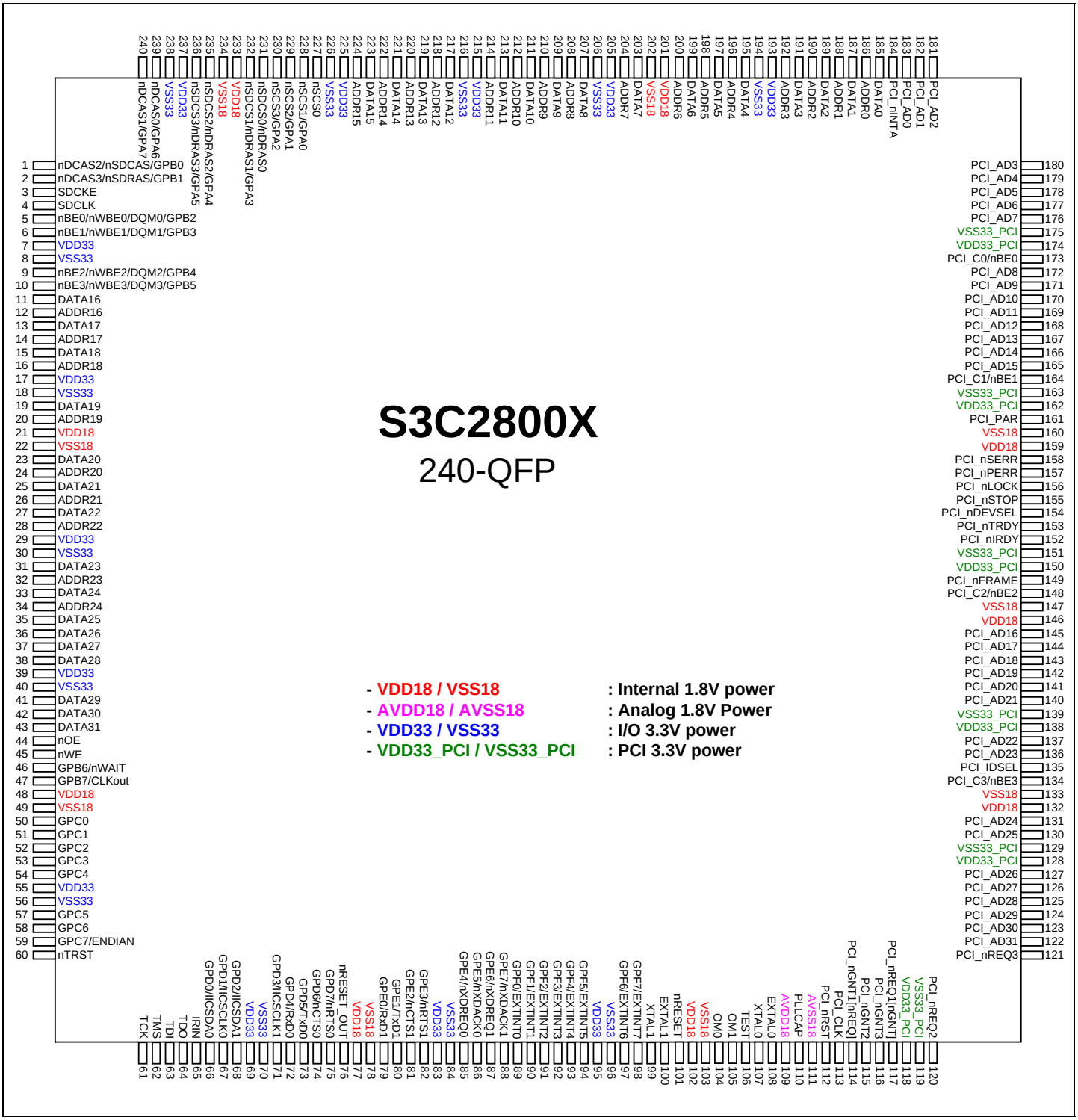


Figure 1-1. S3C2800X Pin Assignment (240-QFP)

SAMSUNG ELECTRONICS

Table 1-1. 240-Pin QFP Pin Assignment

Pin #	Pin Name	Default Function	I/O State @Initial	I/O TYPE(6)
1	nDCAS2/nSDCAS/GPB0	nSDCAS	O/IO	Phbsu50ct8sm
2	nDCAS3/nSDRAS/GPB1	nSDRAS	O/IO	Phbsu50ct8sm
3	SDCKE		O	Phot6
4	SDCLK		O	Phot10
5	nBE0/nWBE0/DQM0/GPB2	DQM0	O/IO	Phbsu50ct8sm
6	nBE1/nWBE1/DQM1/GPB3	DQM1	O/IO	Phbsu50ct8sm
7	VDD33		P	
8	VSS33		P	
9	nBE2/nWBE2/DQM2/GPB4	DQM2	O/IO	Phbsu50ct8sm
10	nBE3/nWBE3/DQM3/GPB5	DQM3	O/IO	Phbsu50ct8sm
11	DATA16		I/O	
12	ADDR16		O	
13	DATA17		I/O	
14	ADDR17		O	
15	DATA18		I/O	
16	ADDR18		O	
17	VDD33		P	
18	VSS33		P	
19	DATA19		I/O	
20	ADDR19		O	
21	VDD18		P	
22	VSS18		P	
23	DATA20		I/O	
24	ADDR20		O	
25	DATA21		I/O	
26	ADDR21		O	
27	DATA22		I/O	
28	ADDR22		O	
29	VDD33		P	
30	VSS33		P	
31	DATA23		I/O	
32	ADDR23		O	
33	DATA24		I/O	

Table 1-1. 240-Pin QFP Pin Assignment (Continued)

Pin #	Pin Name	Default Function	I/O State @Initial	I/O TYPE(6)
34	ADDR24		O	
35	DATA25		I/O	
36	DATA26		I/O	
37	DATA27		I/O	
38	DATA28		I/O	
39	VDD33		P	
40	VSS33		P	
41	DATA29		I/O	
42	DATA30		I/O	
43	DATA31		I/O	
44	nOE		O	Phot8
45	nWE		O	Phot6
46	GPB6/nWAIT	GPB6	IO	Phbsu50ct8sm
47	GPB7/CLKout	GPB7	IO	Phbsu50ct8sm
48	VDD18		P	
49	VSS18		P	
50	GPC0		IO	Phbsu50ct8sm
51	GPC1		IO	Phbsu50ct8sm
52	GPC2		IO	Phbsu50ct8sm
53	GPC3		IO	Phbsu50ct8sm
54	GPC4		IO	Phbsu50ct8sm
55	VDD33		P	
56	VSS33		P	
57	GPC5		IO	Phbsu50ct8sm
58	GPC6		IO	Phbsu50ct8sm
59	GPC7/ENDIAN	ENDIAN	I(1)	Phbsu50ct8sm
60	nTRST		I	Phis
61	TCK		I	Phis
62	TMS		I	Phis
63	TDI		I	Phis
64	TDO		O	Phot6
65	IRIN		I	Phis
66	GPD0/IICSDA0	GPD0	IO(2)	Phbsu50cd4sm

Table 1-1. 240-Pin QFP Pin Assignment (Continued)

Pin #	Pin Name	Default Function	I/O State @Initial	I/O TYPE(6)
67	GPD1/IICSCLK0	GPD1	IO(2)	Phbsu50cd4sm
68	GPD2/IICSDA1	GPD2	IO(2)	Phbsu50cd4sm
69	VDD33		P	
70	VSS33		P	
71	GPD3/IICSCLK1	GPD3	IO(2)	Phbsu50cd4sm
72	GPD4/RxD0	GPD4	IO	Phbsu50ct8sm
73	GPD5/TxD0	GPD5	IO	Phbsu50ct8sm
74	GPD6/nCTS0	GPD6	IO	Phbsu50ct8sm
75	GPD7/nRTS0	GPD7	IO	Phbsu50ct8sm
76	nRESET_OUT		O	Phob10
77	VDD18		P	
78	VSS18		P	
79	GPE0/RxD1	GPE0	IO	Phbsu50ct8sm
80	GPE1/TxD1	GPE1	IO	Phbsu50ct8sm
81	GPE2/nCTS1	GPE2	IO	Phbsu50ct8sm
82	GPE3/nRTS1	GPE3	IO	Phbsu50ct8sm
83	VDD33		P	
84	VSS33		P	
85	GPE4/nXDREQ0	GPE4	IO	Phbsu50ct8sm
86	GPE5/nXDACK0	GPE5	IO	Phbsu50ct8sm
87	GPE6/nXDREQ1	GPE6	IO	Phbsu50ct8sm
88	GPE7/nXDACK1	GPE7	IO	Phbsu50ct8sm
89	GPF0/EXTINT0	GPF0	IO	Phbsu50ct8sm
90	GPF1/EXTINT1	GPF1	IO	Phbsu50ct8sm
91	GPF2/EXTINT2	GPF2	IO	Phbsu50ct8sm
92	GPF3/EXTINT3	GPF3	IO	Phbsu50ct8sm
93	GPF4/EXTINT4	GPF4	IO	Phbsu50ct8sm
94	GPF5/EXTINT5	GPF5	IO	Phbsu50ct8sm
95	VDD33		P	
96	VSS33		P	
97	GPF6/EXTINT6	GPF6	IO	Phbsu50ct8sm
98	GPF7/EXTINT7	GPF7	IO	Phbsu50ct8sm
99	XTAL1		I	Phsosck17

Table 1-1. 240-Pin QFP Pin Assignment (Continued)

Pin #	Pin Name	Default Function	I/O State @Initial	I/O TYPE(6)
100	EXTAL1		O	Phsosck17
101	nRESET		I	Phis
102	VDD18		P	
103	VSS18		P	
104	OM0		I(1)	Phis
105	OM1		I(1)	Phis
106	TEST		I	
107	XTAL0		AI(3)	Phsoscm16
108	EXTAL0		AO(3)	Phsoscm16
109	AVDD18		P	
110	PLLCAP		AI(3)	Phnc50_option
111	AVSS18		P	
112	PCI_nRST		O	
113	PCI_CLK		I	
114	PCI_nGNT1[nREQ]		O	
115	PCI_nGNT2		O	
116	PCI_nGNT3		O	
117	PCI_nREQ1[nGNT]		I	
118	VDD33_PCI		P	
119	VSS33_PCI		P	
120	PCI_nREQ2		I	
121	PCI_nREQ3		I	
122	PCI_AD31		I/O	
123	PCI_AD30		I/O	
124	PCI_AD29		I/O	
125	PCI_AD28		I/O	
126	PCI_AD27		I/O	
127	PCI_AD26		I/O	
128	VDD33_PCI		P	
129	VSS33_PCI		P	
130	PCI_AD25		I/O	
131	PCI_AD24		I/O	
132	VDD18		P	

Table 1-1. 240-Pin QFP Pin Assignment (Continued)

Pin #	Pin Name	Default Function	I/O State @Initial	I/O TYPE(6)
133	VSS18		P	
134	PCI_C3/nBE3		I/O	
135	PCI_IDSEL		I	
136	PCI_AD23		I/O	
137	PCI_AD22		I/O	
138	VDD33_PCI		P	
139	VSS33_PCI		P	
140	PCI_AD21		I/O	
141	PCI_AD20		I/O	
142	PCI_AD19		I/O	
143	PCI_AD18		I/O	
144	PCI_AD17		I/O	
145	PCI_AD16		I/O	
146	VDD18		P	
147	VSS18		P	
148	PCI_C2/nBE2		I/O	
149	PCI_nFRAME		I/O	
150	VDD33_PCI		P	
151	VSS33_PCI		P	
152	PCI_nIRDY		I/O	
153	PCI_nTRDY		I/O	
154	PCI_nDEVSEL		I/O	
155	PCI_nSTOP		I/O	
156	PCI_nLOCK			
157	PCI_nPERR		I/O	
158	PCI_nSERR		I/O	
159	VDD18		P	
160	VSS18		P	
161	PCI_PAR		I/O	
162	VDD33_PCI		P	
163	VSS33_PCI		P	
164	PCI_C1/nBE1		I/O	
165	PCI_AD15		I/O	

Table 1-1. 240-Pin QFP Pin Assignment (Continued)

Pin #	Pin Name	Default Function	I/O State @Initial	I/O TYPE(6)
166	PCI_AD14		I/O	
167	PCI_AD13		I/O	
168	PCI_AD12		I/O	
169	PCI_AD11		I/O	
170	PCI_AD10		I/O	
171	PCI_AD9		I/O	
172	PCI_AD8		I/O	
173	PCI_C0/nBE0		I/O	
174	VDD33_PCI		P	
175	VSS33_PCI		P	
176	PCI_AD7		I/O	
177	PCI_AD6		I/O	
178	PCI_AD5		I/O	
179	PCI_AD4		I/O	
180	PCI_AD3		I/O	
181	PCI_AD2		I/O	
182	PCI_AD1		I/O	
183	PCI_AD0		I/O	
184	PCI_nINTA		O	
185	DATA0		I/O	
186	ADDR0		O	
187	DATA1		I/O	
188	ADDR1		O	
189	DATA2		I/O	
190	ADDR2		O	
191	DATA3		I/O	
192	ADDR3		O	
193	VDD33		P	
194	VSS33		P	
195	DATA4		I/O	
196	ADDR4		O	
197	DATA5		I/O	
198	ADDR5		O	

Table 1-1. 240-Pin QFP Pin Assignment (Continued)

Pin #	Pin Name	Default Function	I/O State @Initial	I/O TYPE(6)
199	DATA6		I/O	
200	ADDR6		O	
201	VDD18		P	
202	VSS18		P	
203	DATA7		I/O	
204	ADDR7		O	
205	VDD33		P	
206	VSS33		P	
207	DATA8		I/O	
208	ADDR8		O	
209	DATA9		I/O	
210	ADDR9		O	
211	DATA10		I/O	
212	ADDR10		O	
213	DATA11		I/O	
214	ADDR11		O	
215	VDD33		P	
216	VSS33		P	
217	DATA12		I/O	
218	ADDR12		O	
219	DATA13		I/O	
220	ADDR13		O	
221	DATA14		I/O	
222	ADDR14		O	
223	DATA15		I/O	
224	ADDR15		O	
225	VDD33		P	
226	VSS33		P	
227	nSCS0		O	Phot8
228	nSCS1/GPA0	nSCS1	O/IO	Phbsu50ct8sm
229	nSCS2/GPA1	nSCS2	O/IO	Phbsu50ct8sm
230	nSCS3/GPA2	nSCS3	O/IO	Phbsu50ct8sm
231	nSDCS0/nDRAS0	nSDCS0	O	Phot8

Table 1-1. 240-Pin QFP Pin Assignment (Continued)

Pin #	Pin Name	Default Function	I/O State @Initial	I/O TYPE(6)
232	nSDCS1/nDRAS1/GPA3	nSDCS1	O/IO	Phbsu50ct8sm
233	VDD18		P	
234	VSS18		P	
235	nSDCS2/nDRAS2/GPA4	nSDCS2	O/IO	Phbsu50ct8sm
236	nSDCS3/nDRAS3/GPA5	nSDCS3	O/IO	Phbsu50ct8sm
237	VDD33		P	
238	VSS33		P	
239	nDCAS0/GPA6	nDCAS0	O/IO	Phbsu50ct8sm
240	nDCAS1/GPA7	nDCAS1	O/IO	Phbsu50ct8sm

SIGNAL DESCRIPTIONS

Table 1-2. S3C2800X Signal Descriptions

Signal	I/O	Description
BUS CONTROLLER		
OM[1:0]	I	OM[1:0] lets S3C2800X be in TEST mode, which is used only at fabrication. Also, It determines the bus width of nGCS0. The logic level is determined by the pull-up/down resistor during the RESET cycle. 00:8-bit 01:16-bit 10:32-bit 11:Test mode
ADDR[24:0]	O	ADDR[24:0] (Address Bus) outputs the memory address of the corresponding bank .
DATA[31:0]	IO	DATA[31:0] (Data Bus) inputs data during memory read and outputs data during memory write. The bus width is programmable among 8/16/32-bit.
nSCS[3:0]	O	nSCS[3:0] (Static memory bank Select) are activated when the address of a memory is within the address region of each bank. The number of access cycles and the bank size can be programmed.
new	O	nWE (Write Enable) indicates that the current bus cycle is a write cycle.
nWBE[3:0]	O	Write Byte Enable
nBE[3:0]	O	16-bit SRAM Byte Enable
nWAIT	I	Request to prolong a current bus cycle. As long as nWAIT is “L”, the current bus cycle can’t be completed.
nOE	O	nOE (Output Enable) indicates that the current bus cycle is a read cycle.
ENDIAN	I	It determines whether or not the data type is little endian or big endian. The logic level is determined by the pull-up/down resistor during the RESET cycle. 0:little endian 1:big endian
DRAM/SDRAM		
nDRAS[3:0]	O	Row Address Strobe
nDCAS[3:0]	O	Column Address strobe
nSDRAS	O	SDRAM Row Address Strobe
nSDCAS	O	SDRAM Column Address Strobe
nSDCS[3:0]	O	SDRAM Chip Select
DQM[3:0]	O	SDRAM Data Mask
SDCLK	O	SDRAM Clock
SDCKE	O	SDRAM Clock Enable
INTERRUPT CONTROL UNIT		
EINT[7:0]	I	External Interrupt request
DMA		
nXDREQ[1:0]	I	External DMA request
nXDACK[1:0]	O	External DMA acknowledge

Table 1-2. S3C2800X Signal Descriptions (Continued)

Signal	I/O	Description
UART		
RxD[1:0]	I	UART receives data input
TxD[1:0]	O	UART transmits data output
nCTS[1:0]	I	UART clear to send input signal
nRTS[1:0]	O	UART request to send output signal
IIC-BUS		
IICSDA[1:0]	IO	IIC-bus data
IICSCL[1:0]	IO	IIC-bus clock
Remote Receive Interrupt		
IRIN	I	Remote Receive interrupt input
GENERAL PORT		
GP[47:0]	IO	General input/output ports (GPA[7:0], GPB[7:0], GPC[3:0], GPD[7:0] , GPE[7:0] , GPF[7:0])
RESET & CLOCK		
nRESET	ST	nRESET suspends any operation in progress and places S3C2800X into a known reset state. For a reset, nRESET must be held to L level for at least 4 SYSCLK after the processor power is stabilized.
nRESET_OUT	O	The nRESET_OUT pin is asserted during hardware reset(POR,nRESET),software reset and watch-dog reset.
XTAL0	AI	Crystal Input for internal osc circuit for system clock. If it isn't used, XTAL0 has to be H level.
EXTAL0	AO	Crystal Output for internal osc circuit for system clock. It is the inverted output of XTAL0. If it isn't used, it has to be a floating pin.
PLLCAP	AI	Loop filter capacitor for system clock PLL. (700pF)
XTAL1	AI	32 KHz crystal input for RTC.
EXTAL1	AO	32 KHz crystal output for RTC. It is the inverted output of XTAL1.

Table 1-2. S3C2800X Signal Descriptions (Continued)

Signal	I/O	Description
JTAG TEST LOGIC		
nTRST	I	nTRST(TAP Controller Reset) resets the TAP controller at start. If debugger is used, A 10K pull-up resister has to be connected. If debugger(black ICE) isn't used, nTRST pin has to be L level or low active pulse.
TMS	I	TMS (TAP Controller Mode Select) controls the sequence of the TAP controller's states. A 10K pull-up resister has to be connected to TMS pin.
TCK	I	TCK (TAP Controller Clock) provides the clock input for the JTAG logic. A 10K pull-up resister has to be connected to TCK pin.
TDI	I	TDI (TAP Controller Data Input) is the serial input for test instructions and data. A 10K pull-up resister has to be connected to TDI pin.
TDO	O	TDO (TAP Controller Data Output) is the serial output for test instructions and data.
POWER		
VDD18	P	S3C2800X core logic VDD (1.8 V)
VSS18	P	S3C2800X core logic VSS
AVDD18	P	S3C2800X Analog logic (PLL loop filter) VDD(1.8V)
AVSS18	P	S3C2800X Analog logic (PLL loop filter) VSS
VDD33	P	S3C2800X I/O port VDD (3.3 V)
VSS33	P	S3C2800X I/O port VSS
VDD33_PCI	P	S3C2800X PCI I/O port VDD (3.3V)
VSS33_PCI	P	S3C2800X PCI I/O port VSS
PCI INTERFACE		
PCI_AD[31:0]	I/O	PCI Address/Data Bus. Multiplexed address and data bus
PCI_C[3:0]/ nBE[3:0]	I/O	PCI C (bus command) or Byte enable
PCI_PAR	I/O	PCI-parity. Parity is even across PCI_AD[31:0] and PCI_C[3:0]/nBE[3:0]. PCI_PAR is valid one cycle after either an address or data phase. The PCI device that drives PCI_AD[31:0] is responsible for driving PCI_PAR on the next PCI bus clock.
PCI_nFRAME	I/O	PCI_nFRAME is driven by the current PCI bus master to indicate beginning and duration of a PCI access.
PCI_nTRDY	I/O	The target of the current PCI transaction drives PCI_nTRDY. Assertion of PCI_nTRDY indicates that the PCI target is ready to transfer data.
PCI_nIRDY	I/O	PCI_nIRDY is driven by the current PCI bus master. Assertion of PC_nIRDY indicates that the PCI initiator is ready to transfer data.
PCI_nSTOP	I/O	The target of the current PCI transaction may assert PCI_nSTOP to indicate to the requesting PCI master that it wants to end the current transaction.
PCI_nDEVSEL	I/O	PCI_nDEVSEL is driven by the target of the current PCI transaction. A PCI target asserts PCI_nDEVSEL when it has decoded an address and command encoding and claims the transaction.

Table 1-2. S3C2800X Signal Descriptions (Continued)

Signal	I/O	Description
PCI_IDSEL	I	PCI_IDSEL is used during configuration cycles to select the PCI slave interface for configuration
PCI_nPERR	I/O	PCI_nPERR is used for reporting data parity errors on PCI transactions. PCI_nPERR is driven active by the device receiving PCI_AD[31:0], PCI_C[3:0]/nBE[3:0], and PCI_PARITY, two PCI clocks following the data in which bad parity is detected.
PCI_nSERR	I/O	PCI_nSERR is used for reporting address parity errors or catastrophic failures detected by a PCI target.
PCI_nREQ1 [nGNT]	I	PCI_nREQ1 when internal arbiter is used or nGNT when external arbiter is used.
PCI_nREQ[3:2]	I	PCI_nREQ[3:2] input when internal arbiter is used. Request indicates to the arbiter that this agent desires use of the bus. This is a point-to-point signal. Every master has its own PCI_nREQ which must be tri-stated while PCI_nRST is asserted.
PCI_nGNT1 [nREQ]	O	PCI_nGNT1 when internal arbiter is used or nREQ when external arbiter is used.
PCI_nGNT[3:2]	O	PCI_nGNT[3:2] output when internal arbiter is used. Grant indicates to the agent that access to the bus has been granted. This is a point-to-point signal. Every master has its own PCI_nGNT which must be ignored while PCI-nRST is asserted.
PCI_CLK	I	PCI_CLK is used as the asynchronous PCI clock when in asynch mode. It is unused when the PCI interface is operated synchronously with the AHB bus.
PCI_nRST	O	PCI specific reset
PCI_nINTA	O	PCI interrupt

Table 1-3. S3C2800X Special Registers

Register Name	Address	R/W	Description	Reset Value
Clock & Power Management				
PLLCON	0x1000 0000	R/W	PLL configuration Register	0x00C0 0002
CLKCON	0x1000 0004	R/W	Clock generator control Register	0x0000 1FFC
CLKSLOW	0x1000 0008	R/W	Slow clock control register	0x0000 0000
LOCKTIME	0x1000 000C	R/W	PLL lock time count register	0x0000 0FFF
SWRCON	0x1000 0010	W	Software reset control register	0x0000 0000
RAMSR	0x1000 0014	R/W	Reset and RTC alarm match status register	0x0000 0001
Reserved	0x1000 0018 ~0x1000 FFFF		Reserved	
Memory Controller				
ENDIAN	0x1001 0000	R	Memory clock & Endian mode control	0x0000 000-
SMBCON0	0x1001 0004	R/W	Bank 0 control register for static memory	0x0000 00A3
SMBCON1	0x1001 0008	R/W	Bank 1 control register for static memory	0x0000 00A3
SMBCON2	0x1001 000C	R/W	Bank 2 control register for static memory	0x0000 00A3
SMBCON3	0x1001 0010	R/W	Bank 3 control register for static memory	0x0000 00A3
REFRESH	0x1001 0014	R/W	DRAM/SDRAM refresh control register	0x00A4 0000
DMTMCON	0x1001 0018	R/W	Timing control for dynamic memory	0x0003 0D50
MRSR	0x1001 001C	R/W	Mode Register Set Register for SDRAM	0x0000 0030
Reserved	0x1001 0020 ~0x1001 FFFF		Reserved	
Interrupt Controller				
SRCPND	0x1002 0000	R/W	Indicates the interrupt request status.	0x0000 0000
INTMOD	0x1002 0004	R/W	Interrupt mode Register	0x0000 0000
INTMSK	0x1002 0008	R/W	Determines which interrupt source is masked.	0x0000 0000
IRQPND	0x1002 000C	R	IRQ interrupt service pending register	0x0000 0000
FIQPND	0x1002 0010	R	FIQ interrupt service pending register	0x0000 0000
Reserved	0x1002 0014 ~0x1002 FFFF		Reserved	

Table 1-3. S3C2800X Special Registers(Continued)

Register Name	Address	R/W	Description	Reset Value
DMA Controller				
DMASRC0	0x1003 0000	R/W	DMA 0 Source address register	0x0000 0000
DMADES0	0x1003 0004	R/W	DMA 0 Destination address register	0x0000 0000
DMACON0	0x1003 0008	R/W	DMA 0 control register	0x0000 0000
DMASTS0	0x1003 000C	R	DMA 0 status register	Undefined
DMACSRC0	0x1003 0010	R	DMA 0 current source address register	Undefined
DMACDES0	0x1003 0014	R	DMA 0 current destination address register	Undefined
MASKTRIG0	0x1003 0018	R/W	DMA 0 mask trigger register	Undefined
Reserved	0x1003 001C ~0x1003 FFFF		Reserved	
DMASRC1	0x1004 0000	R/W	DMA 1 Source address register	0x0000 0000
DMADES1	0x1004 0004	R/W	DMA 1 Destination address register	0x0000 0000
DMACON1	0x1004 0008	R/W	DMA 1 control register	0x0100 0000
DMASTS1	0x1004 000C	R	DMA 1 status register	Undefined
DMACSRC1	0x1004 0010	R	DMA 1 current source address register	Undefined
DMACDES1	0x1004 0014	R	DMA 1 current destination address register	Undefined
MASKTRIG1	0x1004 0018	R/W	DMA 0 mask trigger register	Undefined
Reserved	0x1004 001C ~0x1004 FFFF		Reserved	
DMASRC2	0x1005 0000	R/W	DMA 2 Source address register	0x0000 0000
DMADES2	0x1005 0004	R/W	DMA 2 Destination address register	0x0000 0000
DMACON2	0x1005 0008	R/W	DMA 2 control register	0x0200 0000
DMASTS2	0x1005 000C	R	DMA 2 status register	Undefined
DMACSRC2	0x1005 0010	R	DMA 2 current source address register	Undefined
DMACDES2	0x1005 0014	R	DMA 2 current destination address register	Undefined
MASKTRIG2	0x1005 0018	R/W	DMA 0 mask trigger register	Undefined
Reserved	0x1005 001C ~0x1005 FFFF		Reserved	
DMASRC3	0x1006 0000	R/W	DMA 3 Source address register	0x0000 0000
DMADES3	0x1006 0004	R/W	DMA 3 Destination address register	0x0000 0000
DMACON3	0x1006 0008	R/W	DMA 3 control register	0x0300 0000
DMASTS3	0x1006 000C	R	DMA 3 status register	Undefined
DMACSRC3	0x1006 0010	R	DMA 3 current source address register	Undefined
DMACDES3	0x1006 0014	R	DMA 3 current destination address register	Undefined

Table 1-3. S3C2800X Special Registers(Continued)

Register Name	Address	R/W	Description	Reset Value
MASKTRIG3	0x1006 0018	R/W	DMA 3 mask trigger register	Undefined
Reserved	0x1006 001C ~0x1006 FFFF		Reserved	
PCI Controller				
PCI Register	0x1008 001C ~0x1008 FFFC			
Reserved	0x1009 0000 ~0x100F FFFF			

Table 1-3. S3C2800X Special Registers(Continued)

Register Name	Address	R/W	Description	Reset Value
GPIO Controller				
PCONA	0x1010 0000	R/W	Configures the pins of port A	0x0000 FFFF
PDATA	0x1010 0004	R/W	The data register for port A	Undef.
PUPA	0x1010 0008	R/W	Pull-up disable register for port A	0x0000 0000
PCONB	0x1010 000C	R/W	Configures the pins of port B	0x0000 0FFF
PDATB	0x1010 0010	R/W	The data register for port B	Undef.
PUPB	0x1010 0014	R/W	Pull-up disable register for port B	0x0000 0000
PCONC	0x1010 0018	R/W	Configures the pins of port C	0x0000 0000
PDATC	0x1010 001C	R/W	The data register for port C	Undef.
PUPC	0x1010 0020	R/W	Pull-up disable register for port C	0x0000 0000
PCOND	0x1010 0024	R/W	Configures the pins of port D	0x0000 0000
PDATD	0x1010 0028	R/W	The data register for port D	Undef.
PUPD	0x1010 002C	R/W	Pull-up disable register for port D	0x0000 0000
PCONE	0x1010 0030	R/W	Configures the pins of port E	0x0000 0000
PDATE	0x1010 0034	R/W	The data register for port E	Undef.
PUPE	0x1010 0038	R/W	Pull-up disable register for port E	0x0000 0000
PCONF	0x1010 003C	R/W	Configures the pins of port F	0x0000 0000
PDATF	0x1010 0040	R/W	The data register for port F	Undef.
PUPF	0x1010 0044	R/W	Pull-up disable register for port F	0x0000 0000
EXTINTR	0x1010 0048	R/W	External Interrupt control Register	0x0000 0000
Reserved	0x1010 004C ~0x1010 FFFF		Reserved	
Remote Control Signal Receive Controller				
RRCR	0x1011 0000	R/W	Remocon receiver control register	0x0000 0010
FIFOD	0x1011 0004	R	FIFO Data register	-
Reserved	0x1011 0008 ~0x1011 FFFF		Reserved	
Watch-dog Timer Controller				
WTPSCLR	0x1012 0000	R/W	Watch-dog timer prescaler value Register	0x0000 0080
WTCON	0x1012 0004	R/W	Watch-dog timer control Register	0x0000 0000
WTCNT	0x1012 0008	R	Watch-dog timer count Register	0x0000 0000
Reserved	0x1012 000C ~0x1012 FFFF		Reserved	

Table 1-3. S3C2800X Special Registers(Continued)

Register Name	Address	R/W	Description	Reset Value
Timer Controller				
TMCON0	0x1013 0000	R/W	Timer 0 control register	0x0000 0000
TMDATA0	0x1013 0004	R/W	Timer 0 Data Register	0x0080 FFFF
TMCNT0	0x1013 0008	R	Timer 0 count register	0x0000 FFFF
TMDMASEL	0x1013 000C	R/W	DMA or Interrupt mode selecton register	0x0000 0000
Reserved	0x1013 0010 ~0x1013 FFFF		Reserved	
TMCON1	0x1014 0000	R/W	Timer 1 control register	0x0000 0000
TMDATA1	0x1014 0004	R/W	Timer 1 Data Register	0x0080 FFFF
TMCNT1	0x1014 0008	R	Timer 1 count register	0x0000 FFFF
Reserved	0x1014 000C ~0x1014 FFFF		Reserved	
TMCON2	0x1015 0000	R/W	Timer 2 control register	0x0000 0000
TMDATA2	0x1015 0004	R/W	Timer 2 Data Register	0x0080 FFFF
TMCNT2	0x1015 0008	R	Timer 2 count register	0x0000 FFFF
Reserved	0x1015 000C ~0x1015 FFFF		Reserved	
Real Time Clock Controller				
RTCCON	0x1016 0000	R/W	RTC control Register	0x0000 0000
RTCALM	0x1016 0004	R/W	RTC alarm control Register	0x0000 0000
ALMSEC	0x1016 0008	R/W	Alarm second data Register	0x0000 0000
ALMMIN	0x1016 000C	R/W	Alarm minute data Register	0x0000 0000
ALMHOUR	0x1016 0010	R/W	Alarm hour data Register	0x0000 0000
ALMDAY	0x1016 0014	R/W	Alarm day data Register	0x0000 0001
ALMMON	0x1016 0018	R/W	Alarm month data Register	0x0000 0001
ALMYEAR	0x1016 001C	R/W	Alarm hour data Register	0x0000 0000
BCDSEC	0x1016 0020	R/W	BCD second Register	-
BCDMIN	0x1016 0024	R/W	BCD minute Register	-
BCDHOUR	0x1016 0028	R/W	BCD hour Register	-
BCDDAY	0x1016 002C	R/W	BCD day Register	-
BCDDATE	0x1016 0030	R/W	BCD date Register	-
BCDMON	0x1016 0034	R/W	BCD month Register	-
BCDYEAR	0x1016 0038	R/W	BCD year Register	-
Reserved	0x1016 003C		Reserved	
TICNT	0x1016 0040	R/W	Tick time count Register	0x0000 0000

Table 1-3. S3C2800X Special Registers(Continued)

Register Name	Address	R/W	Description	Reset Value
RTCRST	0x1016 0044	R/W	RTC round reset Register	-
Reserved	0x1016 0044 ~0x1016 FFFF		Reserved	
UART Controller				
ULCON0	0x1017 0000	R/W	UART channel 0 line control register	0x0000 0000
UCON0	0x1017 0004	R/W	UART channel 0 control register	0x0000 0000
UFCON0	0x1017 0008	R/W	UART channel 0 FIFO control register	0x0000 0000
UMCON0	0x1017 000C	R/W	UART channel 0 Modem control register	0x0000 0000
UTRSTAT0	0x1017 0010	R	UART channel 0 Tx/Rx status register	0x0000 0006
UERSTAT0	0x1017 0014	R	UART channel 0 Rx error status register	0x0000 0000
UFSTAT0	0x1017 0018	R	UART channel 0 FIFO status register	0x0000 0000
UMSTAT0	0x1017 001C	R	UART channel 0 Modem status register	0x0000 0000
UTXH0	0x1017 0020(L) 0x1017 0023(B)	W (by byte)	UART channel 0 transmit holding register	-
URXH0	0x1017 0024(L) 0x1017 0027(B)	R (by byte)	UART channel 0 receive buffer register	-
UBRDIV0	0x1017 0028	R/W	Baud rate divisior register 0	0x0000 001A
Reserved	0x1017 002C ~0x1017 FFFF		Reserved	
ULCON1	0x1018 0000	R/W	UART channel 1 line control register	0x0000 0000
UCON1	0x1018 0004	R/W	UART channel 1 control register	0x0000 0000
UFCON1	0x1018 0008	R/W	UART channel 1 FIFO control register	0x0000 0000
UMCON1	0x1018 000C	R/W	UART channel 1 Modem control register	0x0000 0000
UTRSTAT1	0x1018 0010	R	UART channel 1 Tx/Rx status register	0x0000 0006
UERSTAT1	0x1018 0014	R	UART channel 1 Rx error status register	0x0000 0000
UFSTAT1	0x1018 0018	R	UART channel 1 FIFO status register	0x0000 0000
UMSTAT1	0x1018 001C	R	UART channel 1 Modem status register	0x0000 0000
UTXH1	0x1018 0020(L) 0x1018 0023(B)	W (by byte)	UART channel 1 transmit holding register	-
URXH1	0x1018 0024(L) 0x1018 0027(B)	R (by byte)	UART channel 1 receive buffer register	-
UBRDIV1	0x1018 0028	R/W	Baud rate divisior register 1	0x0000 001A
Reserved	0x1018 002C ~0x1018 FFFF		Reserved	

Table 1-3. S3C2800X Special Registers(Continued)

Register Name	Address	R/W	Description	Reset Value
IIC Controller				
IICCON0	0x1019 0000	R/W	IIC-Bus 0 control register	0x0000 0020
IICSTAT0	0x1019 0004	R/W	IIC-Bus 0 control/status register	0x0000 0000
IICADD0	0x1019 0008	R/W	IIC-Bus 0 address register	-
IICDS0	0x1019 000C	R/W	IIC-Bus 0 transmit/receive data shift register	-
Reserved	0x1019 0010 ~0x1019 FFFF		Reserved	
IICCON1	0x101A 0000	R/W	IIC-Bus 1 control register	0x0000 0020
IICSTAT1	0x101A 0004	R/W	IIC-Bus 1 control/status register	0x0000 0000
IICADD1	0x101A 0008	R/W	IIC-Bus 1 address register	-
IICDS1	0x101A 000C	R/W	IIC-Bus 1 transmit/receive data shift register	-
Reserved	0x101A 0010 ~0x101F FFFF		Reserved	
Special Register : 0x1000 0000 ~ 0x101F FFFF (Total 2MByte)				

IMPORTANT NOTES ABOUT S3C44B0X SPECIAL REGISTERS

1. In little endian mode, (L). endian address has to be used. In Big endian mode, (B). endian address has to be used.
2. All registers except UART registers(UTXHn/URXHn) have to be read/written by word unit (32bit) at Little/Big endian.
3. It's very important that the UART registers(UTXHn/URXHn) be read/written by the specified access unit and the specified address. Also, what endian mode is used is carefully considered.
4. The special registers have to be accessed by the word(32-bit) access unit only.
   (To be accessed by LDR/STR or int type pointer(int *)).
5. LDRH/STRH(half-word access) or short int type pointer(short int *) and LDRB/STRB(byte access) or char type pointer(char *) except UART registers(UTXHn/URXHn) have not to be used.

2 PROGRAMMER'S MODEL

ABOUT THE PROGRAMMER'S MODEL

ARM920T incorporates the ARM9TDMI Integer Core, which implements the ARMv4T Architecture. It executes the ARM and Thumb instruction sets, and includes EmbeddedICE JTAG software debug features.

The programmer's model of ARM920T is the programmer's model of ARM9TDMI extended in the following ways:

- The system control coprocessor (CP15), which is integrated within ARM920T, provides additional registers that are used to configure and control the caches, MMU, protection system, and clocking mode of ARM920T.
- The MMU page tables which reside in main memory describe the virtual to physical address mapping, access permissions, and cache and write buffer configuration. These are created by the operating system software and accessed automatically by the ARM920T MMU hardware whenever an access causes a TLB miss.

THE ARM9TDMI PROGRAMMERS MODEL

The ARM9TDMI processor core implements ARM Architechure v4T, and so excutes the ARM 32-bit instruction set and the compressed Thumb 16-bit instruction set.

The ARM v4T architechure specifies a small number of implementation options. The options selected in the ARM9TDMI implementation are listed in the table below. For comparison, the options selected for the ARM7TDMI implementation are also shown.

Table 2-1 ARM9TDMI Implementation option

Processor Core	ARM architecture	Data abort model	Values stored by direct STR, STRT, STM of PC
ARM7TDMI	v4T	Base updated	Address of Inst + 12
ARM9TDMI	v4T	Base restored	Address of Inst + 12

The ARM9TDMI is code compatible with the ARM7TDMI, with two exceptions:

- The ARM9TDMI implements the Base Restored Data Abort model, which significantly simplifies the software data abort handler.
- The ARM9TDMI fully implements the instruction set extension space added to the ARM(32-bit) instruction set in Architeture v4 and v4T.

These differences are explained in more detail below

- **Data abort model**

  The ARM9TDMI implements the Base Restored Data Abort Model, which differs from the Base updated data abort model inplemented by ARM7TDMI.

  The difference in the Data Abort Model affects only a very small section of operating system code, the data abort handler. It does not affect user code. With the Base Restored Data Abort Model, when a data abort exception occurs during the excution of a memory access instruction, the base register is always restored by the processor hardware to the value the register contained before the instruction was excuted. This removes the need for the data abort handler to 'unwind' any base register update which may have been specified by the aborted instruction.

  The Base Restored Data Abort Model significantly simplifies the software data abort handler.

- **Instruction set extension spaces**

  All ARM processors implement the undefined instruction space as one of the entry mechnisms for the Undefined Instruction Exception. That is, ARM instructions with opcode[27:25]=0b011 and opcode[4]=1 are UNDEFINED on all ARM processors including the ARM9TDMI and ARM7TDMI

  ARM Architecture v4 and v4T also introduced a number of instruction set extension space to the ARM instruction set. These are:

  - arithmetic instruction extension space
  - control instruction extension space
  - coprocessor instruction extension space
  - load/store instruction extension space

  Instructions in these space are UNDEFINED (they cause an Undefined Instruction Exception). The ARM9TDMI fully implements all the instruction set extension spaces defined in ARM Architecture v4T as UNDEFINED instructions, allowing emulation of future instruction set additions.

THE ARM920T PROGRAMMERS MODEL

The ARM920T implements uses a five-stage pipeline design. These five stages are:

- instruction fetch (F)
- instruction decode (D)
- execute (E)
- data memory access (M)
- register write (W)

ARM implementations are fully interlocked, so that software will function identically across different implenentations without concern for pipeline effects. Interlock do affect instruction times. For example, the following sequence suffers a single cycle penalty due to a load-use interlock on register r0:

```
LDR     R0,[R7]
ADD     R5,R0,R1
```

PROCESSOR OPERATING STATES

From the programmer's point of view, the ARM920T can be in one of two states:

- ARM state which executes 32-bit, word-aligned ARM instructions.
- *THUMB state* which can execute 16-bit, halfword-aligned THUMB instructions. In this state, the PC uses bit 1 to select between alternate halfwords.

NOTE

Transition between these two states does not affect the processor mode or the contents of the registers.

SWITCHING STATE

Entering THUMB State

Entry into THUMB state can be achieved by executing a BX instruction with the state bit (bit 0) set in the operand register. Transition to THUMB state will also occur automatically on return from an exception (IRQ, FIQ, UNDEF, ABORT, SWI etc.), if the exception was entered with the processor in THUMB state.

Entering ARM State

Entry into ARM state happens:

- On execution of the BX instruction with the state bit clear in the operand register.
- On the processor taking an exception (IRQ, FIQ, RESET, UNDEF, ABORT, SWI etc.). In this case, the PC is placed in the exception mode's link register, and execution commences at the exception's vector address.

MEMORY FORMATS

ARM920T views memory as a linear collection of bytes numbered upwards from zero. Bytes 0 to 3 hold the first stored word, bytes 4 to 7 the second and so on. ARM920T can treat words in memory as being stored either in Big-Endian or Little-Endian format.

BIG-ENDIAN FORMAT

In Big-Endian format, the most significant byte of a word is stored at the lowest numbered byte and the least significant byte at the highest numbered byte. Byte 0 of the memory system is therefore connected to data lines 31 through 24.

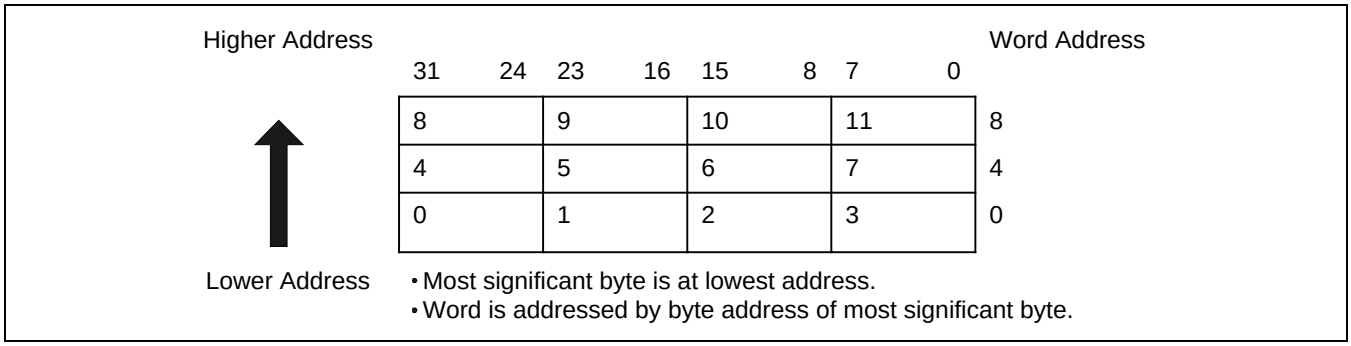


Figure 2-1. Big-Endian Addresses of Bytes within Words

LITTLE-ENDIAN FORMAT

In Little-Endian format, the lowest numbered byte in a word is considered the word's least significant byte, and the highest numbered byte the most significant. Byte 0 of the memory system is therefore connected to data lines 7 through 0.

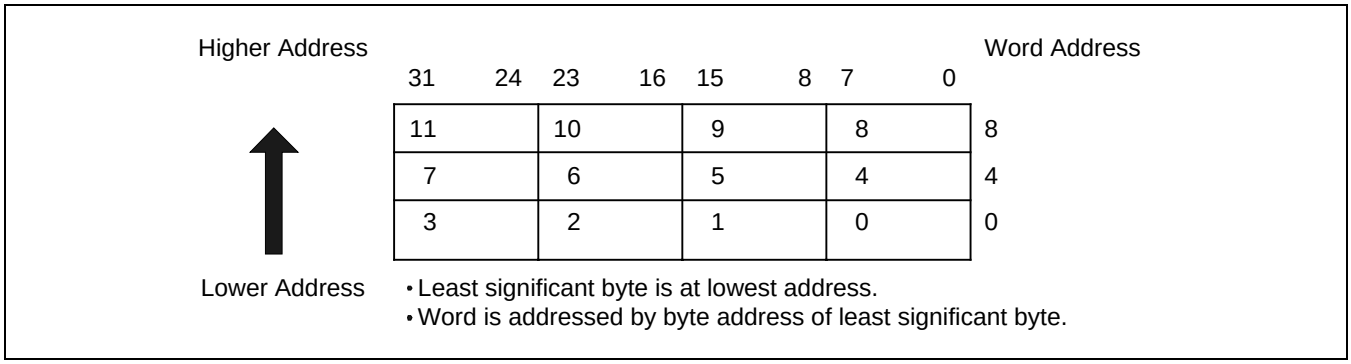


Figure 2-2. Little-Endian Addresses of Bytes whthin Words

INSTRUCTION LENGTH

Instructions are either 32 bits long (in ARM state) or 16 bits long (in THUMB state).

Data Types

ARM920T supports byte (8-bit), halfword (16-bit) and word (32-bit) data types. Words must be aligned to four-byte boundaries and half words to two-byte boundaries.

OPERATING MODES

ARM920T supports seven modes of operation:

- User (usr): The normal ARM program execution state
- FIQ (fiq): Designed to support a data transfer or channel process
- IRQ (irq): Used for general-purpose interrupt handling
- Supervisor (svc): Protected mode for the operating system
- Abort mode (abt): Entered after a data or instruction prefetch abort
- System (sys): A privileged user mode for the operating system
- Undefined (und): Entered when an undefined instruction is executed

Mode changes may be made under software control, or may be brought about by external interrupts or exception processing. Most application programs will execute in User mode. The non-user modes' known as privileged modes-are entered in order to service interrupts or exceptions, or to access protected resources.

REGISTERS

ARM9TDMI has a total of 37 registers - 31 general-purpose 32-bit registers and six status registers - but these cannot all be seen at once. The processor state and operating mode dictate which registers are available to the programmer.

The ARM State Register Set

In ARM state, 16 general registers and one or two status registers are visible at any one time. In privileged (non-User) modes, mode-specific banked registers are switched in. Figure 2-3 shows which registers are available in each mode: the banked registers are marked with a shaded triangle.

The ARM state register set contains 16 directly accessible registers: R0 to R15. All of these except R15 are general-purpose, and may be used to hold either data or address values. In addition to these, there is a seventeenth register used to store status information.

Register 14	is used as the subroutine link register. This receives a copy of R15 when a Branch and Link (BL) instruction is executed. At all other times it may be treated as a general-purpose register. The corresponding banked registers R14_svc, R14_irq, R14_fiq, R14_abt and R14_und are similarly used to hold the return values of R15 when interrupts and exceptions arise, or when Branch and Link instructions are executed within interrupt or exception routines.
Register 15	holds the Program Counter (PC). In ARM state, bits [1:0] of R15 are zero and bits [31:2] contain the PC. In THUMB state, bit [0] is zero and bits [31:1] contain the PC.
Register 16	is the CPSR (Current Program Status Register). This contains condition code flags and the current mode bits.

FIQ mode has seven banked registers mapped to R8-14 (R8_fiq-R14_fiq). In ARM state, many FIQ handlers do not need to save any registers. User, IRQ, Supervisor, Abort and Undefined each have two banked registers mapped to R13 and R14, allowing each of these modes to have a private stack pointer and link registers

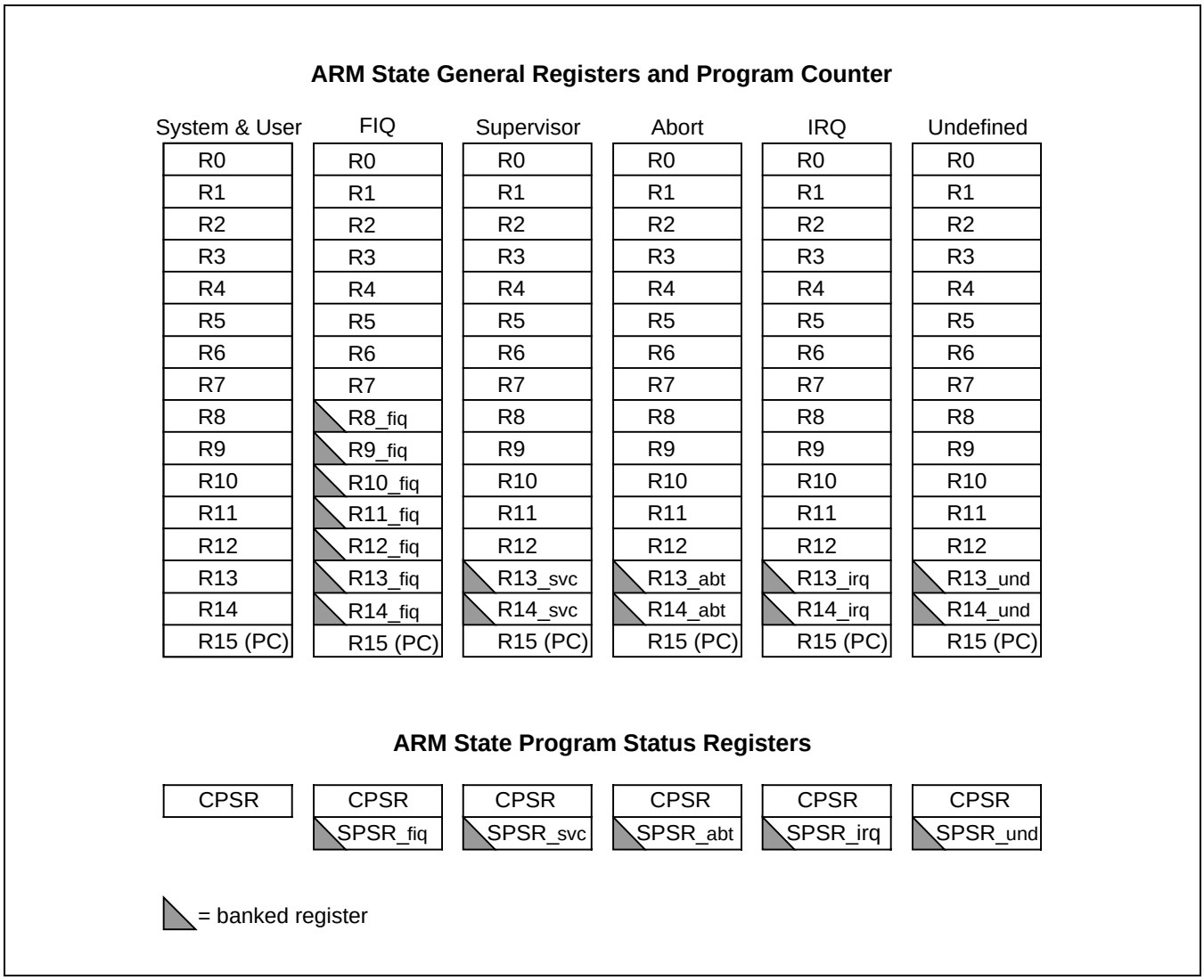


Figure 2-3. Register Organization in ARM State

The THUMB State Register Set

The THUMB state register set is a subset of the ARM state set. The programmer has direct access to eight general registers, R0-R7, as well as the Program Counter (PC), a stack pointer register (SP), a link register (LR), and the CPSR. There are banked Stack Pointers, Link Registers and Saved Process Status Registers (SPSRs) for each privileged mode. This is shown in Figure 2-4.

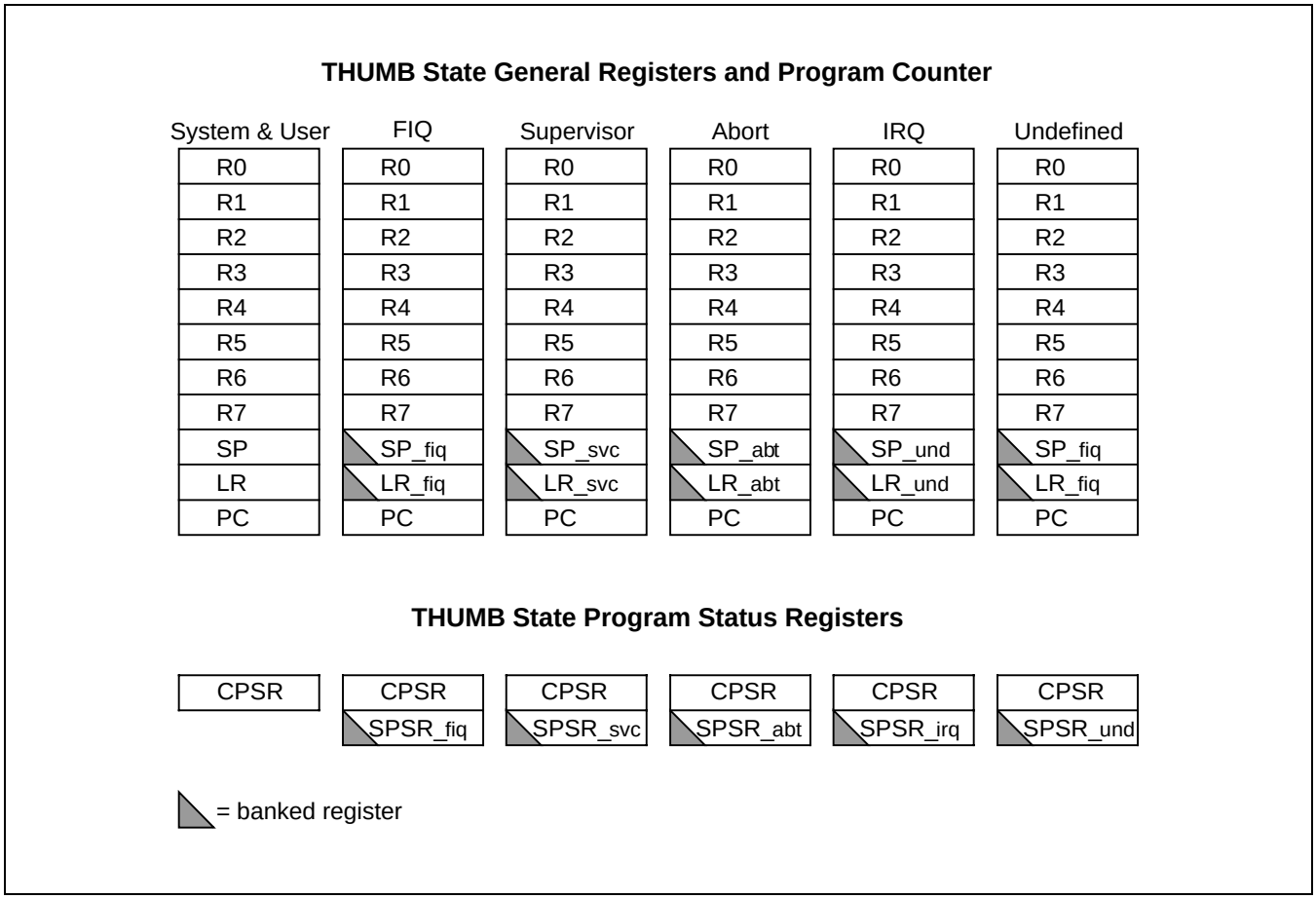


Figure 2-4. Register Organization in THUMB state

The relationship between ARM and THUMB state registers

The THUMB state registers relate to the ARM state registers in the following way:

- THUMB state R0-R7 and ARM state R0-R7 are identical
- THUMB state CPSR and SPSRs and ARM state CPSR and SPSRs are identical
- THUMB state SP maps onto ARM state R13
- THUMB state LR maps onto ARM state R14
- The THUMB state Program Counter maps onto the ARM state Program Counter (R15)

This relationship is shown in Figure 2-5.

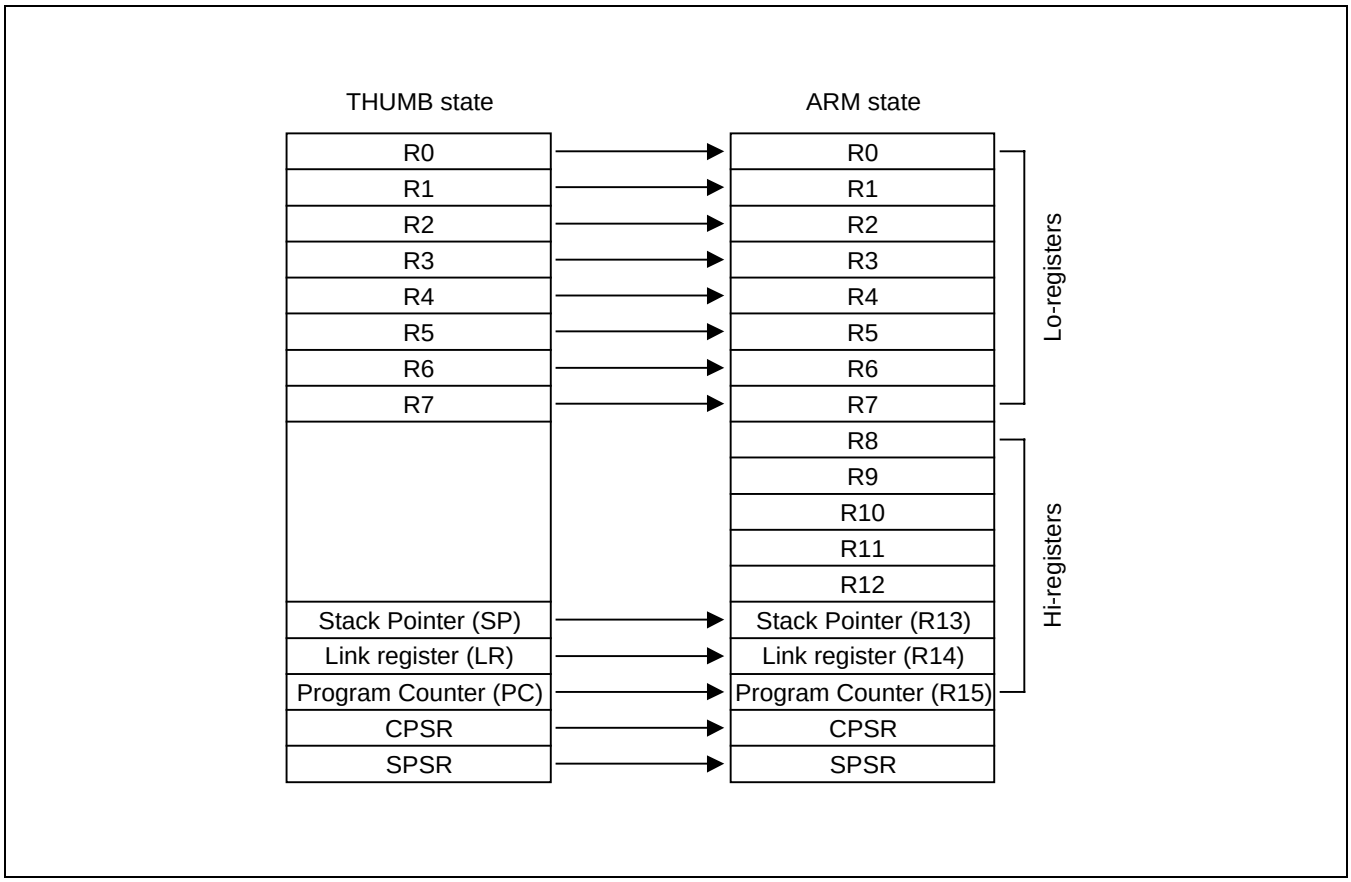


Figure 2-5. Mapping of THUMB State Registers onto ARM State Registers

Accessing Hi-Registers in THUMB State

In THUMB state, registers R8-R15 (the Hi registers) are not part of the standard register set. However, the assembly language programmer has limited access to them, and can use them for fast temporary storage.

A value may be transferred from a register in the range R0-R7 (a Lo register) to a Hi register, and from a Hi register to a Lo register, using special variants of the MOV instruction. Hi register values can also be compared against or added to Lo register values with the CMP and ADD instructions. For more information, refer to Figure 3-34.

THE PROGRAM STATUS REGISTERS

The ARM920T contains a Current Program Status Register (CPSR), plus five Saved Program Status Registers (SPSRs) for use by exception handlers. These register's functions are:

- Hold information about the most recently performed ALU operation
- Control the enabling and disabling of interrupts
- Set the processor operating mode

The arrangement of bits is shown in Figure 2-6.

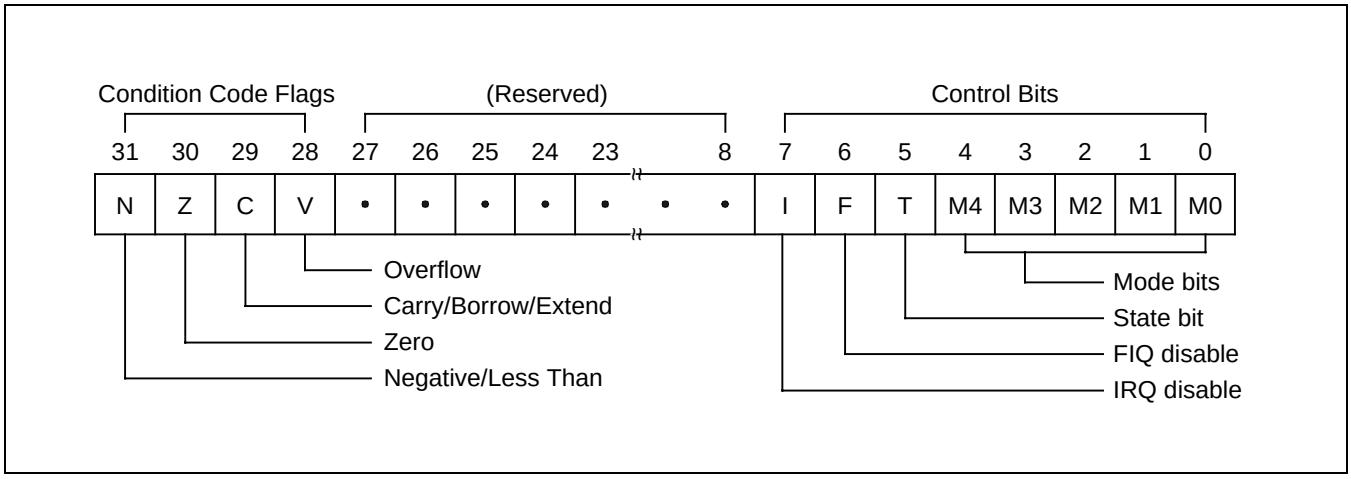


Figure 2-6. Program Status Register Format

The Condition Code Flags

The N, Z, C and V bits are the condition code flags. These may be changed as a result of arithmetic and logical operations, and may be tested to determine whether an instruction should be executed.

In ARM state, all instructions may be executed conditionally: see Table 3-2 for details.

In THUMB state, only the Branch instruction is capable of conditional execution: see Figure 3-46 for details.

The Control Bits

The bottom 8 bits of a PSR (incorporating I, F, T and M[4:0]) are known collectively as the control bits. These will be changed when an exception arises. If the processor is operating in a privileged mode, they can also be manipulated by software.

The T bit	This reflects the operating state. When this bit is set, the processor is executing in THUMB state, otherwise it is executing in ARM state. This is reflected on the **TBIT** external signal. Note that the software must never change the state of the **TBIT** in the CPSR. If this happens, the processor will enter an unpredictable state.
Interrupt disable bits	The I and F bits are the interrupt disable bits. When set, these disable the IRQ and FIQ interrupts respectively.
The mode bits	The M4, M3, M2, M1 and M0 bits (M[4:0]) are the mode bits. These determine the processor's operating mode, as shown in Table 2-1. Not all combinations of the mode bits define a valid processor mode. Only those explicitly described shall be used. The user should be aware that if any illegal value is programmed into the mode bits, M[4:0], then the processor will enter an unrecoverable state. If this occurs, reset should be applied.
Reserved bits	The remaining bits in the PSRs are reserved. When changing a PSR's flag or control bits, you must ensure that these unused bits are not altered. Also, your program should not rely on them containing specific values, since in future processors they may read as one or zero.

Table 2-2. PSR Mode Bit Values

M[4:0]	Mode	Visible THUMB state registers	Visible ARM state registers
10000	User	R7..R0, LR, SP PC, CPSR	R14..R0, PC, CPSR
10001	FIQ	R7..R0, LR_fiq, SP_fiq PC, CPSR, SPSR_fiq	R7..R0, R14_fiq..R8_fiq, PC, CPSR, SPSR_fiq
10010	IRQ	R7..R0, LR_irq, SP_irq PC, CPSR, SPSR_irq	R12..R0, R14_irq, R13_irq, PC, CPSR, SPSR_irq
10011	Supervisor	R7..R0, LR_svc, SP_svc, PC, CPSR, SPSR_svc	R12..R0, R14_svc, R13_svc, PC, CPSR, SPSR_svc
10111	Abort	R7..R0, LR_abt, SP_abt, PC, CPSR, SPSR_abt	R12..R0, R14_abt, R13_abt, PC, CPSR, SPSR_abt
11011	Undefined	R7..R0 LR_und, SP_und, PC, CPSR, SPSR_und	R12..R0, R14_und, R13_und, PC, CPSR
11111	System	R7..R0, LR, SP PC, CPSR	R14..R0, PC, CPSR

Reserved bits — The remaining bits in the PSR's are reserved. When changing a PSR's flag or control bits, you must ensure that these unused bits are not altered. Also, your program should not rely on them containing specific values, since in future processors they may read as one or zero.

EXCEPTIONS

Exceptions arise whenever the normal flow of a program has to be halted temporarily, for example to service an interrupt from a peripheral. Before an exception can be handled, the current processor state must be preserved so that the original program can resume when the handler routine has finished.

It is possible for several exceptions to arise at the same time. If this happens, they are dealt with in a fixed order. See Exception Priorities on page 2-14.

Action on Entering an Exception

When handling an exception, the ARM920T:

1. Preserves the address of the next instruction in the appropriate Link Register. If the exception has been entered from ARM state, then the address of the next instruction is copied into the Link Register (that is, current PC + 4 or PC + 8 depending on the exception. See Table 2-2 on for details). If the exception has been entered from THUMB state, then the value written into the Link Register is the current PC offset by a value such that the program resumes from the correct place on return from the exception. This means that the exception handler need not determine which state the exception was entered from. For example, in the case of SWI, MOVS PC, R14_svc will always return to the next instruction regardless of whether the SWI was executed in ARM or THUMB state.
2. Copies the CPSR into the appropriate SPSR
3. Forces the CPSR mode bits to a value which depends on the exception
4. Forces the PC to fetch the next instruction from the relevant exception vector

It may also set the interrupt disable flags to prevent otherwise unmanageable nestings of exceptions.

If the processor is in THUMB state when an exception occurs, it will automatically switch into ARM state when the PC is loaded with the exception vector address.

Action on Leaving an Exception

On completion, the exception handler:

1. Moves the Link Register, minus an offset where appropriate, to the PC. (The offset will vary depending on the type of exception.)
2. Copies the SPSR back to the CPSR
3. Clears the interrupt disable flags, if they were set on entry

NOTE

An explicit switch back to THUMB state is never needed, since restoring the CPSR from the SPSR automatically sets the T bit to the value it held immediately prior to the exception.

Exception Entry/Exit Summary

Table 2-2 summarises the PC value preserved in the relevant R14 on exception entry, and the recommended instruction for exiting the exception handler.

Table2-2. Exception Entry/Exit

	Return Instruction	Previous State		Notes
		ARM R14_x	THUMB R14_x	
BL	MOV PC, R14	PC + 4	PC + 2	1
SWI	MOVS PC, R14_svc	PC + 4	PC + 2	1
UDEF	MOVS PC, R14_und	PC + 4	PC + 2	1
FIQ	SUBS PC, R14_fiq, #4	PC + 4	PC + 4	2
IRQ	SUBS PC, R14_irq, #4	PC + 4	PC + 4	2
PABT	SUBS PC, R14_abt, #4	PC + 4	PC + 4	1
DABT	SUBS PC, R14_abt, #8	PC + 8	PC + 8	3
RESET	NA	-	-	4

NOTES:

1. Where PC is the address of the BL/SWI/Undefined Instruction fetch which had the prefetch abort.
2. Where PC is the address of the instruction which did not get executed since the FIQ or IRQ took priority.
3. Where PC is the address of the Load or Store instruction which generated the data abort.
4. The value saved in R14_svc upon reset is unpredictable.

FIQ

The FIQ (Fast Interrupt Request) exception is designed to support a data transfer or channel process, and in ARM state has sufficient private registers to remove the need for register saving (thus minimising the overhead of context switching).

FIQ is externally generated by taking the **nFIQ** input LOW. This input can except either synchronous or asynchronous transitions, depending on the state of the **ISYNC** input signal. When **ISYNC** is LOW, **nFIQ** and **nIRQ** are considered asynchronous, and a cycle delay for synchronization is incurred before the interrupt can affect the processor flow.

Irrespective of whether the exception was entered from ARM or Thumb state, a FIQ handler should leave the interrupt by executing

```
SUBS    PC,R14_fiq,#4
```

FIQ may be disabled by setting the CPSR's F flag (but note that this is not possible from User mode). If the F flag is clear, ARM920T checks for a LOW level on the output of the FIQ synchroniser at the end of each instruction.

IRQ

The IRQ (Interrupt Request) exception is a normal interrupt caused by a LOW level on the **nIRQ** input. IRQ has a lower priority than FIQ and is masked out when a FIQ sequence is entered. It may be disabled at any time by setting the I bit in the CPSR, though this can only be done from a privileged (non-User) mode.

Irrespective of whether the exception was entered from ARM or Thumb state, an IRQ handler should return from the interrupt by executing

```
SUBS    PC,R14_irq,#4
```

Abort

An abort indicates that the current memory access cannot be completed. It can be signalled by the external **ABORT** input. ARM920T checks for the abort exception during memory access cycles.

There are two types of abort:

- *Prefetch abort:* occurs during an instruction prefetch.
- *Data abort:* occurs during a data access.

If a prefetch abort occurs, the prefetched instruction is marked as invalid, but the exception will not be taken until the instruction reaches the head of the pipeline. If the instruction is not executed - for example because a branch occurs while it is in the pipeline - the abort does not take place.

If a data abort occurs, the action taken depends on the instruction type:

- Single data transfer instructions (LDR, STR) write back modified base registers: the Abort handler must be aware of this.
- The swap instruction (SWP) is aborted as though it had not been executed.
- Block data transfer instructions (LDM, STM) complete. If write-back is set, the base is updated. If the instruction would have overwritten the base with data (ie it has the base in the transfer list), the overwriting is prevented. All register overwriting is prevented after an abort is indicated, which means in particular that R15 (always the last register to be transferred) is preserved in an aborted LDM instruction.

The abort mechanism allows the implementation of a demand paged virtual memory system. In such a system the processor is allowed to generate arbitrary addresses. When the data at an address is unavailable, the Memory Management Unit (MMU) signals an abort. The abort handler must then work out the cause of the abort, make the requested data available, and retry the aborted instruction. The application program needs no knowledge of the amount of memory available to it, nor is its state in any way affected by the abort.

After fixing the reason for the abort, the handler should execute the following irrespective of the state (ARM or Thumb):

```
SUBS    PC,R14_abt,#4    ;  for a prefetch abort, or
SUBS    PC,R14_abt,#8    ;  for a data abort
```

This restores both the PC and the CPSR, and retries the aborted instruction.

Software Interrupt

The software interrupt instruction (SWI) is used for entering Supervisor mode, usually to request a particular supervisor function. A SWI handler should return by executing the following irrespective of the state (ARM or Thumb):

```
MOV     PC,R14_svc
```

This restores the PC and CPSR, and returns to the instruction following the SWI.

NOTE

nFIQ, nIRQ, ISYNC, LOCK, BIGEND, and ABORT pins exist only in the ARM920T CPU core.

Undefined Instruction

When ARM920T comes across an instruction which it cannot handle, it takes the undefined instruction trap. This mechanism may be used to extend either the THUMB or ARM instruction set by software emulation.

After emulating the failed instruction, the trap handler should execute the following irrespective of the state (ARM or Thumb):

```
MOVS    PC,R14_und
```

This restores the CPSR and returns to the instruction following the undefined instruction.

Exception Vectors

The following table shows the exception vector addresses.

Table 2-4. Exception Vectors

Address	Exception	Mode in Entry
0x00000000	Reset	Supervisor
0x00000004	Undefined instruction	Undefined
0x00000008	Software Interrupt	Supervisor
0x0000000C	Abort (prefetch)	Abort
0x00000010	Abort (data)	Abort
0x00000014	Reserved	Reserved
0x00000018	IRQ	IRQ
0x0000001C	FIQ	FIQ

Exception Priorites

When multiple exceptions arise at the same time, a fixed priority system determines the order in which they are handled:

Highest priority:

1. Reset
2. Data abort
3. FIQ
4. IRQ
5. Prefetch abort

Lowest priority:

6. Undefined Instruction, Software interrupt.

Not All Exceptions Can Occur at Once:

Undefined Instruction and Software Interrupt are mutually exclusive, since they each correspond to particular (non-overlapping) decodings of the current instruction.

If a data abort occurs at the same time as a FIQ, and FIQs are enabled (ie the CPSR's F flag is clear), ARM920T enters the data abort handler and then immediately proceeds to the FIQ vector. A normal return from FIQ will cause the data abort handler to resume execution. Placing data abort at a higher priority than FIQ is necessary to ensure that the transfer error does not escape detection. The time for this exception entry should be added to worst-case FIQ latency calculations.

INTERRUPT LATENCIES

The worst case latency for FIQ, assuming that it is enabled, consists of the longest time the request can take to pass through the synchroniser (*Tsyncmax* if asynchronous), plus the time for the longest instruction to complete (*Tldm*, the longest instruction is an LDM which loads all the registers including the PC), plus the time for the data abort entry (*Texc*), plus the time for FIQ entry (*Tfiq*). At the end of this time ARM920T will be executing the instruction at 0x1C.

Tsyncmax is 3 processor cycles, *Tldm* is 20 cycles, *Texc* is 3 cycles, and *Tfiq* is 2 cycles. The total time is therefore 28 processor cycles. This is just over 1.4 microseconds in a system which uses a continuous 20 MHz processor clock. The maximum IRQ latency calculation is similar, but must allow for the fact that FIQ has higher priority and could delay entry into the IRQ handling routine for an arbitrary length of time. The minimum latency for FIQ or IRQ consists of the shortest time the request can take through the synchroniser (*Tsyncmin*) plus *Tfiq*. This is 4 processor cycles.

RESET

When the **nRESET** signal goes LOW, ARM920T abandons the executing instruction and then continues to fetch instructions from incrementing word addresses.

When **nRESET** goes HIGH again, ARM920T:

1. Overwrites R14_svc and SPSR_svc by copying the current values of the PC and CPSR into them. The value of the saved PC and SPSR is not defined.
2. Forces M[4:0] to 10011 (Supervisor mode), sets the I and F bits in the CPSR, and clears the CPSR's T bit.
3. Forces the PC to fetch the next instruction from address 0x00.
4. Execution resumes in ARM state.

ARM920T SYSTEM CONTROL COPROCESSOR (CP15) REGISTER SUMMARY

Throughout this section the following terms and abbreviations are used:

Term	Abbreviation	Description
unpredictable	UNP	For reads: the data returned when reading from this location is unpredictable; it could have any value. For writes: writing to this location will cause unpredictable behavior, or an unpredictable change in device configuration.
undefined		An instruction that accesses CP15 in the manner indicated will take the undefined instruction trap.
should be zero	SBZ	When writing to this location, all bits of this field should be 0.
should be one		When writing to this location, all bits in this field should be 1.

In all cases, reading from, or writing any data values to any CP15 registers, including those fields specified as unpredictable or should be zero, will not cause any permanent damage.

CP15 defines 16 registers. Table 2-2 on page 2-4 shows which registers are defined forreading and which registers are defined for writing. All CP15 register bits that aredefined and contain state, are set to zero by **Reset** except V-Bit in register 1, which takes the value of macrocell input **VINITH**I.

CP15 registers can only be accessed with MRC and MCR instructions in a privileged mode. The instruction bit pattern of the MCR and MRC instructions is shown in Figure 2-1. The assembler for these instructions is

MCR/MRC{cond} P15,opcode_1,Rd,CRn,CRm,opcode_2

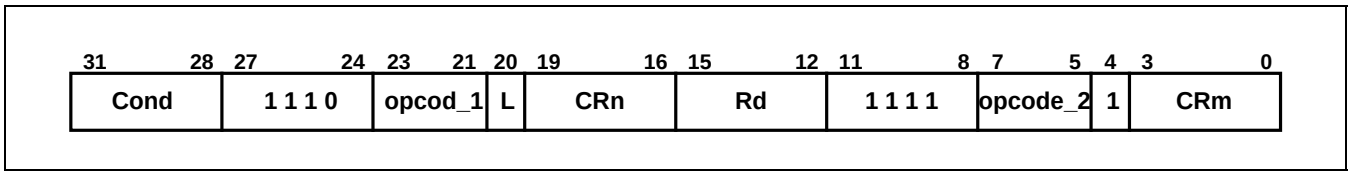


Figure 2-1 CP15 MRC and MCR bit pattern

Instructions CDP, LDC and STC, along with unprivileged MRC and MCR instructions to CP15 will cause the undefined instruction trap to be taken. The `CRn` field of MRC and MCR instructions specifies the coprocessor register to access. The `CRm` field and `opcode_2` field are used to specify a particular action when addressing registers.

Attempting to read from a non-readable register, or writing to a non-writable register will cause unpredictable results.

The opcode_1, opcode_2 and CRm fields should be zero, except when the values specified should be used to select the desired operations, in all instructions which access CP15. Using other values will result in unpredictable behavior.

Table 2-1 CP15 abbreviations

Register	Reads	Writes
0	ID	Unpredictable
1	Control	Control
2	Translation table base	Translation table base
3	Domain access control	Domain access control
4	Unpredictable	Unpredictable
5	Fault status	Fault status
6	Fault address	Fault address
7	Unpredictable	Cache operations
8	Unpredictable	TLB operations
9	Cache lock down	Cache lock down
10	TLB lock down	TLB lock down
11	Unpredictable	Unpredictable
12	Unpredictable	Unpredictable
13	Process ID	Process ID
14	Unpredictable	Unpredictable
15	Test configuration	Test configuration

2.2.1 CP15 REGISTERS

REGISTER 0: ID REGISTER

Register 0 is the ID register and cache configuration register.

Reading from this register will return the device ID or the ICache and DCache sizes and line lengths of the device, depending on the value of opcode_2 used.

The CRm fields should be zero when reading:

- opcode_2 = 0 gives the ID value 0x4102920r, where r is the revision
- opcode_2 = 1 gives the ICache and DCache sizes, associativity and line lengths encoded as 0x0D172172

Writing to register 0 is unpredictable.

Table 2-3 Reading from register 0

Function	Data	Instruction
Read ID	ARM920T device ID	MRC p15,0,Rd,c0,c0,0
Read cache sizes	ICache and DCache type	MRC p15,0,Rd,c0,c0,1

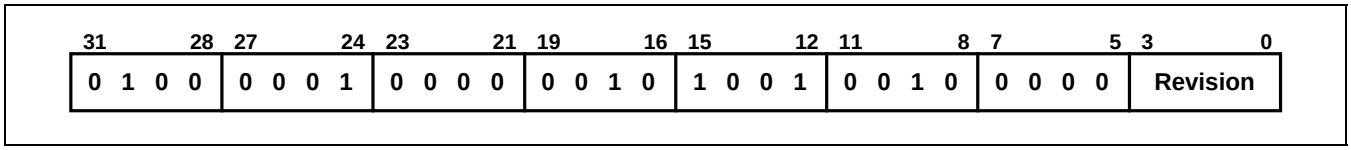


Figure 2-2 Register 0 read device ID

Bits [31:24] contain the ASCII code of implementers trademark (0x41 = ARM).

Bits [23:16] contain the architecture 0x02 = Version 4T.

Bits [15:4] contain the 3-digit part number in BCD format 0x920.

Bits [3:0] contain the revision number for the processor.

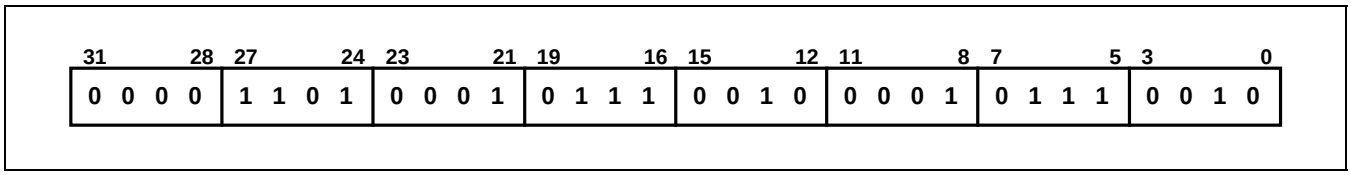


Figure 2-3 Register 0 read cache type

Register0	Bits	Function
	[31:29]	Reserved as 0b000
	[28:25]	Indicate which major cache class the implementation falls into. 0x6 means that the cache provides: • cache-clean-step operation • cache-flush-step operation • lock-down facilities.
	[24]	Contains the cache Harvardness. 1 = Harvard
	[23:21]	Reserved as 0b000
Data cache size	[20:18]	Data cache size 000 = 512B 001 = 1KB 010 = 2KB 011 = 4KB 100 = 8KB 101 = 16KB 110 = 32KB 111 = 64KB
Data cache associativity.	[17:15]	Cache associativity encoding 000 = Direct mapped 001 = 2 Associativity 010 = 4 Associativity 011 = 8 Associativity 100 = 16 Associativity 101 = 32 Associativity 110 = 64 Associativity 111 = 128 Associativity
	[14]	Reserved 0
data cache line length.	[13:12]	Line length encoding 00 = 2 word/Line 01 = 4 word/Line 10 = 8 word/Line 11 = 16 word/Line

3 CLOCK & POWER MANAGEMENT(Preliminary)

OVERVIEW

The Clock Generator in S3C2800X can generate the necessary clocks signals for the CPU as well as peripherals. The Clock Generator has the controllability of supplying or disconnecting clock to each peripheral block by S/W, which will reduce the power by having the selection on necessary peripherals suitable for given task. As well as this kind of S/W controllability, S3C2800X has various power management schemes to keep the optimal power consumption for the operation of given task.

The power management in S3C2800X consists of three mode : Normal mode, Slow mode, Idle mode.

The Normal mode is to supply clocks to CPU as well as all peripherals in S3C2800X. In this case, the power consumption will be maximized when all peripherals are turn on. The user can control the operation of peripherals by S/W. For example, if user does not need timer and DMA, user can disconnect the clock to timer and DMA to reduce the power.

The Slow mode is non-PLL mode. The difference from Normal mode is that the Slow mode uses external crystal clock directly as master clock in S3C2800X without PLL. In this case, the power consumption depends on the frequency of external crystal clock and the power consumption due to PLL itself should be excluded, compared to Normal mode.

The Idle mode disconnects the clock to CPU core only while it supply the clock to all peripherals. By using this Idle mode, we can reduce the power consumption due to CPU core. The wake-up from Idle mode can be done by all kind of interrupt request to CPU.

FEATURE

- Input frequency range : 4MHz ~ 10MHz.
- Output frequency range : 20MHz ~ 150MHz.
- Frequency changed by programmable divider.
- Power management : Normal, Slow, Idle.
- Reset controller : Hardware, Software, Watchdog reset.

FUNCTION DESCRIPTION

CLOCK GENERATION

Figure 5-1 shows a block diagram of the clock generator. The main clock source is coming from an external crystal clock. The clock generator has an oscillator(Oscillation Amplifier) which should be connected to an external crystal, and also has a PLL (Phase-Locked-Loop) which takes the low frequency oscillator output as its input and generates the high frequency clock required by S3C2800X. The clock generator block has the logic to generate a stable clock frequency after a reset because it takes time to stabilize the clock.

Maximum Bus Frequencies

Table 5-1 lists the maximum operating frequencies for the S3C2800X. When selecting strap settings, ensure that the bus divider ratios result in bus frequencies that do not exceed these maximums.

Table3-1 Maximum Bus Frequencies

Internal Bus	Maximum Frequency	Module on the Internal Bus	Symbol
CPU	150MHz	CPU Core, I/D cache, R/W Buffer, MMU	CPUCLK
AHB	75MHz	DMA,Interrupt,Clock & Power, PCI, Memory controller	AHBCLK
APB	50MHz	IIC, GPIO, UART, Timer, Remote Signal Receive, RTC, Watchdog timer.	APBCLK

Table 3-2. Possible Maximum Frequency

CPU Frequency(CPUCLK)	AHB Frequency(AHBCLK)	APB Frequency(APBCLK)
150MHz	75MHz (= CPUCLK/2)	37.5MHz (= AHBCLK/2)
133MHz	66.5MHz (= CPUCLK/2)	33.25MHz (= AHBCLK/2)
100MHz	50MHz (= CPUCLK/2)	50MHz (= AHBCLK)
75MHz	75MHz (= CPUCLK)	37.5MHz (= AHBCLK/2)

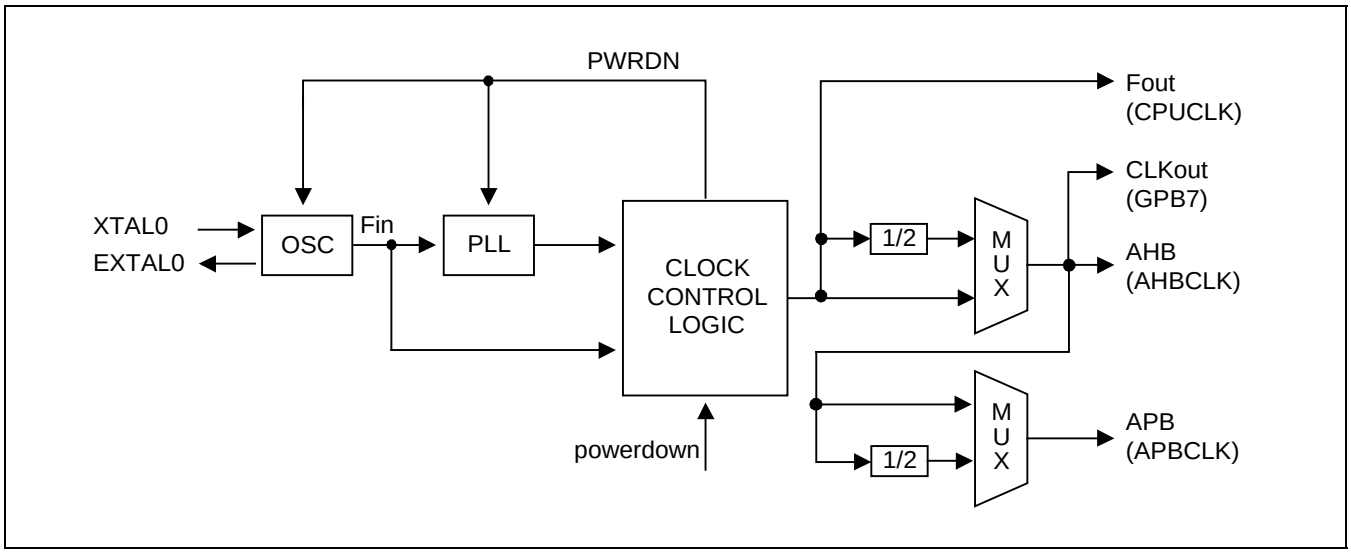


Figure 3-1. Clock Generator Block Diagram

NOTES:

1. Although the PLL starts its operate just after a reset, the PLL output can not be used as Fpllo until S/W writes valid settings to the PLLCON register. Before this valid setting, the clock from crystal oscillator clock source will be used as Fout directly until lock time is started. Even if user want to maintain the default value of PLLCON register, user should write the same value into PLLCON register.

PLL (PHASE-LOCKED-LOOP)

The PLL within the clock generator is the circuit which synchronizes an output signal with a reference or input signal in terms of frequency as well as phase. In this application, it includes the following basic blocks (Figure 5-2 show the PLL block diagram), the VCO(Voltage Controlled Oscillator) to generate the output frequency proportional to input DC voltage, the divider P to divide the reference frequency by p, the divider M to divide the VCO output frequency by m which is input to PFD(Phase Frequency Detector), the divider S to divide the VCO output frequency by s which is Fpllo(the output frequency from PLL block), the phase detector, charge pump, and loop filter. The output clock frequency Fpllo is related to the reference input clock frequency Fin by the following equation:

$$Fpllo = (m * Fin) / (p * 2^S)$$

m = M (the value for divider M)+ 8, p = P(the value for divider P) + 2

The following sections describe the PLL operation that includes the phase detector, charge pump, VCO (Voltage controlled oscillator), and loop filter.

Phase Detector

The phase detector monitors the phase difference between the Fref (the reference frequency as shown in Fig. 5-2) and Fvco (the output frequency from VCO and Divider M block), and generates a control signal(tracking signal) when it detects difference between two.

Charge Pump

The charge pump converts the phase detector control signal into a proportional charge in voltage across the external filter that drives the VCO.

Loop Filter

The control signal that the phase detector generates for the charge pump, may generate large excursions(ripples) each time the VCO output is compared to the system clock. To avoid overloading the VCO, a low pass filter samples and filters the high-frequency components out of the control signal. The filter is typically a single-pole RC filter consisting of a resistor and capacitor.

A recommended capacitance in external loop filter(Capacitance as shown in Figure 5-2) is 700pF.

Voltage Controlled Oscillator (VCO)

The output voltage from the loop filter drives the VCO, causing its oscillation frequency to increase or decrease linearly as a function of variations in average voltage. When the VCO output matches the system clock in terms of frequency as well as phase, the phase detector stops sending a control signal to the charge pump, which in turn stabilizes the input voltage to the loop filter. The VCO frequency then remains constantly, and the PLL remains locked onto the system clock.

Usual Condition for PLL & Clock Generator

The following condition is used usually.

Loop filter capacitance	320 pF
External X-tal frequency	4 ~ 10 Mhz
External capacitance used for X-tal	15 ~ 22 pF

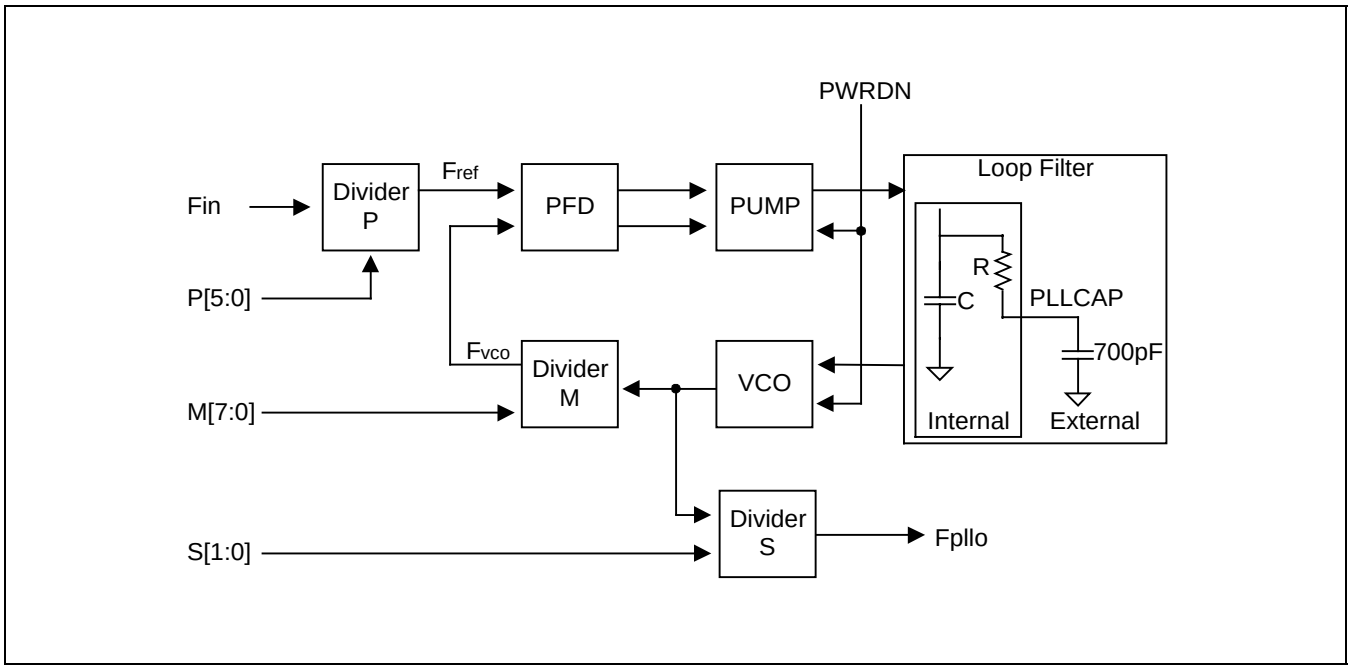


Figure 3-2. PLL (Phase-Locked Loop) Block Diagram

CLOCK CONTROL LOGIC

The clock control logic determines which clock source should be used, i.e., the PLL clock or the direct OSC clock. When PLL is configured to new frequency value, the clock control logic disables the Fpllo up to when PLL output is stabilized through the PLL locking time. The clock control logic is also activated when the power-on reset and wake-up from power-down mode happens.

PLL Lock Time

The lock time is the minimum time that is needed until the PLL output is stabilized. The lock time is a minimum 200us. After reset, the lock-time is inserted automatically by internal logic with lock time count register. The automatically inserted lock time is calculated as follows;

t_lock(the PLL lock time by H/W logic) = (1/ Fin) x n, (n = LTIMECNT value)

Power-On Reset

Figure 5-3 shows the clock behavior during the power-on reset sequence. The crystal oscillator begins oscillation within several milliseconds. When nRESET is released after the stabilization of OSC clock, the PLL begins the operation according to the default PLL configuration. But, as it is known that the PLL output is unstable after power-on reset, the Fin is feed to Fout directly instead of the Fpllo(PLL output) before new configuration on PLLCON by S/W. Even if the user want to use the default value of PLLCON register after Reset, the user should write the same value into PLLCON register by S/W.

Only after PLL is configured to have a new frequency by S/W, the PLL begins the lockup sequence again toward the new frequency. Just after the lock time, the Fout can be configured to be PLL output(Fpllo).

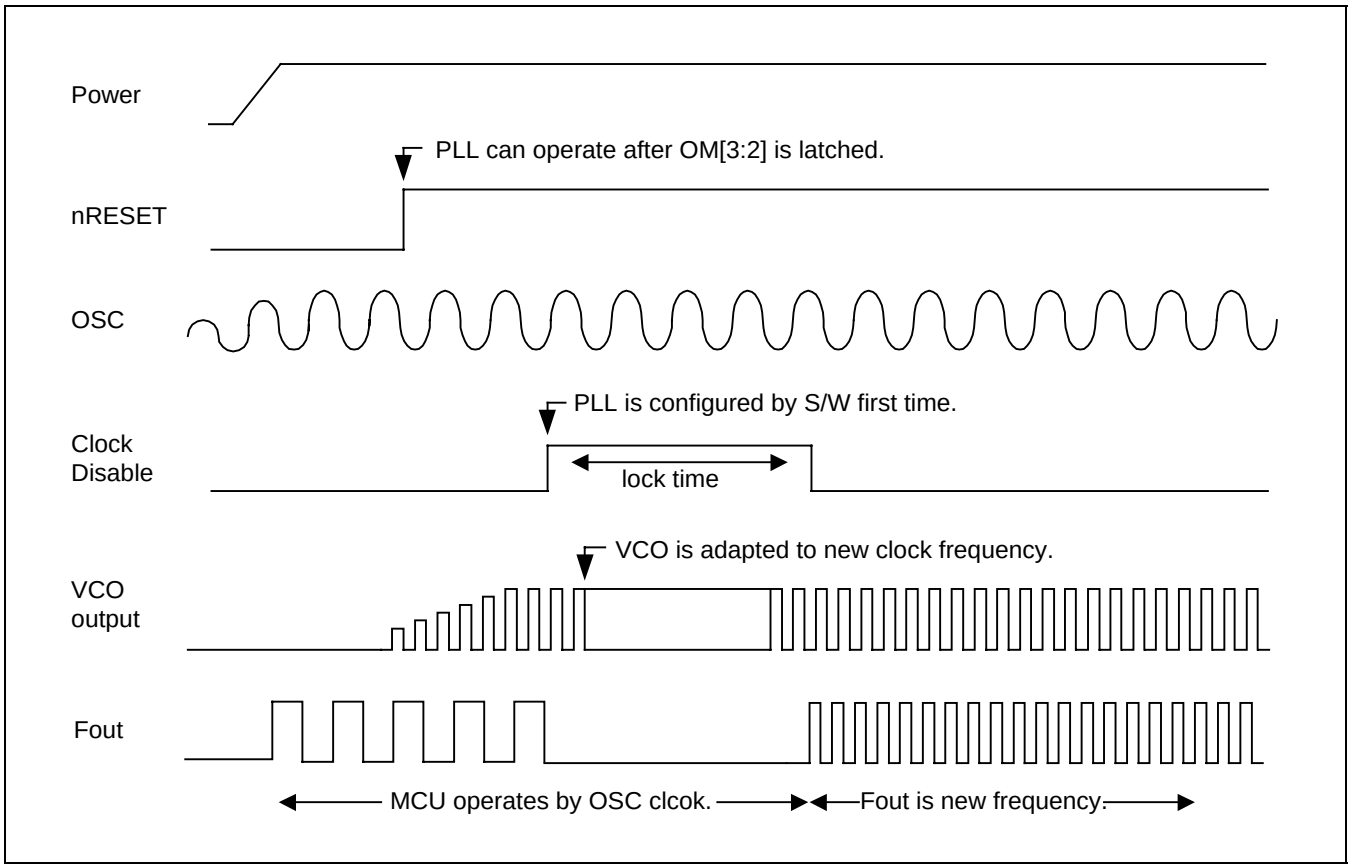


Figure 3-3. Power-On Reset Sequence

Change PLL Settings In Normal Operation Mode

During the operation of S3C2800X in Normal mode, if user want to change the frequency by writing PMS value, the PLL lock time is automatically inserted. During the lock time, the clock is not supplied to internal blocks in S3C2800X. The timing diagram is as follow.

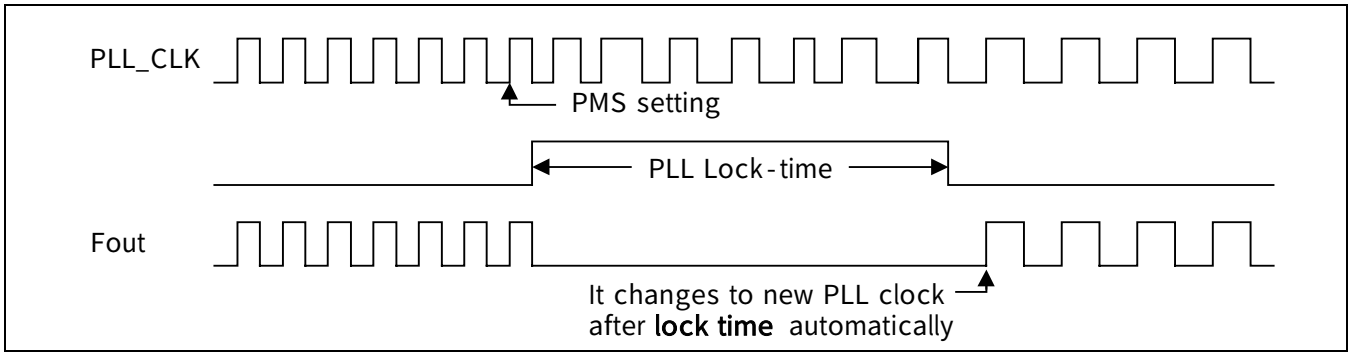


Figure 5-4. The case that change Slow clock by setting PMS value

POWER MANAGEMENT

The power management block controls the system clocks by software for reduction of power consumption in S3C2800X. These schemes are related with PLL, clock control logic, peripheral clock control, and wake-up signal.

S3C2800X has four power-down modes. The following section describes each power managing mode. The transition between the modes isn't allowed freely. For available transitions among the modes, please refer to Figure 5-10.

Normal Mode

In normal mode, All peripherals(UART, DMA, Timer, and so on) and the basic blocks(CPU core, bus controller, memory controller, interrupt controller, and power management block) may operate fully. But, the clock to each peripheral, except the basic blocks, can be stopped selectively by S/W for the reduction of power consumption.

NOTE : The basic blocks consist of the CPU core, bus controller, memory controller, interrupt controller, and power management.

IDLE Mode

In IDLE mode, the clock to CPU core among the basic blocks is stopped except bus controller, memory controller, interrupt controller, and power management block. To exit IDLE mode, EXTINT[7:0], or RTC alarm interrupt, or the other interrupts should be activated. (If users are willing to use EXTINT[7:0], GPIO block has to be turned on before the activation).

SLOW Mode (non-PLL Mode)

The SLOW mode can reduce the power consumption if we apply slow clock and because we can exclude the power consumption due to PLL itself. The Fout is the frequency of divide_by_n of Fin without PLL. The divider ratio is determined by SLOW_VAL in the CLKSLOW control register.

Fout = Fin / (2 x SLOW_VAL), when SLOW_VAL is bigger than 0
Fout = Fin , when SLOW_VAL is 0

In SLOW mode, the PLL will be turned off to reduce the PLL power consumption. When PLL is turned off in SLOW mode and users change power mode from SLOW mode to NORMAL mode, the PLL need clock stabilization time(PLL lock time). This PLL stabilization time is automatically inserted by internal logic with lock time count register. The PLL stability time will be taken 200us after PLL is turn on. During PLL lock time, the Fout is SLOW clock.

Users can change the frequency by enabling SLOW mode bit in CLKSLOW register. The SLOW clock is generated during SLOW mode. The timing diagram is as follow.

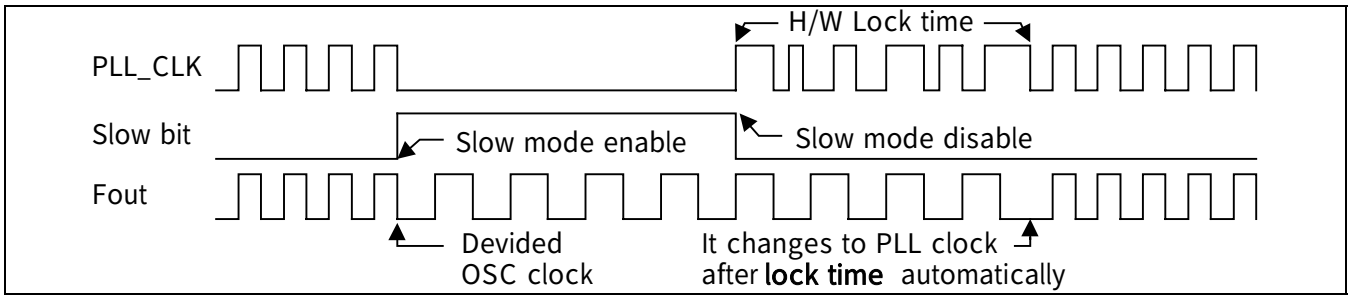


Figure 3-5. The Timing Diagram in Slow Mode

Entering IDLE Mode

If CLKCON[2] is set to 1 to enter the IDLE mode, S3C2800X will enter into IDLE mode after some delay(Up to when the power control logic receives ACK signal from the CPU wrapper).

PLL On/Off

The PLL can only be turned off for power saving in slow mode.

POWER MANAGEMENT STATE MACHINE

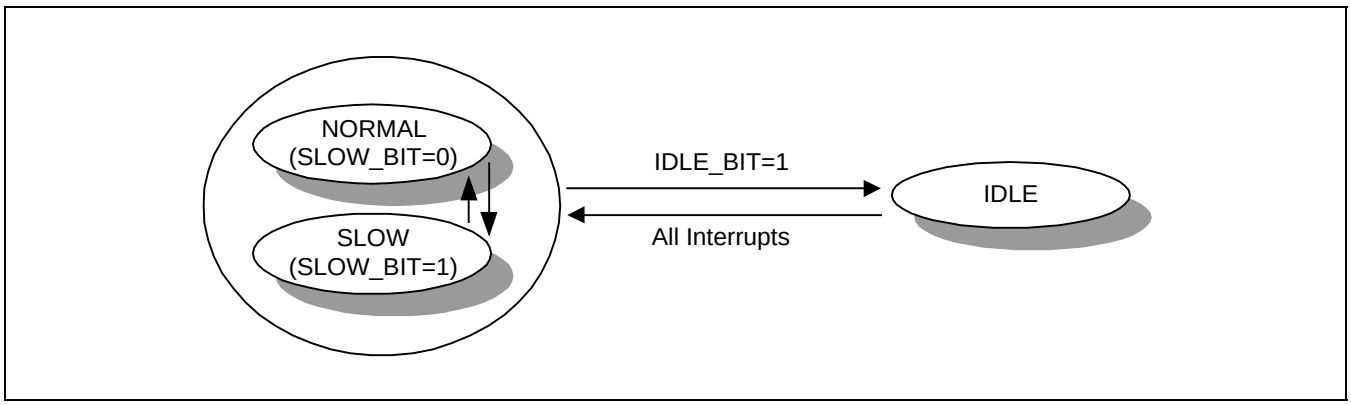


Figure 3-6. Power Management State Machine

CLOCK GENERATOR & POWER MANAGEMENT SPECIAL REGISTER

PLL CONTROL REGISTER (PLLCON)

Fpllo = (m * Fin) / (p * 2^S)
m = (MDIV + 8), p = (PDIV + 2), s = SDIV

Table 5-2. For example, A value of MDIV, PDIV, SDIV(M=MDIV, P=PDIV, S=SDIV)

Fin / Fout	4 MHz (M / P / S)	5 MHz (M / P / S)	6 MHz (M / P / S)	7 MHz (M / P / S)	8 MHz (M / P / S)	9 MHz (M / P / S)	10 MHz (M / P / S)
20 MHz	0x20 / 0 / 2	0x38 / 0 / 3	0x48 / 1 / 3	-	0x48 / 2 / 3	-	0x48 / 3 / 3
40 MHz	0x48 / 0 / 2	0x78 / 0 / 3	0x98 / 1 / 3	-	0x98 / 2 / 3	-	0x98 / 3 / 3
66 MHz	0x3A / 0 / 1	-	0x7C / 1 / 2	-	0x7C / 2 / 2	0xA8 / 1 / 3	0x7C / 3 / 2
80 MHz	0x48 / 0 / 1	0xF8 / 0 / 3	0x98 / 1 / 2	-	0x98 / 2 / 2	-	0x98 / 3 / 2
100 MHz	0xC0 / 0 / 2	0x98 / 0 / 2	0xC0 / 1 / 2	-	0xC0 / 2 / 2	-	0xC0 / 3 / 2
120 MHz	0xE8 / 0 / 2	0xB8 / 0 / 2	0xE8 / 1 / 2	-	0x8E / 3 / 1	0x98 / 1 / 2	0xE8 / 3 / 2
133 MHz	0x7D / 0 / 1	-	0x7D / 1 / 1	0xDC / 1 / 2	0x7D / 2 / 1	-	0x7D / 3 / 1
150 MHz	0x8E / 0 / 1	0xE8 / 0 / 2	0x8E / 1 / 1	-	0xD9 / 1 / 2	0xC0 / 1 / 2	0xE8 / 2 / 2

note : This value may be calculated using PLLSET.EXE utility from Samsung.
This PLL is not guaranteed that the PMS values are all zero.

PLL VALUE SELECTION GUIDE

1. (Fin/p) must be equal or above than 2MHz (p=PDIV+2).

PLL CONFIGURATION REGISTER(PLLCON)

Register	Address	R/W	Description	Reset Value
PLLCON	0x1000 0000	R/W	PLL configuration Register	0x000C 0002

PLLCON	Bit	Description	Initial State
Reserved	[31:20]	Reserved	
MDIV	[19:12]	Main divider control	0xC0
Reserved	[11:10]	Reserved	0
PDIV	[9:4]	Pre-divider control	0x00
Reserved	[3:2]	Reserved	00
SDIV	[1:0]	Post divider control	10

CLOCK CONTROL REGISTER (CLKCON)

Register	Address	R/W	Description	Reset Value
CLKCON	0x1000 0004	R/W	Clock generator control Register	0x0000 1FFC

CLKCON	Bit	Description	Initial State
APBCLK	[12]	APB divide ratio from AHB 0 = AHBLCK 1 = AHBCLK/2	1
AHBCLK	[11]	AHB divide ratio from CPU 0 = CPUCLK 1 = CPUCLK/2	1
PCI	[10]	Controls CPUCLK into PCI block 0 = Disable, 1 = Enable	1
IIC1	[9]	Controls APBCLK into IIC0 block 0 = Disable, 1 = Enable	1
IIC0	[8]	Controls APBCLK into IIC1 block 0 = Disable, 1 = Enable	1
RTC	[7]	Controls APBCLK into RTC control block. Even if this bit is cleared to 0, RTC timer is alive. 0 = Disable, 1 = Enable	1
UART1	[6]	Controls APBCLK into UART1 block 0 = Disable, 1 = Enable	1
UART0	[5]	Controls APBCLK into UART0 block 0 = Disable, 1 = Enable	1
DMA2,3	[4]	Controls AHBCLK into DMA channel 2,3 block 0 = Disable, 1 = Enable (If DMA is turned off, the peripherals in the peripheral bus may not be accessed)	1
DMA0,1	[3]	Controls AHBCLK into DMA channel 0,1 block 0 = Disable, 1 = Enable (If DMA is turned off, the peripherals in the peripheral bus may not be accessed)	1
TIMER	[2]	Controls APBCLK into TIMER block 0 = Disable, 1 = Enable	1
IDLE BIT	[1]	Enters IDLE mode. This bit cleared automatically by wake-up. 0 = Disable, 1 = Transition to IDLE(SL_IDLE) mode	0
Reserved	[0]	Reserved This bit must be 0.	0

CLOCK SLOW CONTROL REGISTER (CLKSLOW)

Register	Address	R/W	Description	Reset Value
CLKSLOW	0x1000 0008	R/W	Slow clock control register	0x0000 0000

CLKSLOW	Bit	Description	Initial State
Reserved	[31:5]	Reserved	
SLOW_BIT	[4]	Slow mode enable or Disable 0 : Disable slow mode (Normal mode) Fout = Fpllo (PLL output) 1 : Enable slow mode (Slow mode) Fout = Fin / (2 x SLOW_VAL), (SLOW_VAL > 0) Fout = Fin, (SLOW_VAL = 0)	0x0
SLOW_VAL	[3:0]	The divider value for slow clock when SLOW_BIT is on.	0x0

LOCK TIME COUNT REGISTER (LOCKTIME)

Register	Address	R/W	Description	Reset Value
LOCKTIME	0x1000 000C	R/W	PLL lock time count register	0x0000 0FFF

LOCKTIME	Bit	Description	Initial State
Reserved	[31:12]	Reserved	
LTIME CNT	[11:0]	PLL lock time count value	0xFFF

RESET CONTROLLER

The reset controller manages the various reset sources within the S3C2800X. From a programmer's view, it is visible as two registers: one used to invoke software reset and one to read status after booting to indicate why the processor was reset.

The three types of reset in the S3C2800X include:

HARDWARE RESET

Hardware reset is invoked when the nRESET pin is asserted and resets all units in the S3C2800X to a known state. Hardware reset is intended to be used for power-up only. Because the memory controller receives a full reset, all dynamic memory(DRAM/SDRAM) contents will be lost during hardware reset.

The nRESET_OUT pin is asserted during hardware reset.

SOFTWARE RESET

Software reset is invoked when the software reset (SWR) bit in the SWRCON is set by software. After the SWR bit is set, the S3C2800X stays reset for 128 processor clocks(APBCLK) and then is allowed to boot again.

The nRESET_OUT pin is asserted during software reset

WATCHDOG RESET

Watchdog reset is invoked when the watchdog enable bits in the WTCON[7:0] is set and the WTCNT matches the watchdog timer counter. When watchdog reset is invoked, the rest of the reset sequence is identical to software reset. After the WTCNT matches the watchdog timer counter, the S3C2800X stays reset for 128 processor clocks(APBCLK) and then is allowed to boot again.

The nRESET_OUT pin is asserted during watchdog reset

After booting from a reset, software can examine the reset and RTC alarm match status register (RAMSR) to determine which types of reset caused the reset condition.

RESET CONTROLLER REGISTERS

The reset controller contains two registers, the software reset control register (SWRCON) and the reset and RTC alarm match status register (RAMSR).

The software reset control register has a software reset bit, which when set, causes a reset of the S3C2800X. The software reset bit (SWR) is located within the least significant bit of the write-only software reset register (SWRCON). Writing a one to this bit causes all on-chip resources to reset but does not cause the PLL to go out of lock. The software reset bit is self-resetting. It is automatically cleared to zero several system clock cycles after a one is written to it. Writing zero to the software reset bit has no effect. Care should be taken to restrict access to this register by programming MMU permissions.

The following table shows the SWRCON.

SOFTWARE RESET CONTROL REGISTER (SWRCON)

Register	Address	R/W	Description	Reset Value
SWRCON	0x1000 0010	W	Software reset control register	0x0000 0000

SWRCON	Bit	Description	Initial State
Reserved	[31:1]	Reserved	
SWR	[0]	Software reset. 0 = Do not invoke a software reset of the chip. 1 = Invoke a software reset of the chip. This bit is self-resetting, and is automatically cleared several system clock cycles after it has been set.	0

RESET & RTC ALARM MATCH STATUS REGISTER (RAMSR)

The reset status register (RSR) is used by the CPU to determine the last cause or causes of the reset. The S3C2800X has three sources of reset:

- Hardware reset
- Software reset
- Watchdog reset

Each RSR status bit is set by a different source of reset, and can be cleared by setting a one of the other reset status bits. Note that the hardware reset state of software and watchdog reset bits is zero.

The RTC alarm match status bit is set when the RTC alarm is matched only, and can be cleared by writing a zero to that bit.

The table below shows the status bits within RAMSR.

RESET AND RTC ALARM MATCH STATUS REGISTER (RAMSR)

Register	Address	R/W	Description	Reset Value
RAMSR	0x1000 0014	R/W	Reset and RTC alarm match status register	0x0000 0001

RAMSR	Bit	Description	Initial State
Reserved	[31:4]	Reserved	
Alarm Match	[3]	RTC alarm match 0 = RTC alarm match has not occurred. 1 = RTC alarm match has occurred. This bit can be cleared by writing a zero.	0
WDR	[2]	Watchdog reset.(Read only) 0 = Watchdog reset has not occurred. 1 = Watchdog reset has occurred This bit can be cleared only by setting a one of the other reset status bits.	0
SWR	[1]	Software reset.(Read only) 0 = Software reset has not occurred. 1 = Software reset has occurred This bit can be cleared only by setting a one of the other reset status bits.	0
HWR	[0]	Hardware reset.(Read only) 0 = Hardware reset has not occurred. 1 = Hardware reset has occurred This bit can be cleared only by setting a one of the other reset status bits.	1

Clock & Power Control Register

Register	Address	R/W	Description	Reset Value
PLLCON	0x1000 0000	R/W	PLL configuration Register	0x0008 E011
CLKCON	0x1000 0004	R/W	Clock generator control Register	0x0000 1FFC
CLKSLOW	0x1000 0008	R/W	Slow clock control register	0x0000 0000
LOCKTIME	0x1000 000C	R/W	PLL lock time count register	0x0000 0FFF
SWRCON	0x1000 0010	W	Software reset control register	0x0000 0000
RAMSR	0x1000 0014	R/W	Reset and RTC alarm match status register	0x0000 0001

4 DMA(Preliminary)

OVERVIEW

We support 4 DMA controllers. They are located between the system bus and the peripheral bus. Each of DMA controllers can perform the data movement among the devices in the system bus and/or peripheral bus with no restrictions.

For example, we can perform

1) memory to memory transfer (both source and destination are in the system bus(AHB)),

2) memory to an I/O device in the peripheral bus(APB),

3) I/O device to memory (source is in the peripheral bus(APB) and destination is in the system bus(ASB)), and

4) I/O device to I/O device (both source and destination are in the peripheral bus(APB)).

The main advantage of DMA is that it can transfer the data without CPU intervention. The operation of DMA can be initiated by S/W, the request from internal peripherals or the external request pins(nXDREQ0,nXDREQ1).

DMA OPERATION

The details of DMA operation can be explained using three-state FSM as follows:

State-1. As an initial state, it waits for the DMA request. If it comes, go to state-2. At this state, DMA ACK and INT REQ are low.

State-2. In this state, DMA ACK becomes high and TC is loaded from the SRC register. Note that DMA ACK remains high until it is cleared.

State-3. In this state, sub-FSM handling the actual operation of DMA is initiated.

The sub-FSM reads the data from the source address and then writes it to destination address. In this operation, data size and transfer size (single and burst) are considered. This operation is repeated until TC reaches in the whole service mode, while performed only once in a single service mode.

The main FSM (this FSM) counts down the TC when the sub-FSM finishes each of writing operation. In addition, this main FSM asserts the INT REQ signal when TC reaches and the interrupt setting of CNT register is set to one. In addition, it clears DMA ACK if 1) TC reaches in the whole service mode, or 2) writing operation finishes in the single service mode.

Note that in the single service mode, these three states of main FSM are performed and then stops, and waits for another DMA REQ. And if DMA REQ comes in all the three states are repeated. Therefore, DMA ACK is asserted and then de-asserted for each transfer. In contrast, in the whole service mode, main FSM waits at state-3 until TC reaches. Therefore, DMA ACK is asserted during all the transfers and then de-asserted when TC reaches.

However, INT REQ is asserted only if TC reaches regardless of the service mode (single service mode or whole service mode).

The DMA requesting sources should assert DMA request if and only if the DMA ACK is low. Otherwise, the request may be lost.

Figure 7-1 shows the internal diagram of a DMA block. The DMA is in Bridge, which is the interface layer between AHB and APB. The main role of DMA is to transfer the data between external memory and internal peripherals like UART, Timer, etc, which are attached to APB. The Timer can also request DMA operation every time. Usually, CPU or other master device should access to external memory through memory controller, which is attached to AHB. Please remind that the DMA is also a kind of master device. To transfer the data from memory(peripheral devices) to peripheral devices(memory) attached to APB(AHB), we should use the memory controller attached to AHB. Because the DMA is in the Bridge, which is an interface layer between AHB and APB, it can transfer the data between two devices, which are attached to AHB as well as APB.

In the DMA, there is a temporary buffer which enable the multiple transfer to enhance the bus utilization as well as transfer speed. In other word, S3C2800X has a 4-word FIFO-type buffer to support the 4-word burst transfer during DMA operation. For example, during the DMA operation between memories, a 4-word burst write happens after a 4-word burst read.

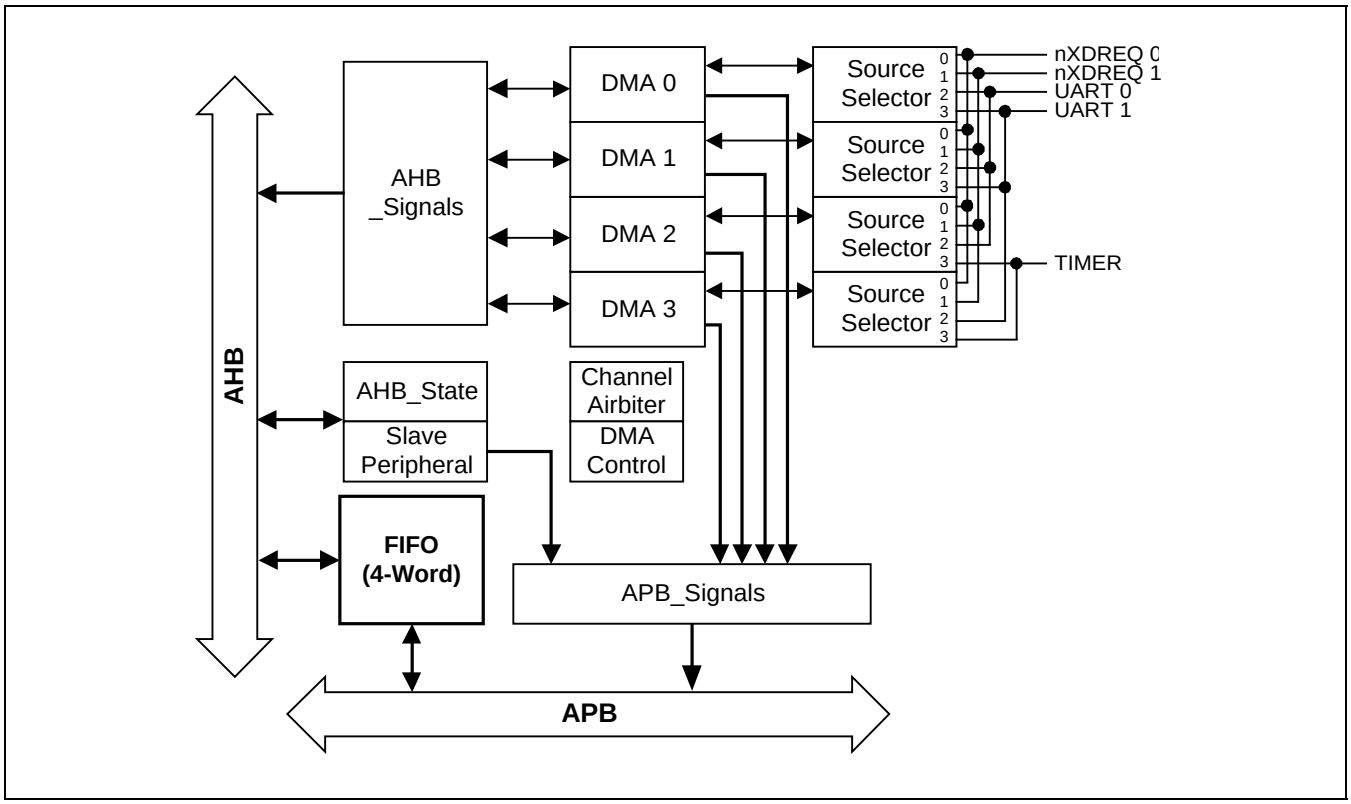


Figure 4-1. DMA Controller Block Diagram

DMA REQ/ACK PROTOCOL

There are two types of DMA request/acknowledge protocol. Each type defines how the signals like DMA request and acknowledge are related to these protocol.

Single service Mode

The single service mode means that there are two DMA acknowledge cycles indicating DMA read and write cycle. In the single service mode, the bus mastership can be handed over to other bus master between Read and Write. During the inactive period of nXDACK, i.e., between Read and Write cycle, the bus controller re-evaluates the bus priority to determine the new bus mastership.

When the DMA request signal goes low, the bus controller indicates the bus allocation for the DMA operation by lowering the DMA Acknowledge signal if there is not higher priority bus request except this DMA request. During the first low level period of the DMA Acknowledge signal, there will be a DMA read cycle. After the DMA read cycle, there will be a rising of the DMA Acknowledge signal to indicate the end of the DMA read cycle. Simultaneously, the next DMA write cycle will happen if the DMA request signal is still low at the rising edge of DMA acknowledge. But, if the DMA request signal is already high at the rising edge of DMA acknowledge, the next DMA write cycle will be delayed to the new coming of DMA request signal activation. These two cases are shown in below Figure 7-2a and Figure 7-2b.

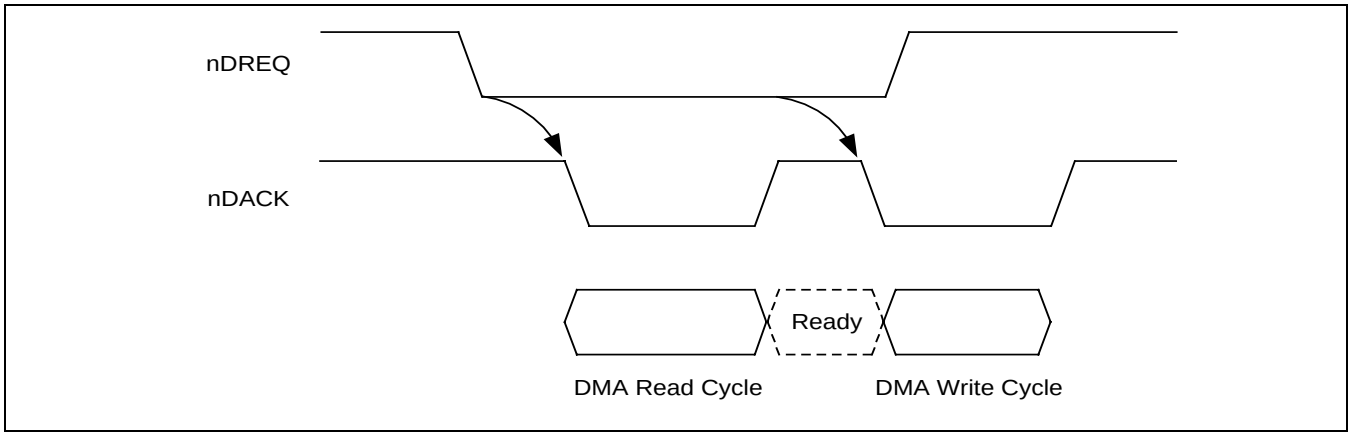


Figure 4-2a. Single Service Mode (Case 1)

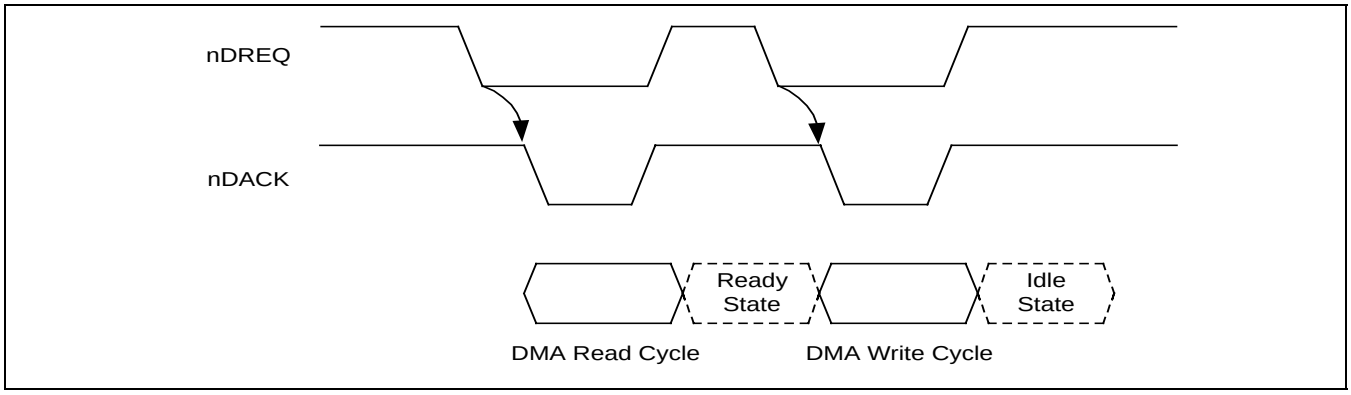


Figure 4-2b. Single Service Mode (Case 2)

Whole Service Mode

The whole service mode means that the specified number of DMA operations, i.e., number of DMA operations based on transfer count, will be initiated by a single activation of DMA Request, and will be proceeded without further activation of DMA requests. The below figure shows how the whole service mode proceeds. The nDACK signal will be active until the end of whole DMA operations.

If the number of DMA transfer operation is too large, the long bus occupation during the whole service mode of DMA operation may make problem because the other bus services can't be provided. To solve this kind of problem, the DMA releases the bus mastership in the whole service mode every time when one unit (1byte, or 1 half-word, or 1 word) is transferred. When the DMA release the bus mastership, the other bus masters, such as CPU, the other DMA, etc,may have bus mastership. This feature in whole service mode can provide the optimal bus sharing, preventing the monopoly of bus mastership by DMA. If the other master intercept the bus mastership as shown in Fig 7-3b, the remained DMA operation can be done again after the service of impinged bus mastership, without the re-activation of nDREQ.

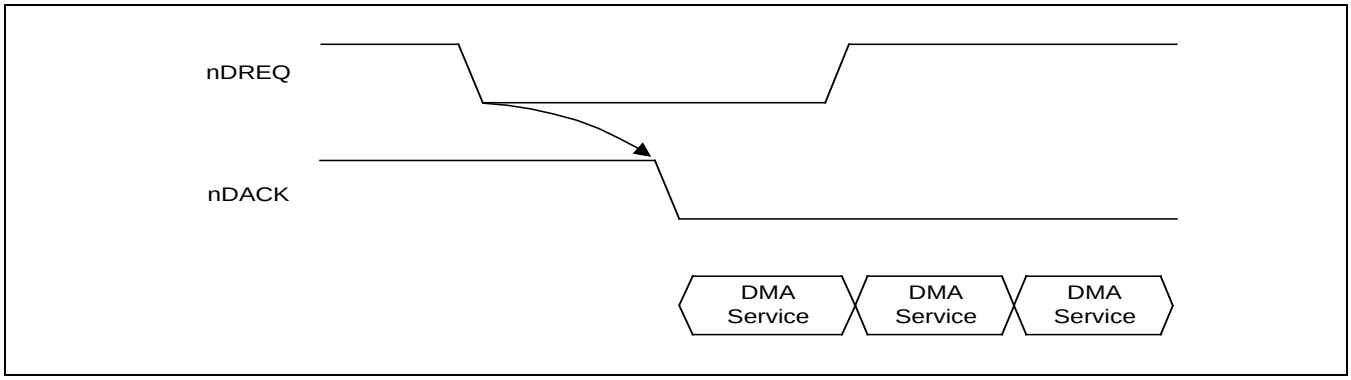


Figure 4-3a. Whole Service Mode

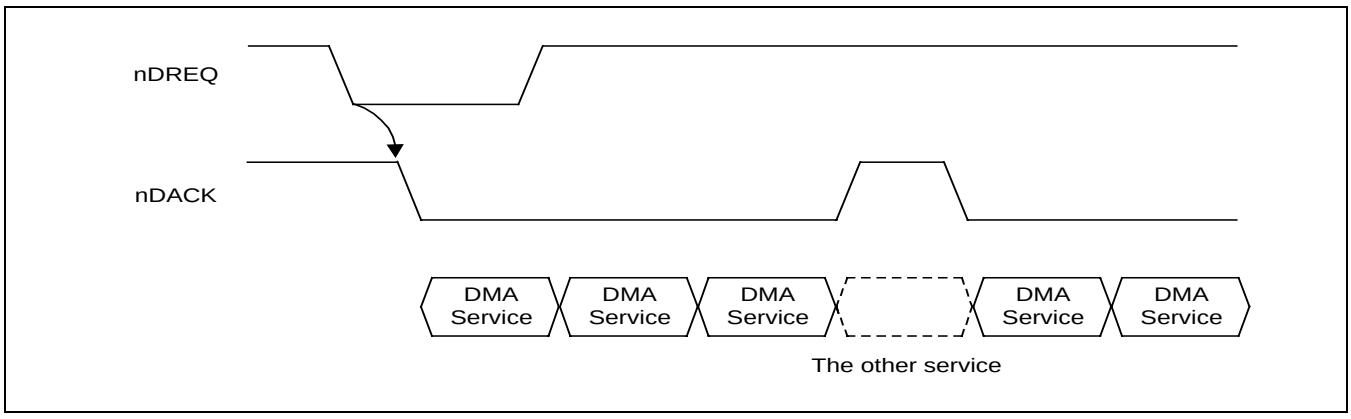


Figure 4-3b. Whole Service Mode When the Other Bus Master Acquires Bus Mastership.

DMA TRANSFER MODE

There are tow types of DMA transfer mode (Single transfer mode, Burst transfer mode). Different from the DMA request/acknowledge protocol, the DMA transfer mode defines the number of read/write per unit transfer as shown in the following table.

DMA Transfer Mode	Read/Write
Single transfer	1 unit read, then 1 unit write
Burst transfer	4 unit burst read, then 4 unit burst write

Single Transfer Mode

The single transfer mode means that the paired DMA read/write cycle happens corresponding each DMA request as shown in below Figure. Figure 7-4 shows the example case of the unit transfer mode at the sigle service mode.

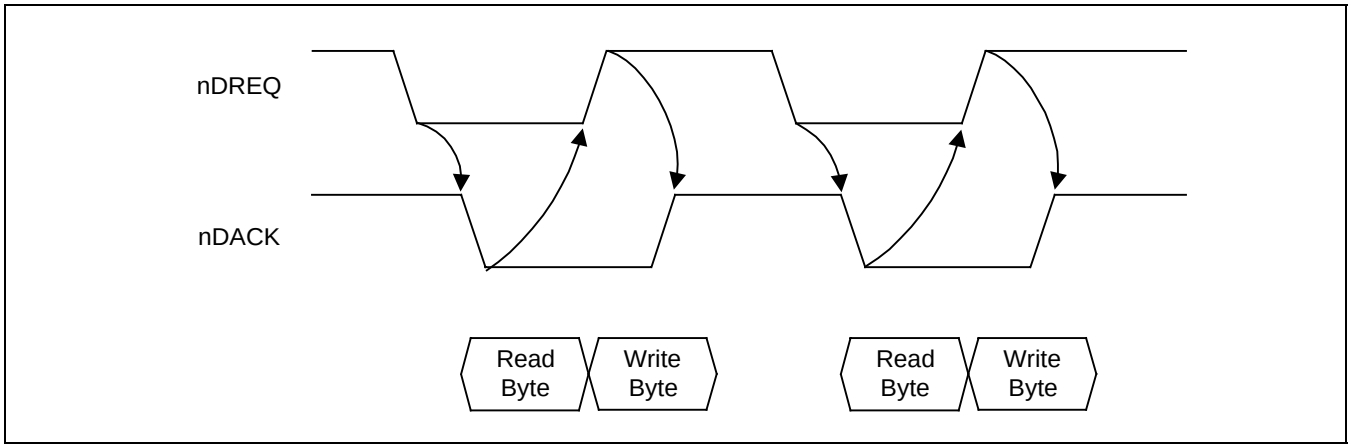


Figure 4-4. Single Transfer Mode with single service mode

Burst (4-word) Transfer Mode

The burst (4-word) transfer mode means that the successive 4-word DMA read cycle happens before successive 4-word DMA write cycles as shown in Figure 7-5. Figure 7-5 shows the example of the burst transfer mode with single service mode.

If the burst transfer mode is used, the total data size to be transferred should be the multiple of 16 bytes. In other word, the minimum transfer size is 16 bytes, i.e., 4 words. Because the DMA count is defined by byte unit, we should have 16 as DMA transfer count for the case of 4 words transfer. If the transfer size or DMA count is not multiple of 16, for example 16, 32, 48, 64, and so on, the DMA can not transfer the data completely. If we are assuming 100 bytes transfer(DMA count is 100), 100- 6x16 = 96 bytes can be transferred by block transfer mode of DMA. But, the remained 4 bytes can not be transferred because DMA operation will be stopped after 96 bytes transfer. The users should be aware of this characteristics when they select the block transfer mode of DMA.

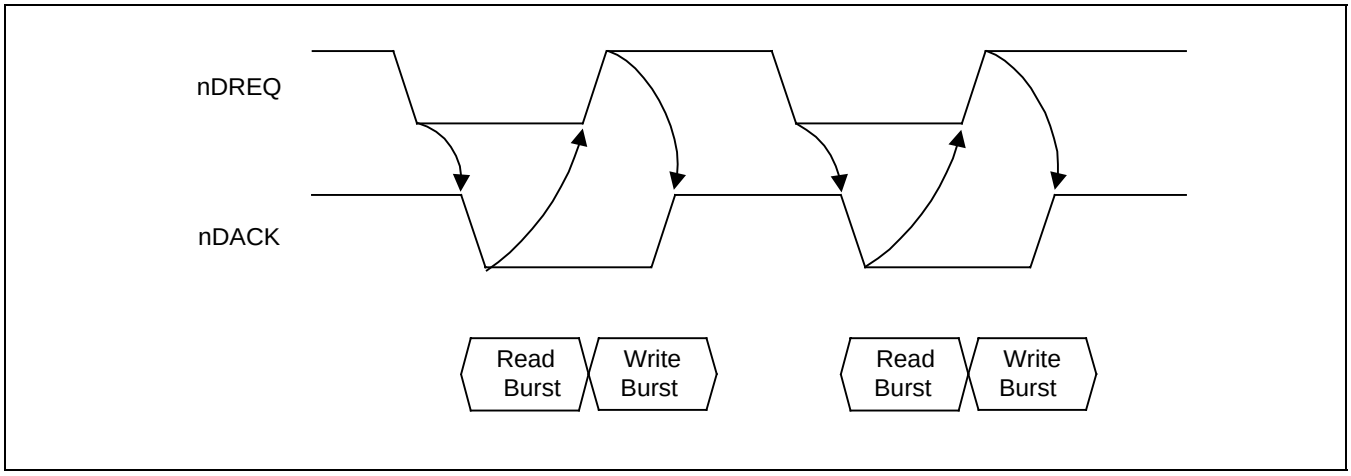


Figure 4-5. Burst Transfer Mode With Single Service Mode

DMA REQUEST SOURCE SELECTION

In the DMA request sources are S/W or H/W by writing the SSH(bit 23) field as 0 or 1 in DMACONn register. The S/W trigger can be done by writing the SWTRIG(bit 0) field as 1 in MASKTRIGn register, i.e., the start of DMA. Before the start of DMA, we should configure DMA-related parameter, for example source address, destination address, transfer count and so on. Based-on these configuration, the DMA operation will start when we write the SWTRIG field as 1. In this case of S/W trigger, the DMA operations will continue as long as the bust mastership is allocated to DMA master and as long as the DMA transfer count or TC(Terminal Count) reach to zero, i.e., the completion of DMA operation. If the higher bus master acquire the bus mastership, the DMA operations will be continued again after the service of higher priority. The DMA operations can also be initiated by nDREQ(DMA request signal) as well as S/W when the DMA is configured to have an external trigger mode, i.e., enable External DMA request by writing MASK bit as 0 in MASKTRIG register.

In DMA, there are seven hardware request sources like nXDREQ0, nXDREQ1, UART0, UART1, Timer ,SPDIF and IIS. The DMA can be initiated by software. These kinds of sources can be selected by writing the QSC field in DMACONn register.

DMA SPECIAL REGISTERS

DMA SOURCE ADDRESS REGISTER (DMASRCn)

Register	Address	R/W	Description	Reset Value
DMASRC0	0x1003 0000	R/W	DMA 0 Source address register	0x0000 0000
DMASRC1	0x1004 0000	R/W	DMA 1 Source address register	0x0000 0000
DMASRC2	0x1005 0000	R/W	DMA 2 Source address register	0x0000 0000
DMASRC3	0x1006 0000	R/W	DMA 3 Source address register	0x0000 0000

DMASRCn	Bit	Description	Initial State
SLS	[31]	Select the location of source 0 = Source is in the System bus(AHB) 1 = Source is in the Peripheral bus(APB)	0
SAI	[30]	Select the source address increment 0 = Increment The address is increased by its data size after each transfer in burst and single transfer mode 1 = Fixed(Not changed) The address is not changed after the transfer. In the burst mode, address is increased during the burst transfer, but the address is recovered to its first value after the transfer.	0
SRCADDR	[29:0]	Base address (start address) of source for the transfer	0x0000 0000

DMA DESTINATION ADDRESS REGISTER (DMASRCn)

Register	Address	R/W	Description	Reset Value
DMADES0	0x1003 0004	R/W	DMA 0 Destination address register	0x0000 0000
DMADES1	0x1004 0004	R/W	DMA 1 Destination address register	0x0000 0000
DMADES2	0x1005 0004	R/W	DMA 2 Destination address register	0x0000 0000
DMADES3	0x1006 0004	R/W	DMA 3 Destination address register	0x0000 0000

DMASRCn	Bit	Description	Initial State
SLD	[31]	Select the location of destination 0 = Destination is in the System bus(AHB) 1 = Destination is in the Peripheral bus(APB)	0
DAI	[30]	Select the destination address increment 0 = Increment The address is increased by its data size after each transfer in burst and single transfer mode 1 = Fixed(Not changed) The address is not changed after the transfer. In the burst mode, address is increased during the burst transfer, but the address is recovered to its first value after the transfer.	0
DESADDR	[29:0]	Base address (start address) of destination for the transfer	0x0000 0000

DMA CONTROL REGISTER (DMACONn)

Register	Address	R/W	Description	Reset Value
DMACON0	0x1003 0008	R/W	DMA 0 control register	0x0000 0000
DMACON1	0x1004 0008	R/W	DMA 1 control register	0x0100 0000
DMACON2	0x1005 0008	R/W	DMA 2 control register	0x0200 0000
DMACON3	0x1006 0008	R/W	DMA 3 control register	0x0300 0000

DMACONn	Bit	Description	Initial State
INTEN	[28]	Interrupt enable 0 = Interrupt disable (Software polling) 1 = Interrupt enable Interrupt request is generated when all the transfer is done.	0
TSZ	[27]	Transfer size 0 = Single transfer size 1 = Burst transfer size(4-word length)	0
SMT	[26]	Service mode for transfer 0 = Single service mode is elected in which after each transfer (single or burst of length four) DMA stops and waits for another request. 1 = Whole service mode is selected in which DMA transfer is performed until the required transfer count is met. In this mode, additional request is not required.	0
QSC	[25:24]	**Selection of hardware DMA request** **Refer to Table 7-1**	Refer to Table 7-1
SSH	[23]	Select the DMA source between software and hardware 0 = Software triggering is selected as the DMA request 1 = Hardware request is selected	0
MOA	[22]	Used to set the mask off automatically when transfer count (TC) reaches (i.e., all the transfers are performed). 0 = Not automatically 1 = Mask off automatically mask off bit of MASKTREG register is set automatically when TC reaches.	0
DSZ	[21:20]	Data size for transfer 00 = Byte 01 = Half word 1x = Word	00
TC	[19:0]	Transfer count Note that the actual number of bytes that are transferred is computed by the following equation: DSZ x TSZ x TC, where DSZ, TSZ, and TC represent data size (bit 21-20), transfer size (bit 27), and transfer count, respectively.	0x0 0000

Table 4-1 DMA Source selection

Register	Bit	Description	Initial State
DMACON0 (DMA 0)	[25:24]	Selection of hardware DMA request for DMA channel 0 00 = nXDREQ0 01 = nXDREQ1 10 = UART0 11 = UART1	00
DMACON1 (DMA 1)		Selection of hardware DMA request for DMA channel 1 00 = nXDREQ0 01 = nXDREQ1 10 = UART0 11 = UART1	01
DMACON2 (DMA 2)		Selection of hardware DMA request for DMA channel 2 00 = nXDREQ0 01 = nXDREQ1 10 = UART0 11 = TIMER	10
DMACON3 (DMA 3)		Selection of hardware DMA request for DMA channel 3 00 = nXDREQ0 01 = nXDREQ1 10 = UART1 11 = TIMER	11

DMA STATUS REGISTER (DMASTSn)

Register	Address	R/W	Description	Reset Value
DMASTS0	0x1003 000C	R	DMA 0 status register	Undefined
DMASTS1	0x1004 000C	R	DMA 1 status register	Undefined
DMASTS2	0x1005 000C	R	DMA 2 status register	Undefined
DMASTS3	0x1006 000C	R	DMA 3 status register	Undefined

DMASTSn	Bit	Description	Initial State
SDMA	[20]	Status of the DMA controller 0 = Ready for another DMA request 1 = Busy for transfers	Undefined
STC	[19:0]	Shows the current value of transfer count	Undefined

DMA CURRENT SOURCE ADDRESS REGISTER (DMACSRCn)

Register	Address	R/W	Description	Reset Value
DMACSRC0	0x1003 0010	R	DMA 0 current source address register	Undefined
DMACSRC1	0x1004 0010	R	DMA 1 current source address register	Undefined
DMACSRC2	0x1005 0010	R	DMA 2 current source address register	Undefined
DMACSRC3	0x1006 0010	R	DMA 3 current source address register	Undefined

DMACSRCn	Bit	Description	Initial State
CSADDR	[29:0]	Shows the current source address	Undefine

DMA CURRENT DESTINATION ADDRESS REGISTER (DMACSRCn)

Register	Address	R/W	Description	Reset Value
DMACDES0	0x1003 0014	R	DMA 0 current destination address register	Undefined
DMACDES1	0x1004 0014	R	DMA 1 current destination address register	Undefined
DMACDES2	0x1005 0014	R	DMA 2 current destination address register	Undefined
DMACDES3	0x1006 0014	R	DMA 3 current destination address register	Undefined

DMACDESn	Bit	Description	Initial State
CDADDR	[29:0]	Shows the current destination address	Undefine

DMA MASK TRIGGER REGISTER (MASKTRIGn)

Register	Address	R/W	Description	Reset Value
MASKTRIG0	0x1003 0018	R/W	DMA 0 mask trigger register	Undefined
MASKTRIG1	0x1004 0018	R/W	DMA 0 mask trigger register	Undefined
MASKTRIG2	0x1005 0018	R/W	DMA 0 mask trigger register	Undefined
MASKTRIG3	0x1006 0018	R/W	DMA 0 mask trigger register	Undefined

MASKTRIGn	Bit	Description	Initial State
MASK	[1]	The mask bit. 0 = Masked off the DMA request to this DMA controller is masked off and not handled. 1 = Not masked DMA request is not masked and can be handled.	Undefined
SWTRIG	[0]	The software trigger If it is 1, it requests a DMA operation to this controller. However, note that for this trigger to have real effects software request has to be selected (bit 23 of DMACONn) and mask bit has to be 1. If these conditions are met and DMA controller receives the request, this bit is automatically cleared.	Undefined

DMA Register

Register	Address	R/W	Description	Reset Value
DMASRC0	0x1003 0000	R/W	DMA 0 Source address register	0x0000 0000
DMADES0	0x1003 0004	R/W	DMA 0 Destination address register	0x0000 0000
DMACON0	0x1003 0008	R/W	DMA 0 control register	0x0000 0000
DMASTS0	0x1003 000C	R	DMA 0 status register	Undefined
DMACSRC0	0x1003 0010	R	DMA 0 current source address register	Undefined
DMACDES0	0x1003 0014	R	DMA 0 current destination address register	Undefined
MASKTRIG0	0x1003 0018	R/W	DMA 0 mask trigger register	Undefined
DMASRC1	0x1004 0000	R/W	DMA 1 Source address register	0x0000 0000
DMADES1	0x1004 0004	R/W	DMA 1 Destination address register	0x0000 0000
DMACON1	0x1004 0008	R/W	DMA 1 control register	0x0100 0000
DMASTS1	0x1004 000C	R	DMA 1 status register	Undefined
DMACSRC1	0x1004 0010	R	DMA 1 current source address register	Undefined
DMACDES1	0x1004 0014	R	DMA 1 current destination address register	Undefined
MASKTRIG1	0x1004 0018	R/W	DMA 0 mask trigger register	Undefined
DMASRC2	0x1005 0000	R/W	DMA 2 Source address register	0x0000 0000
DMADES2	0x1005 0004	R/W	DMA 2 Destination address register	0x0000 0000
DMACON2	0x1005 0008	R/W	DMA 2 control register	0x0200 0000
DMASTS2	0x1005 000C	R	DMA 2 status register	Undefined
DMACSRC2	0x1005 0010	R	DMA 2 current source address register	Undefined
DMACDES2	0x1005 0014	R	DMA 2 current destination address register	Undefined
MASKTRIG2	0x1005 0018	R/W	DMA 0 mask trigger register	Undefined
DMASRC3	0x1006 0000	R/W	DMA 3 Source address register	0x0000 0000
DMADES3	0x1006 0004	R/W	DMA 3 Destination address register	0x0000 0000
DMACON3	0x1006 0008	R/W	DMA 3 control register	0x0300 0000
DMASTS3	0x1006 000C	R	DMA 3 status register	Undefined
DMACSRC3	0x1006 0010	R	DMA 3 current source address register	Undefined
DMACDES3	0x1006 0014	R	DMA 3 current destination address register	Undefined
MASKTRIG3	0x1006 0018	R/W	DMA 0 mask trigger register	Undefined

5 I/O PORTS(Preliminary)

OVERVIEW

S3C2800X has 48 multi-functional input/output port pins. There are six ports:

— Six 8-bit input/output ports.

Each port can be easily configured by software to meet various system configuration and design requirements. You have to define which function of each pin is used before starting the main program. If the multiplexed functions on a pin are not used, the pin can be configured as I/O ports.

The initial pin states, before pin configurations, are configured elegantly to avoid some problems.

Table 5-1. S3C2800X Port Configuration Overview

Port A	Selectable Pin functions	
	Function 1	Function 2
GPA0	Input/output	nSCS1
GPA1	Input/output	nSCS2
GPA2	Input/output	nSCS3
GPA3	Input/output	nSDCS1/nDRAS1
GPA4	Input/output	nSDCS2/nDRAS2
GPA5	Input/output	nSDCS3/nDRAS3
GPA6	Input/output	nDCAS0
GPA7	Input/output	nDCAS1

Port B	Selectable Pin functions	
	Function 1	Function 2
GPB0	Input/output	nDCAS2/nSDCAS
GPB1	Input/output	nDCAS3/nSDRAS
GPB2	Input/output	nBE0/nWBE0/DQM0
GPB3	Input/output	nBE1/nWBE1/DQM1
GPB4	Input/output	nBE2/nWBE2/DQM2
GPB5	Input/output	nBE3/nWBE3/DQM3
GPB6	Input/output	nWAIT
GPB7	Input/output	CLKout

Port C	Selectable Pin functions	
	Function 1	Function 2
GPC0	Input/output	-
GPC1	Input/output	-
GPC2	Input/output	-
GPC3	Input/output	-
GPC4	Input/output	-
GPC5	Input/output	-
GPC6	Input/output	-
GPC7	ENDIAN	output only-

NOTE : ENDIAN(GPC7) is used only when nRESET is Low**.**

Table 5-1. S3C2800X Port Configuration Overview (Continued)

Port D	Selectable Pin functions	
	Function 1	Function 2
GPD0	Input/output	IICSDA0
GPD1	Input/output	IICSCLK0
GPD2	Input/output	IICSDA1
GPD3	Input/output	IICSCLK1
GPD4	Input/output	RxD0
GPD5	Input/output	TxD0
GPD6	Input/output	nCTS0
GPD7	Input/output	nRTS0

Port E	Selectable Pin functions	
	Function 1	Function 2
GPE0	Input/output	RxD1
GPE1	Input/output	TxD1
GPE2	Input/output	nCTS1
GPE3	Input/output	nRTS1
GPE4	Input/output	nXDREQ0
GPE5	Input/output	nXDACK0
GPE6	Input/output	nXDREQ1
GPE7	Input/output	nXDACK1

Port F	Selectable Pin functions	
	Function 1	Function 2
GPF0	Input/output	EXTINT0
GPF1	Input/output	EXTINT1
GPF2	Input/output	EXTINT2
GPF3	Input/output	EXTINT3
GPF4	Input/output	EXTINT4
GPF5	Input/output	EXTINT5
GPF6	Input/output	EXTINT6
GPF7	Input/output	EXTINT7

NOTES:

1. The underlined function name is selected just after a reset.
2. IICSDAn and IICSCLKn pins are open-drain pin. So, this pin needs pull-up resisters when used as output port(GPD[3:0]).

PORT CONTROL DESCRIPTIONS

PORT CONFIGURATION REGISTER (PCONA-F)

In S3C2800X, most pins are multiplexed pins. So, It is determined which function is selected for each pins. The PCONn (port control register) determines which function is used for each pin.

If GPF0 – GPF7 is used for the wakeup signal in power down mode, these ports must be configured in interrupt mode.

PORT DATA REGISTER (PDATA-F)

If Ports are configured as output ports, data can be written to the corresponding bit of PDATn. If Ports are configured as input ports, the data can be read from the corresponding bit of PDATn.

PORT PULL-UP REGISTER (PUPA-F)

The port pull-up register controls the pull-up resister enable/disable of each port group. When the corresponding bit is 0, the pull-up resister of the pin is enabled. When 1, the pull-up resister is disabled.

EXTERNAL INTERRUPT CONTROL REGISTER

The 8 external interrupts are requested by various signaling methods. The EXTINT register configures the signaling method among the low level trigger, high level trigger, falling edge trigger, rising edge trigger, and both edge trigger for the external interrupt request

Because each external interrupt pin has a digital filter, the interrupt controller can recognize the request signal that is longer than 3 clocks.

I/O PORT CONTROL REGISTER

PORT A CONTROL REGISTERS (PCONA, PDATA, PUPA)

Port A control registers are shown in Table 8-2:

Register	Address	R/W	Description	Reset Value
PCONA	0x1010 0000	R/W	Configures the pins of port A	0x0000 FFFF
PDATA	0x1010 0004	R/W	The data register for port A	Undef.
PUPA	0x1010 0008	R/W	Pull-up disable register for port A	0x0000 0000

Table 5-2. Port of Group A Control Registers (PCONA,PDATA,PUPA)

PCONA	Bit	Description
GPA7	[15:14]	00 = Input 01 = Output 1x = nDCAS1
GPA6	[13:12]	00 = Input 01 = Output 1x = nDCAS0
GPA5	[11:10]	00 = Input 01 = Output 1x = nSDCS3/nDRAS3
GPA4	[9:8]	00 = Input 01 = Output 1x = nSDCS2/nDRAS2
GPA3	[7:6]	00 = Input 01 = Output 1x = nSDCS1/nDRAS1
GPA2	[5:4]	00 = Input 01 = Output 1x = nSCS3
GPA1	[3:2]	00 = Input 01 = Output 1x = nSCS2
GPA0	[1:0]	00 = Input 01 = Output 1x = nSCS1

PDATA	Bit	Description
GPA[7:0]	[7:0]	When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.

PUPA	Bit	Description
GPA[7:0]	[7:0]	0: the pull up register attached to to the corresponding port pin is enabled. 1: the pull up register is disabled.

PORT B CONTROL REGISTERS (PCONB, PDATB, PUPB)

Port B control registers are shown in Table 5-3:

Register	Address	R/W	Description	Reset Value
PCONB	0x1010 000C	R/W	Configures the pins of port B	0x0000 0FFF
PDATB	0x1010 0010	R/W	The data register for port B	Undef.
PUPB	0x1010 0014	R/W	Pull-up disable register for port B	0x0000 0000

Table 5-3. Port of Group C Control Registers (PCONB,PDATB,PUPB)

PCONB	Bit	Description
GPB7	[15:14]	00 = Input 01 = Output 1x = AHBCLK out
GPB6	[13:12]	00 = Input 01 = Output 1x = nWAIT
GPB5	[11:10]	00 = Input 01 = Output 1x = nBE3/nWBE3/DQM3
GPB4	[9:8]	00 = Input 01 = Output 1x = nBE2/nWBE2/DQM2
GPB3	[7:6]	00 = Input 01 = Output 1x = nBE1/nWBE1/DQM1
GPB2	[5:4]	00 = Input 01 = Output 1x = nBE0/nWBE0/DQM0
GPB1	[3:2]	00 = Input 01 = Output 1x = nDCAS3/nSDRAS
GPB0	[1:0]	00 = Input 01 = Output 1x = nDCAS2/nSDCAS

PDATA	Bit	Description
GPB[7:0]	[7:0]	When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.

PUPA	Bit	Description
GPB[7:0]	[7:0]	0: the pull up register attached to to the corresponding port pin is enabled. 1: the pull up register is disabled.

PORT C CONTROL REGISTERS (PCONC, PDATC, PUPC)

Port C control registers are shown in Table 5-4:

Register	Address	R/W	Description	Reset Value
PCONC	0x1010 0018	R/W	Configures the pins of port C	0x0000 0000
PDATC	0x1010 001C	R/W	The data register for port C	Undef.
PUPC	0x1010 0020	R/W	Pull-up disable register for port C	0x0000 0000

Table 5-4. Port of Group C Control Registers (PCONC,PDATC,PUPC)

PCONC	Bit	Description
GPC7	[15:14]	0x = Reserved(ENDIAN) 1x = Output GPC7 can be used as ENDIAN only during reset cycle. It is written by 1x to use output state
GPC6	[13:12]	0x = Input 1x = Output
GPC5	[11:10]	0x = Input 1x = Output
GPC4	[9:8]	0x = Input 1x = Output
GPC3	[7:6]	0x = Input 1x = Output
GPC2	[5:4]	0x = Input 1x = Output
GPC1	[3:2]	0x = Input 1x = Output
GPC0	[1:0]	0x = Input 1x = Output

PDATC	Bit	Description
GPC[7:0]	[7:0]	When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.

PUPC	Bit	Description
GPC[6:0]	[6:0]	0 : the pull up register attached to to the corresponding port pin is enabled. 1 : the pull up register is disabled. GPC7 don't have programmale pull-up register.

PORT D CONTROL REGISTERS (PCOND, PDATD, PUPD)

Port D control registers are shown in Table 5-5:

Register	Address	R/W	Description	Reset Value
PCOND	0x1010 0024	R/W	Configures the pins of port D	0x0000 0000
PDATD	0x1010 0028	R/W	The data register for port D	Undef.
PUPD	0x1010 002C	R/W	Pull-up disable register for port D	0x0000 0000

Table 5-5. Port of Group D Control Registers (PCOND,PDATD,PUPD)

PCONA	Bit	Description
GPD7	[15:14]	00 = Input 01 = Output 1x = nRTS0
GPD6	[13:12]	00 = Input 01 = Output 1x = nCTS0
GPD5	[11:10]	00 = Input 01 = Output 1x = TxD0
GPD4	[9:8]	00 = Input 01 = Output 1x = RxD0
GPD3	[7:6]	00 = Input 01 = Output 1x = IICSCLK1
GPD2	[5:4]	00 = Input 01 = Output 1x = IICSDA1
GPD1	[3:2]	00 = Input 01 = Output 1x = IICSCLK0
GPD0	[1:0]	00 = Input 01 = Output 1x = IICSDA0

PDATD	Bit	Description
GPD[7:0]	[7:0]	When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.

PUPD	Bit	Description
GPD[7:0]	[7:0]	0: the pull up register attached to to the corresponding port pin is enabled. 1: the pull up register is disabled.

PORT E CONTROL REGISTERS (PCONE, PDATE, PUPE)

Port E control registers are shown in Table 5-6:

Register	Address	R/W	Description	Reset Value
PCONE	0x1010 0030	R/W	Configures the pins of port E	0x0000 0000
PDATE	0x1010 0034	R/W	The data register for port E	Undef.
PUPE	0x1010 0038	R/W	Pull-up disable register for port E	0x0000 0000

Table 5-6. Port of Group E Control Registers (PCONE,PDATE,PUPE)

PCONB	Bit	Description
GPE7	[15:14]	00 = Input 01 = Output 1x = nXDACK1
GPE6	[13:12]	00 = Input 01 = Output 1x = nXDREQ1
GPE5	[11:10]	00 = Input 01 = Output 1x = nXDACK0
GPE4	[9:8]	00 = Input 01 = Output 1x = nXDREQ0
GPE3	[7:6]	00 = Input 01 = Output 1x = nRTS1
GPE2	[5:4]	00 = Input 01 = Output 1x = nCTS1
GPE1	[3:2]	00 = Input 01 = Output 1x = TxD1
GPE0	[1:0]	00 = Input 01 = Output 1x = RxD1

PDATE	Bit	Description
GPE[7:0]	[7:0]	When the port is configured as an output port, the pin state is the same as the corresponding bit. When the port is configured as a functional pin, the undefined value will be read.

PUPE	Bit	Description
GPE[7:0]	[7:0]	0: the pull up register attached to to the corresponding port pin is enabled. 1: the pull up register is disabled.

PORT F CONTROL REGISTERS (PCONF, PDATF, PUPF)

Port F control registers are shown in Table 5-7:

If GPF0 - GPF7 will be used for wake-up signals at power down mode, the ports will be set in interrupt mode.

Register	Address	R/W	Description	Reset Value
PCONF	0x1010 003C	R/W	Configures the pins of port F	0x0000 0000
PDATF	0x1010 0040	R/W	The data register for port F	Undef.
PUPF	0x1010 0044	R/W	Pull-up disable register for port F	0x0000 0000

Table 5-7. Port of Group F Control Registers (PCONF, PDATF, PUPF)

PCONF	Bit	Description
GPF7	[15:14]	00 = Input 01 = Output 1x = EXTINT7
GPF6	[13:12]	00 = Input 01 = Output 1x = EXTINT6
GPF5	[11:10]	00 = Input 01 = Output 1x = EXTINT5
GPF4	[9:8]	00 = Input 01 = Output 1x = EXTINT4
GPF3	[7:6]	00 = Input 01 = Output 1x = EXTINT3
GPF2	[5:4]	00 = Input 01 = Output 1x = EXTINT2
GPF1	[3:2]	00 = Input 01 = Output 1x = EXTINT1
GPF0	[1:0]	00 = Input 01 = Output 1x = EXTINT0

PDATF	Bit	Description
GPF[7:0]	[7:0]	When the port is configured as an input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as a functional pin, the undefined value will be read.

PUPF	Bit	Description
GPF[7:0]	[7:0]	0: the pull up register attached to to the corresponding port pin is enabled. 1: the pull up register is disabled.

EXTINTR (EXTERNAL INTERRUPT CONTROL REGISTER)

The 8 external interrupts can be requested by various signaling methods. The EXTINTR register configures the signaling method between the level trigger and edge trigger for the external interrupt request, and also configures the signal polarity.

Register	Address	R/W	Description	Reset Value
EXTINTR	0x1010 0048	R/W	External Interrupt control Register	0x0000 0000

Table 5-8. External Interrupt Control Register (EXTINTR)

EXTINT	Bit	Description
EXTINT7	[30:28]	Setting the signaling method of the EXTINT7. 000 = Low level interrupt 001 = High level interrupt 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EXTINT6	[26:24]	Setting the signaling method of the EXTINT6. 000 = Low level interrupt 001 = High level interrupt 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EXTINT5	[22:20]	Setting the signaling method of the EXTINT5. 000 = Low level interrupt 001 = High level interrupt 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EXTINT4	[18:16]	Setting the signaling method of the EXTINT4. 000 = Low level interrupt 001 = High level interrupt 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EXTINT3	[14:12]	Setting the signaling method of the EXTINT3. 000 = Low level interrupt 001 = High level interrupt 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EXTINT2	[10:8]	Setting the signaling method of the EXTINT2. 000 = Low level interrupt 001 = High level interrupt 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EXTINT1	[6:4]	Setting the signaling method of the EXTINT1. 000 = Low level interrupt 001 = High level interrupt 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EXTINT0	[2:0]	Setting the signaling method of the EXTINT0. 000 = Low level interrupt 001 = High level interrupt 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered

NOTE: Because each external interrupt pins has a digital filter, the interrupt controller can recognize a request signal that is longer than 3 clocks.

NOTES

GPIO Control Register

Register	Address	R/W	Description	Reset Value
PCONA	0x1010 0000	R/W	Configures the pins of port A	0x0000 FFFF
PDATA	0x1010 0004	R/W	The data register for port A	Undef.
PUPA	0x1010 0008	R/W	Pull-up disable register for port A	0x0000 0000
PCONB	0x1010 000C	R/W	Configures the pins of port B	0x0000 0FFF
PDATB	0x1010 0010	R/W	The data register for port B	Undef.
PUPB	0x1010 0014	R/W	Pull-up disable register for port B	0x0000 0000
PCONC	0x1010 0018	R/W	Configures the pins of port C	0x0000 0000
PDATC	0x1010 001C	R/W	The data register for port C	Undef.
PUPC	0x1010 0020	R/W	Pull-up disable register for port C	0x0000 0000
PCOND	0x1010 0024	R/W	Configures the pins of port D	0x0000 0000
PDATD	0x1010 0028	R/W	The data register for port D	Undef.
PUPD	0x1010 002C	R/W	Pull-up disable register for port D	0x0000 0000
PCONE	0x1010 0030	R/W	Configures the pins of port E	0x0000 0000
PDATE	0x1010 0034	R/W	The data register for port E	Undef.
PUPE	0x1010 0038	R/W	Pull-up disable register for port E	0x0000 0000
PCONF	0x1010 003C	R/W	Configures the pins of port F	0x0000 0000
PDATF	0x1010 0040	R/W	The data register for port F	Undef.
PUPF	0x1010 0044	R/W	Pull-up disable register for port F	0x0000 0000
EXTINTR	0x1010 0048	R/W	External Interrupt control Register	0x0000 0000

6 16-BIT TIMERS(Preliminary)

OVERVIEW

The S3C2800X has the three 16-bit timers, each of timer can operate in interrupt-based or DMA-based mode. The Timers 0, 1, 2, These timers can operate in interval mode.

The timer 0,1,2 have an 8-bit prescaler. Each timer has a clock-divider which has 4 different divided signals (1/4, 1/8, 1/16, 1/32). Each timer block receives its own clock signals from the clock-divider which receives the clock from the corresponding 8-bit prescaler. The 8-bit prescaler is programmable and divides the APBCLK signal depending on the loading value which is stored in TMDATAn register.

Each timer has its own 16-bit down-counter which is driven by the timer clock. When the down-counter reaches zero, the timer interrupt request is generated to inform the CPU that the timer operation is completed. When the timer counter reaches zero, the value of corresponding TMDATAn is automatically loaded into the down-counter to continue the next operation. However, if the timer stops, for example, by clearing the count enable bit of TMCONn during the timer running mode, the value of TMDATAn will not be reloaded into the counter.

FEATURE

— Three 16-bit timers with DMA-based or interrupt-based operation

— Three 8-bit prescalers & Three 5-bit dividers

— Auto reload operation

— Max frequency source is 50MHz (APBCLKmax=50MHz@AHBCLK=50MHz)

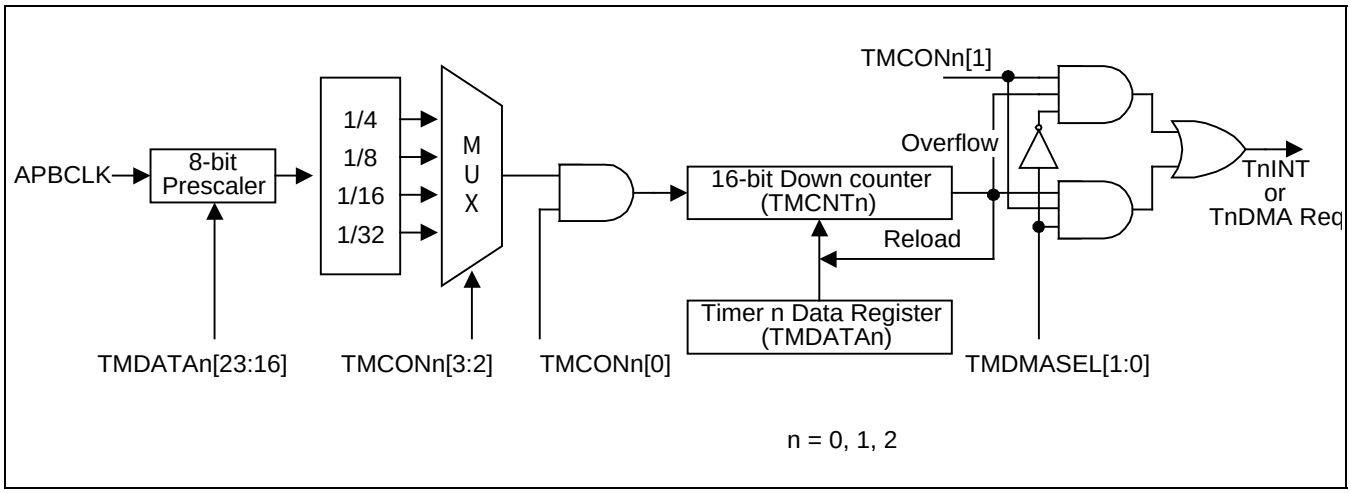


Figure 6-1. 16-bit Timer Block Diagram

16-BIT TIMER OPERATION

PRESCALER & DIVIDER

8-bit prescaler & independent divider make following output frequencies: (APBCLKmax = 50MHz)

Table 6-1. Example for interval timing.

Ddivider settings	Minimum resolution (prescaler = 1)	Maximum resolution (prescaler = 255)	maximum interval (TCNTBn = 65535)
1/4 (APBCLK = 50 MHz)	0.16 us (6.25 MHz)	20.48 us (48.83 KHz)	1.342 sec
1/8 (APBCLK = 50 MHz)	0.32 us (3.125 MHz)	40.96 us (24.42 KHz)	2.684 sec
1/16 (APBCLK = 50 MHz)	0.64 us (1.563 MHz)	81.92 us (12.21 KHz)	5.368 sec
1/32 (APBCLK = 50 MHz)	1.28 us (0.782 MHz)	163.84 us (6.11 KHz)	10.736 sec
1/4 (APBCLK = 37.5 MHz)	0.21 us (4.688 MHz)	27.31 us (36.62 KHz)	1.786 sec
1/8 (APBCLK = 37.5 MHz)	0.42 us (2.344 MHz)	54.61 us (18.31 KHz)	3.579 sec
1/16 (APBCLK = 37.5 MHz)	0.84 us (1.172 MHz)	109.22 us (9.16 KHz)	7.158 sec
1/32 (APBCLK = 37.5 MHz)	1.71 us (0.586 MHz)	218.44 us (4.58 KHz)	14.316 sec

DMA REQUEST MODE

The timer can generate DMA request every specific times. The timer keeps DMA request signal low until the timer receive the ACK signal. When receives the ACK signal, it makes the request signal inactive. One of 3 timers can generate DMA request. The timer, that generates the DMA request, is determined by setting DMA mode bits(in TMCON1 register). If a timer is configured as DMA request mode, the timer does not generate an interrupt request. The others can generate interrupt normally.

DMA MODE CONFIGURATION AND DMA / INTERRUPT OPERATION

DMA mode	DMA request	Timer0 INT	Timer1 INT	Timer2 INT
00	No select	ON	ON	ON
01	Timer0	OFF	ON	ON
10	Timer1	ON	OFF	ON
11	Timer2	ON	ON	OFF

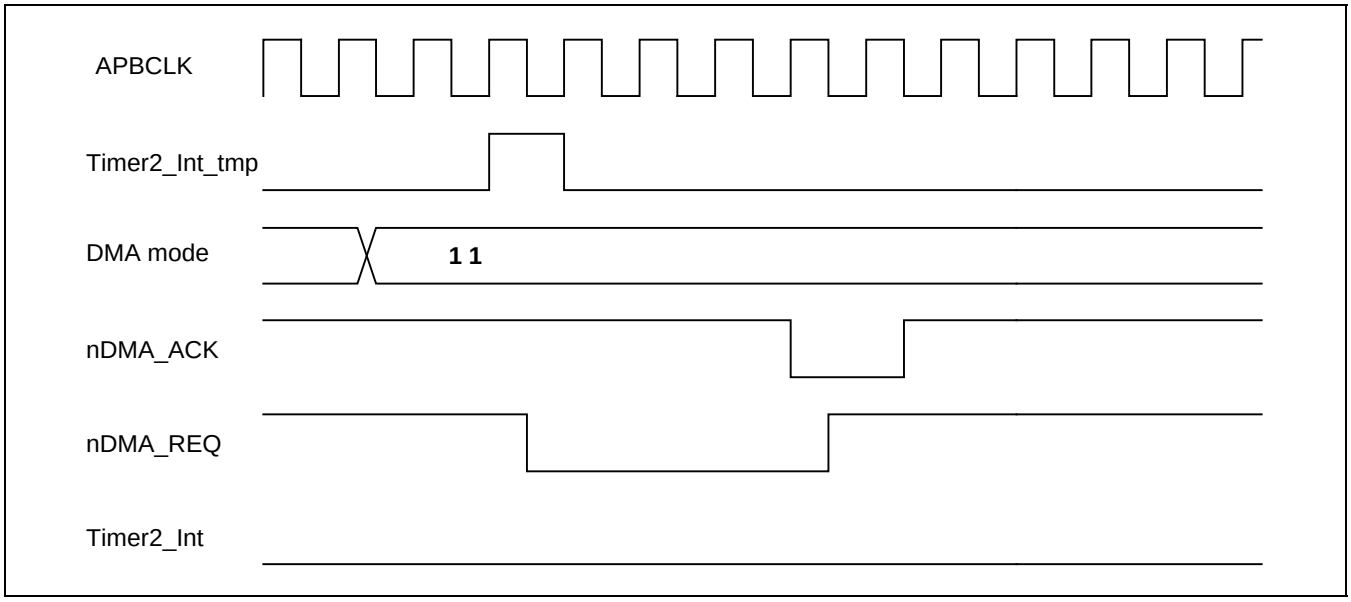


Figure 6-2. The Timer2 DMA mode operation

TIMER CONTROL REGISTERS

TIMER DMA SELECTION REGISTER1 (TMDMA)

Register	Address	R/W	Description	Reset Value
TMDMASEL	0x1013 000C	R/W	DMA or Interrupt mode selecton register	0x0000 0000

TMDMASEL	Bit	Description	Initial State
DMA mode	[1:0]	Select DMA request channel 00 = No select(All interrupt) 01 = Timer0 10 = Timer1 11 = Timer2	0

TIMER CONTROL REGISTER0 (TMCON0 ~ TMCON2)

Timer input clock Frequency = APBCLK / {prescaler value+1} / {divider value}
{prescaler value} = 1~255 (TMDATAn[23:16])
{divider value} = 4,8,16,32

Register	Address	R/W	Description	Reset Value
TMCON0	0x1013 0000	R/W	Timer 0 control register	0x0000 0800
TMCON1	0x1014 0000	R/W	Timer 1 control register	0x0000 0800
TMCON2	0x1015 0000	R/W	Timer 2 control register	0x0000 0800

TMCONn	Bit	Description	Initial State
MUX	[3:2]	Select MUX input 00 = 1/4 01 = 1/8 10 = 1/16 11 = 1/32	00
Interrupt/DMA Enable	[1]	Interrupt or DMA Enable 0 = Disable 1 = Enable	0
Count Enable	[0]	Timer down counter run or stop 0 = Stop 1 = Run This bit enables or disables timer. When the bit is set to “0”, the 16-bit down counter is clear to “0x0000”, and then it is stops. When it is “1”, the 16-bit timer down counter starts counting again after reload the timer data value and pre-scaler value, and then the counter value decrements by one on accepting every clock.	0

TIMER DATA REGISTER (TMDATAn)

The timer data registers, TMDATA0, TMDATA1, and TMDATA2, contain a value that specifies the time-out duration for each timer. The formula for calculating time-out duration is (Timer data + 1) cycles.

Register	Address	R/W	Description	Reset Value
TMDATA0	0x1013 0004	R/W	Timer 0 Data Register	0x0080 FFFF
TMDATA1	0x1014 0004	R/W	Timer 1 Data Register	0x0080 FFFF
TMDATA2	0x1015 0004	R/W	Timer 2 Data Register	0x0080 FFFF

TMDATAn	Bit	Description	Initial State
Pre-scaler	[23:16]	These 8 bits determine prescaler value (1 ~ 255) 0 = not supported.	0x80
Timer data value	[15:0]	[15:0] Timer data value This field specifies the time-out period of the corresponding timer. The time-out period is calculated as (Timer data + 1) cycles.Therefore, a maximum time-out period of 65,536 cycles is possible (when the timer data value is 0xffff). The minimum time-out period (2 cycles) is obtained by writing the value 0x0001h to the timer data register field.	0x0000 FFFF

TIMER COUNT REGISTER (TMCNTn)

The timer count registers, TMCNT0, TMCNT1, and TMCNT2, contain current timer 0, 1, and 2 count value, respectively. The timer count registers operate as a decrement counter.

Register	Address	R/W	Description	Reset Value
TMCNT0	0x1013 0008	R	Timer 0 count register	0x0000 FFFF
TMCNT1	0x1014 0008	R	Timer 1 count register	0x0000 FFFF
TMCNT2	0x1015 0008	R	Timer 2 count register	0x0000 FFFF

TMCNTn	Bit	Description	Initial State
Timer count value	[15:0]	[15:0] Counting value This field specifies the time-out period of the corresponding timer. The time-out period is calculated as (Timer data + 1) cycles.Therefore, a maximum time-out period of 65,536 cycles is possible (when the timer data value is 0xffff). The minimum time-out period (2 cycles) is obtained by writing the value 0x0001h to the timer data register field.	0x0000 FFFF

NOTES

Timer Register

Register	Address	R/W	Description	Reset Value
TMDMASEL	0x1013 000C	R/W	DMA or Interrupt mode selecton register	0x0000 0000
TMCON0	0x1013 0000	R/W	Timer 0 control register	0x0000 0000
TMDATA0	0x1013 0004	R/W	Timer 0 Data Register	0x0080 FFFF
TMCNT0	0x1013 0008	R	Timer 0 count register	0x0000 FFFF
TMCON1	0x1014 0000	R/W	Timer 1 control register	0x0000 0000
TMDATA1	0x1014 0004	R/W	Timer 1 Data Register	0x0080 FFFF
TMCNT1	0x1014 0008	R	Timer 1 count register	0x0000 FFFF
TMCON2	0x1015 0000	R/W	Timer 2 control register	0x0000 0000
TMDATA2	0x1015 0004	R/W	Timer 2 Data Register	0x0080 FFFF
TMCNT2	0x1015 0008	R	Timer 2 count register	0x0000 FFFF

7 UART(Preliminary)

OVERVIEW

The S3C2800X UART (Universal Asynchronous Receiver and Transmitter) unit provides two independent asynchronous serial I/O ports, each of which can operate in interrupt-based or DMA-based mode. In other words, UART can generate an interrupt or DMA request to transfer data between CPU and UART. It can support bit rates of up to 230.4Kbps. Each UART channel contains two 16-byte FIFOs for receive and transmit.

The S3C2800X UART includes programmable baud-rates, infra-red (IR) transmit/receive, one or two stop bit insertion, 5-bit, 6-bit, 7-bit or 8-bit data width and parity checking.

Each UART contains a baud-rate generator, transmitter, receiver and control unit, as shown in Figure10-1. The baud-rate generator can be clocked by APBCLK. The transmitter and the receiver contain 16-byte FIFOs and data shifters. Data, which is to be transmitted, is written to FIFO and then copied to the transmit shifter. It is then shifted out by the transmit data pin (TxDn). The received data is shifted from the receive data pin (RxDn), and then copied to FIFO from the shifter.

FEATURE

— RxD0,TxD0,RxD1,TxD1 with DMA-based or interrupt-based operation

— UART Ch 0 with IrDA 1.0 & 16-byte FIFO

— UART Ch 1 with IrDA 1.0 & 16-byte FIFO

— Supports handshake transmit / receive

— Baud-rate(max) = 230.4Kbps

BLOCK DIAGRAM

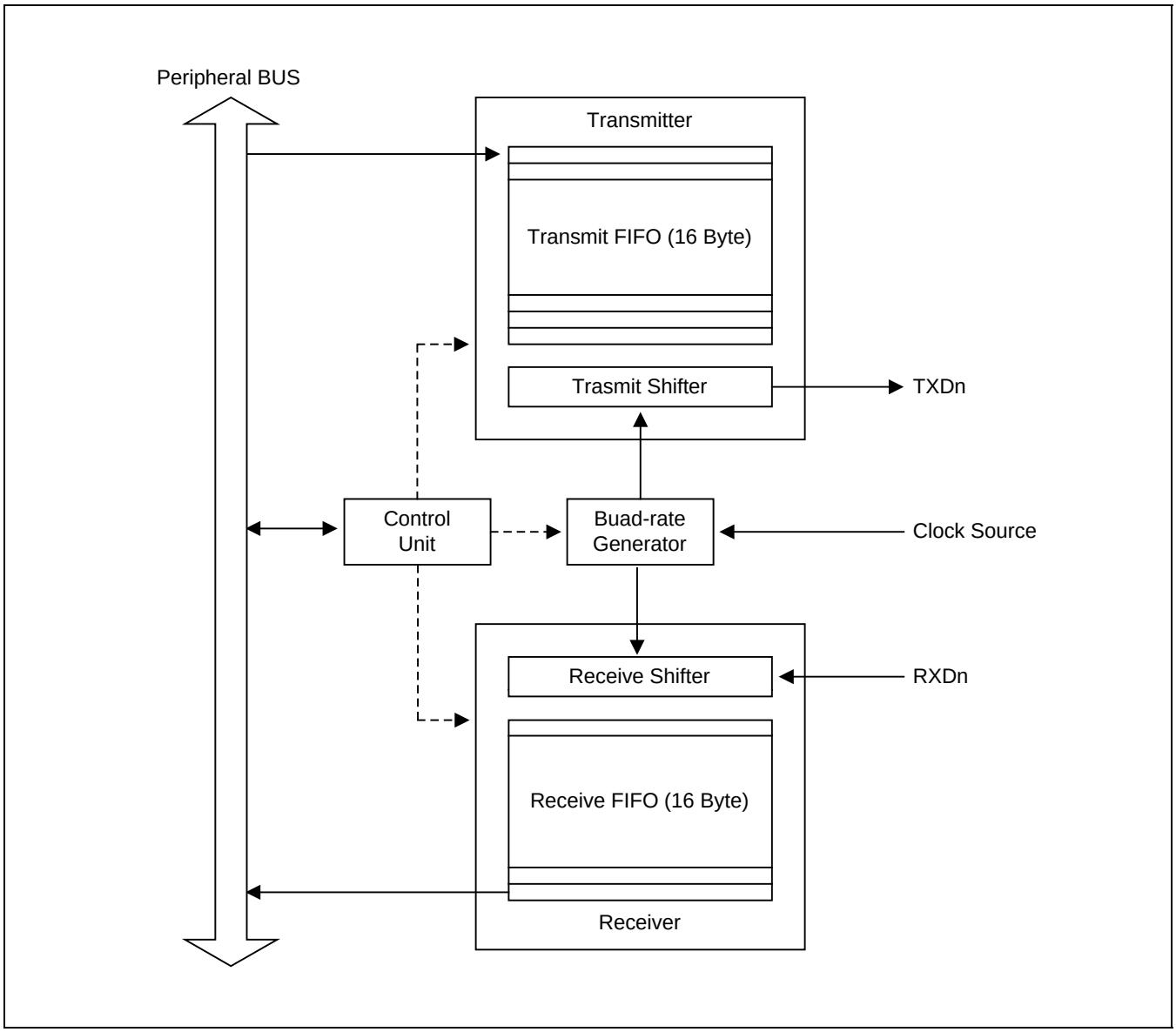


Figure 7-1. UART Block Diagram (with FIFO)

UART OPERATION

The following sections describe the UART operations that include data transmission, data reception, interrupt generation, baud-rate generation, loopback mode, infra-red mode, auto flow control.

Data Transmission

The data frame for transmission is programmable. It consists of a start bit, 5 to 8 data bits, an optional parity bit and 1 to 2 stop bits, which can be specified by the line control register (UCONn). The transmitter can also produce the break condition. The break condition forces the serial output to logic 0 state for a duration longer than one frame transmission time. This block transmit break signal after the present transmissive word transmits perfectly. After the break signal transmit, continously transmit data into the Tx FIFO (Tx holding register in the case of Non-FIFO mode).

Data Reception

Like the transmission, the data frame for reception is also programmable. It consists of a start bit, 5 to 8 data bits, an optional parity bit and 1 to 2 stop bits by settings in the line control register (UCONn). The receiver can detect overrun error, parity error, frame error and break condition, each of which can set an error flag.

- The overrun error indicates that new data has overwritten the old data before the old data has been read.
- The parity error indicates that the receiver has detected unexpected parity condition.
- The frame error indicates that the received data does not have a valid stop bit.
- The break condition indicates that the RxDn input is held in the logic 0 state for a duration longer than one frame transmission time.

Receive time-out condition occurs when it does not receive data during the 3 word time and the Rx FIFO is not empty state at FIFO mode.

Auto Flow Control(AFC)

S3C2800X's UART supports auto flow control with nRTS and nCTS signal, in this case should have to connect UART to UART. If users connect UART to Modem, disable auto flow control bit in UMCONn register and control the signal of nRTS by software.

In AFC, nRTS is controlled by condition of receiver and operation of transmitter is controlled by nCTS signal. The UART's transmitter transfer the data in FIFO only when nCTS signal is activated(In AFC, nCTS means that the other UART's FIFO is ready to receive data). Before the UART receives data, nRTS has to be activated when its receive FIFO has the spare more than 2-byte and has to be inactivated when its receive FIFO has the spare under 1-byte(In AFC, nRTS means that own receive FIFO is ready to receive data).

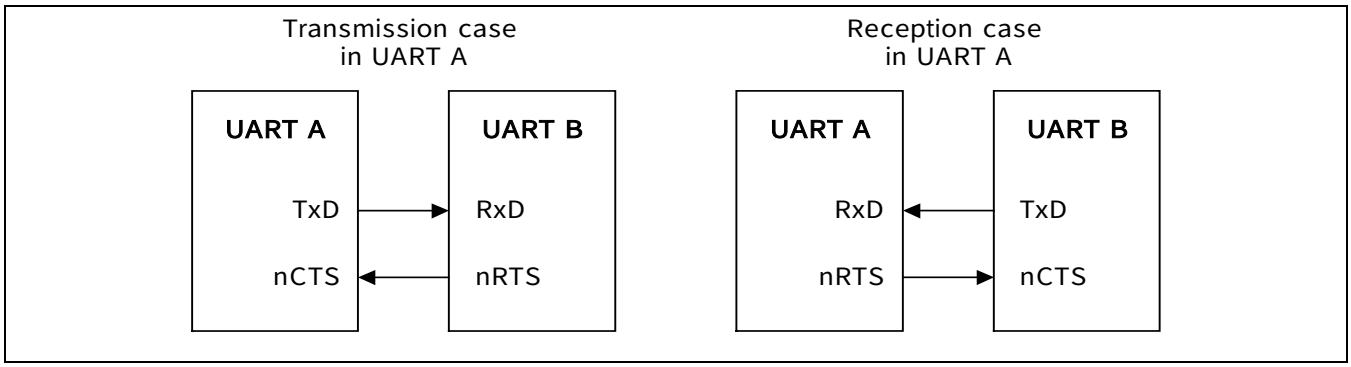


Figure 7-2. UART AFC interface

Non Auto-Flow control(Controlling nRTS and nCTS by S/W)

Rx operation

1. Select receive mode(Interrupt or DMA mode).

2. Check the value of Rx FIFO count in UFSTATn register. If the value is less than 15, users have to set the value of UMCONn[0] to '1'(activate nRTS), and if it is equal or larger than 15 users have to set the value to '0'(inactivate nRTS).

3. Repeat 2 item.

Tx operation

1. Select transmit mode(Interrupt or DMA mode)

2. Check the value of UMSTATn[0]. If only the value is '1'(nCTS is activated), users write the data in Tx buffer or Tx FIFO register.

RS-232C interface

If users connect to modem interface(not equal null modem), need nRTS, nCTS, nDSR, nDTR, DCD and nRI signals, In this case, users control these signals with general I/O ports by S/W because the AFC does not support RS-232C interface.

Interrupt/DMA Request Generation

Each UART of S3C2800X has seven status(Tx/Rx/Error) signals: Overrun error, Parity error, Frame error, Break, Receive FIFO/buffer data ready, Transmit FIFO/buffer empty, and Transmit shifter empty, all of which are indicated by the corresponding UART status register (UTRSTATn/UERSTATn).

The overrun error, parity error, frame error and break condition are referred to as the receive error status, each of which can cause the receive error status interrupt request, if the receive-error-status-interrupt-enable bit is set to one in the control register UCONn. When a receive-error-status-interrupt-request is detected, you can know the signal which causes the request by reading UERSTSTn.

When the receiver transfers the data of the receive shifter to the receive FIFO, it activates the receive FIFO full status signal which will cause the receive interrupt, if the receive mode in control register is selected as the interrupt mode.

When the transmitter transfers data from its transmit FIFO to its transmit shifter, the transmit FIFO empty status signal is activated. The signal causes the transmit interrupt if the transmit mode in control register is selected as that interrupt mode.

The receive-FIFO-full and transmit-FIFO-empty status signals can also be connected to generate the DMA request signals if the receive/transmit mode is selected as the DMA mode.

Table 7-1. Interrupts In Connection With FIFO

Type	FIFO Mode	Non-FIFO Mode
Rx interrupt	Each time receive data gets to the trigger level of receive FIFO, the Rx interrupt will be generated. When the FIFO is not empty and does not receive data during 3 word time, the Rx interrupt will be generated(receive time out).	Each time receive data becomes full receive shift register, generates interrupt.
Tx interrupt	Each time transmit data gets to the trigger level of transmit FIFO, the Tx interrupt will be generated.	Each time transmit data become empty, the transmit holding register generates interrupt.
Error interrupt	Framing error, parity error, and break signal are detected as each byte which is received, the error interrupt will be generated. When it gets to the top of the receive FIFO, the error interrupt will be generated(overrun error).	All errors generate an error interrupt immediately. However if another error occurs at the same time, only one interrupt is generated.

UART Error Status FIFO

UART has the status FIFO aside from the Rx FIFO register. The status FIFO indicates which data, among FIFO registers, is received with an error. The error interrupt will be issued only when the data, which has an error, is ready to read out. To clear the status FIFO, the URXHn, that has an error, and UERSTATn has to be read out.

For example,

It is assumed that the UART FIFO receives A, B, C, D, E characters sequentially, and the frame error is occurred while receiving the 'B' , and the frame error is occurred while receiving the 'D'.

Although the UART error has been occurred, the error interrupt will not occur because the character, which has been received with an error, is not read yet. The error interrupt will occur when the character is read out.

Time	Sequence flow	Error interrupt	Note
#0	When no character is read out	-	
#1	After A is read out	The frame error(in B) interrupt occurs	The 'B' has to be read out
#2	After B is read out	-	
#3	After C is read out	The parity error(in D) interrupt occurs	The 'D' has to be read out
#4	After D is read out	-	
#5	After E is read out	-	

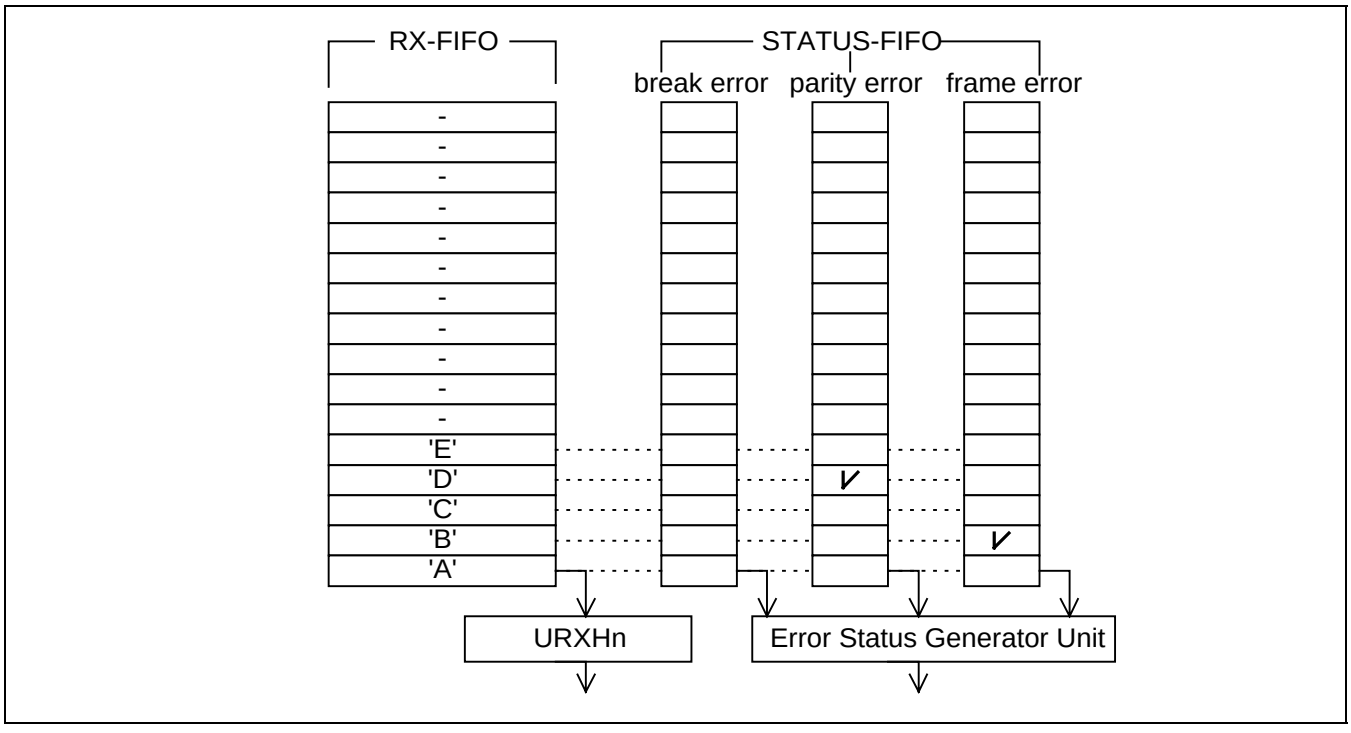


Figure 7-3. The Case that UART Receives 5 Characters Including 2 Errors

Baud-Rate Generation

Each UART's baud-rate generator provides the serial clock for transmitter and receiver. The source clock for the baud-rate generator can be selected with the S3C2800X's internal system clock. The baud-rate clock is generated by dividing the source clock by 16 and a 16-bit divisor specified by the UART baud-rate divisor register (UBRDIVn). The UBRDIVn can be determined as follows:

UBRDIVn = (round_off)(APBCLK/(bps x 16)) -1

where the divisor should be from 1 to (2^{16}-1). For example, if the baud-rate is 230400 bps and APBCLK is 37.5MHz , UBRDIVn is:

UBRDIVn = (int)(37500000/(230400 x 16)+0.5) -1
= (int)(10.2+0.5) -1
= 10 -1 = 9

Loop-back Mode

The S3C2800X UART provides a test mode referred to as the loopback mode, to aid in isolating faults in the communication link. In this mode, the transmitted data is immediately received. This feature allows the processor to verify the internal transmit and to receive the data path of each SIO channel. This mode can be selected by setting the loopback-bit in the UART control register (UCONn).

Break Condition

The break is defined as a continuous low level signal on the transmit data output with a duration more than one frame transmission time.

IR (Infra-Red) Mode

The S3C2800X UART block supports infra-red (IR) transmission and reception, which can be selected by setting the infra-red-mode bit in the UART control register (ULCONn). The implementation of the mode is shown in Figure 10-3.

In IR transmit mode, the transmit period is pulsed at a rate of 3/16 as at the normal serial transmit rate (when the transmit data bit is zero); In IR receive mode, the receiver must detect the 3/16 pulsed period to recognize a zero value (refer to the frame timing diagrams shown in Figures 10-5 and 10-6).

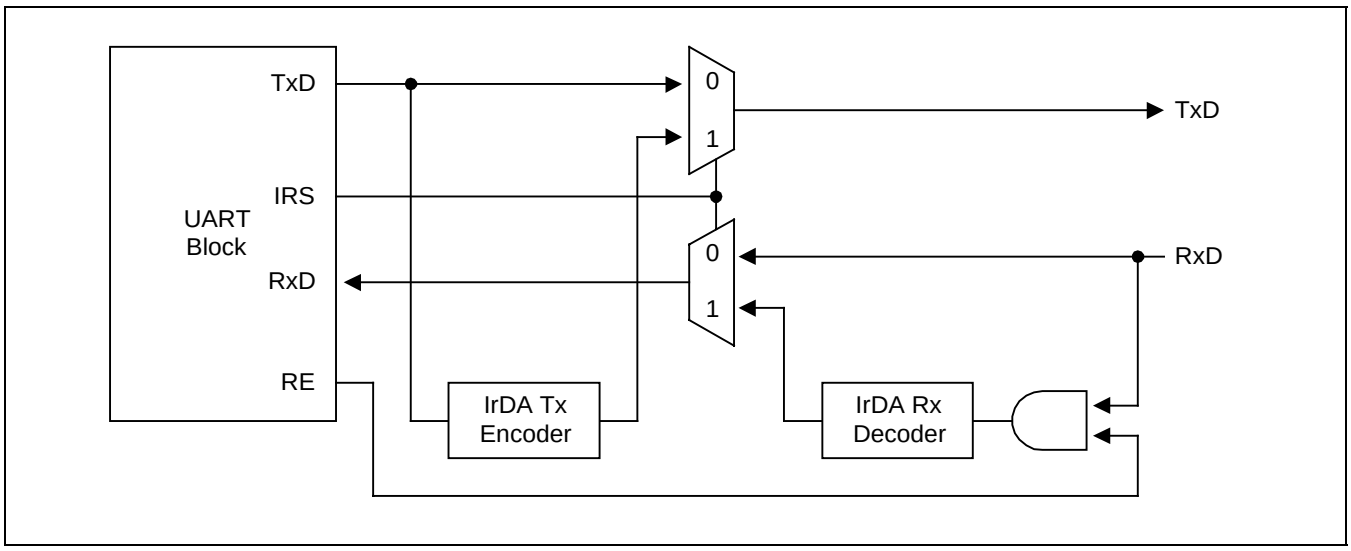


Figure 7-3. IrDA Function Block Diagram

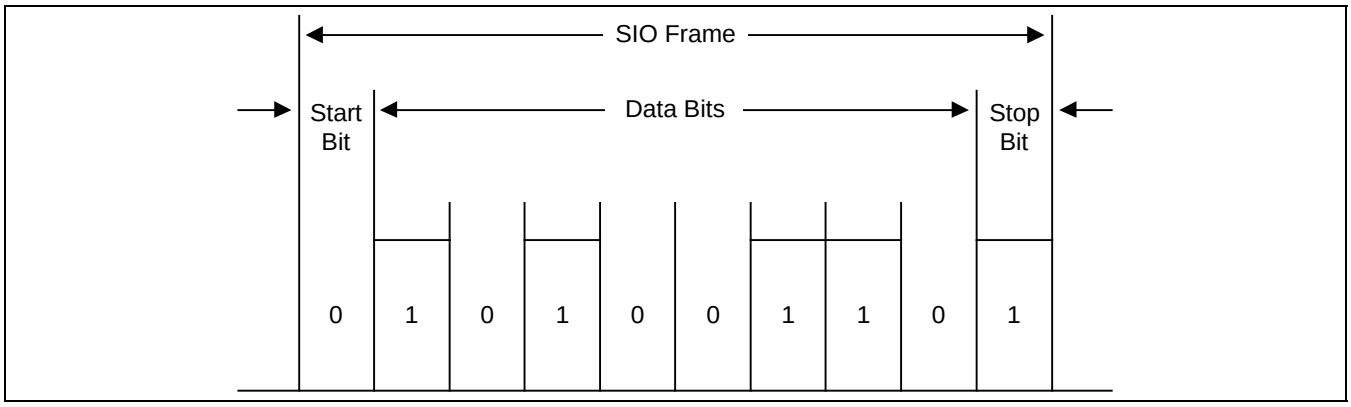


Figure 7-4. Serial I/O Frame Timing Diagram (Normal UART)

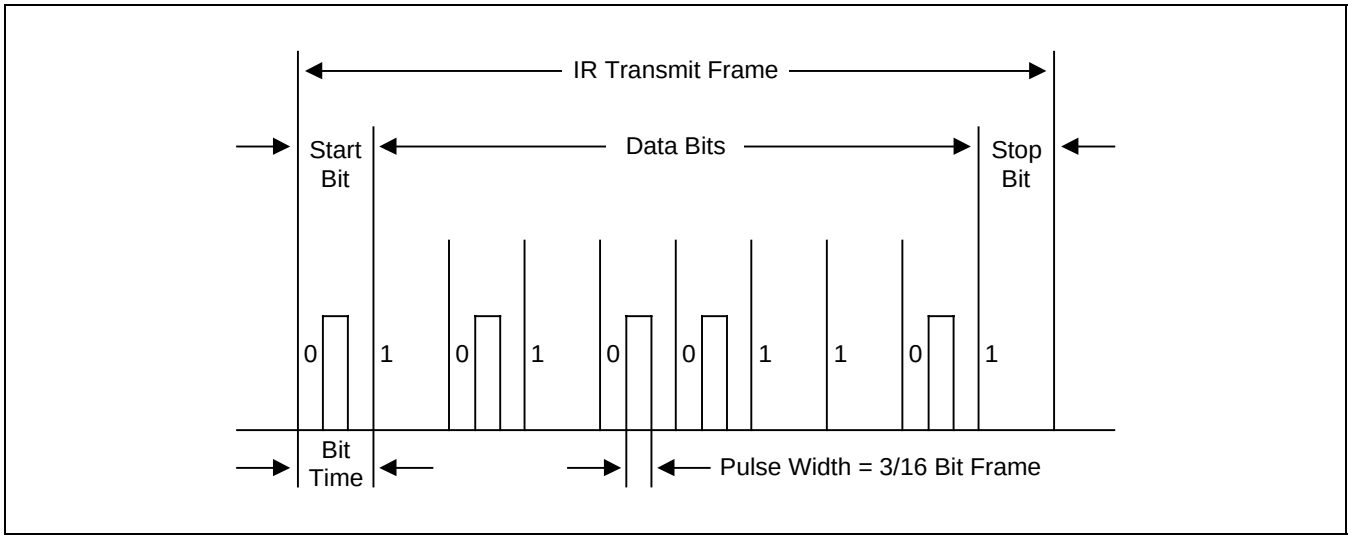


Figure 7-5. Infra-Red Transmit Mode Frame Timing Diagram

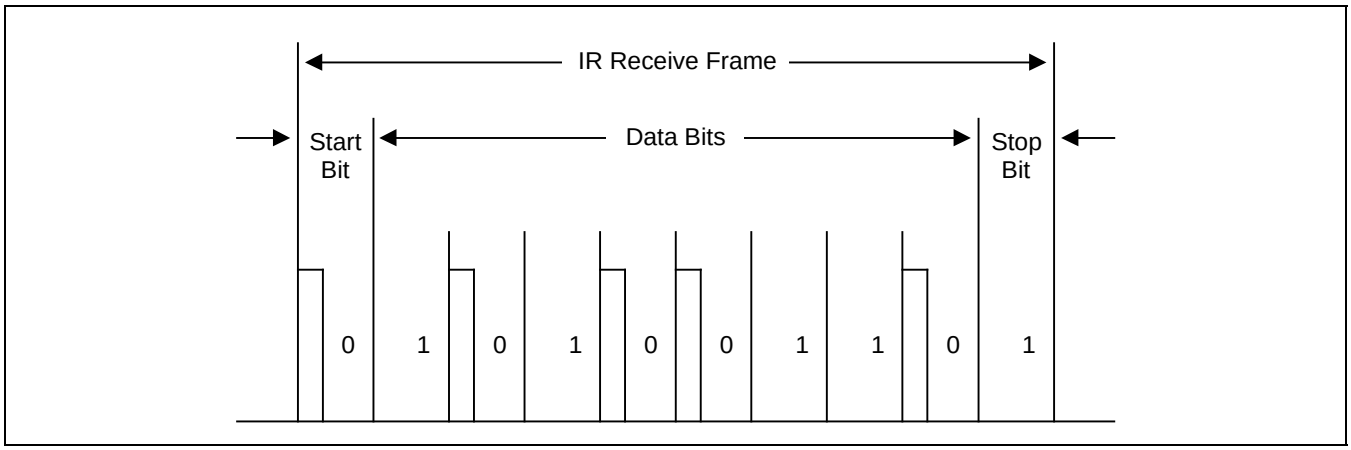


Figure 7-6. Infra-Red Receive Mode Frame Timing Diagram

UART SPECIAL REGISTERS

UART LINE CONTROL REGISTER

There are two UART line control registers, ULCON0 and ULCON1 in the UART block.

Register	Address	R/W	Description	Reset Value
ULCON0	0x1017 0000	R/W	UART channel 0 line control register	0x0000 0000
ULCON1	0x1018 0000	R/W	UART channel 1 line control register	0x0000 0000

ULCONn	Bit	Description	Initial State
Reserved	[31:8]	Reserved	0
Infra-Red Mode	[7]	The Infra-Red mode determines whether or not to use the Infra-Red mode. 0 = Normal mode operation 1 = Infra-Red Tx/Rx mode	0
Parity Mode	[6:4]	The parity mode specifies how parity generation and checking are to be performed during UART transmit and receive operation. 0xx = No parity 100 = Odd parity 101 = Even parity 110 = Parity forced/checked as 1 111 = Parity forced/checked as 0	000
Reserved	[3]	Reserved	0
Number of stop bit	[2]	The number of stop bits specify how many stop bits are use d to signal end-of-frame. 0 = One stop bit per frame 1 = Two stop bit per frame	0
Word length	[1:0]	The word length indicates the number of data bits to be transmitted or received per frame. 00 = 5-bits 01 = 6-bits 10 = 7-bits 11 = 8-bits	00

UART CONTROL REGISTER

There are two UART control registers, UCON0 and UCON1 in the UART block.

Register	Address	R/W	Description	Reset Value
UCON0	0x1017 0004	R/W	UART channel 0 control register	0x0000 0000
UCON1	0x1018 0004	R/W	UART channel 1 control register	0x0000 0000

UCONn	Bit	Description	Initial State
Reserved	[31:10]	Reserved	
Tx interrupt type	[9]	Interrupt request type 0 = Pulse (Just when Tx buffer is empty) 1 = Level (While Tx buffer is empty)	0
Rx interrupt type	[8]	Interrupt request type 0 = Pulse (Just when Rx buffer receives the data) 1 = Level (While Rx buffer has the received data)	0
Rx time out enable	[7]	Enable/Disable Rx time out interrupt when UART FIFO is enabled. The interrupt is receive interrupt. 0 = Disable 1 = Enable	0
Rx error status interrupt enable	[6]	This bit enables the UART to generate an interrupt if an exception, such as a break, frame error, parity error, or overrun error occurs during a receive operation. 0 = Do not generate receive error status interrupt 1 = Generate receive error status interrupt	0
Loop-back Mode	[5]	Setting loop-back bit to 1 causes the UART to enter loop-back mode. This mode is provided for test purposes only. 0 = Normal operation 1 = Loop-back mode	0
Send Break Signal	[4]	Setting this bit causes the UART to send a break during 1 frame time. This bit is auto-cleared after sending break signal. 0 = Normal transmit 1 = Send break signal	0
Transmit Mode	[3:2]	These two bits determine which function is currently able to write Tx data to the UART transmit holding register. 00 = Disable 01 = Interrupt request 1x = DMA request	00
Receive Mode	[1:0]	These two bits determine which function is currently able to read data from UART receive buffer register. 00 = Disable, 01 = Interrupt request 1x = DMA request	00

UART FIFO CONTROL REGISTER

There are two UART FIFO control registers, UFCON0 and UFCON1 in the UART block.

Register	Address	R/W	Description	Reset Value
UFCON0	0x1017 0008	R/W	UART channel 0 FIFO control register	0x0000 0000
UFCON1	0x1018 0008	R/W	UART channel 1 FIFO control register	0x0000 0000

UFCONn	Bit	Description	Initial State
Reserved	[31:8]		0
Tx FIFO Trigger Level	[7:6]	These two bits determine trigger level of transmit FIFO. 00 = Empty 01 = 4-byte 10 = 8-byte 11 = 12-byte	00
Rx FIFO Trigger Level	[5:4]	These two bits determine trigger level of receive FIFO. 00 = 4-byte 01 = 8-byte 10 = 12-byte 11 = 16-byte	00
Reserved	[3]		0
Tx FIFO Reset	[2]	This bit is auto-cleared after resetting FIFO 0 = Normal 1= Tx FIFO reset	0
Rx FIFO Reset	[1]	This bit is auto-cleared after resetting FIFO 0 = Normal 1= Rx FIFO reset	0
FIFO Enable	[0]	0 = FIFO disable 1 = FIFO mode	0

Note : When the UART does not get to FIFO trigger level and does not receive data during 3 word time in DMA receive mode with FIFO, the Rx interrupt will be generated(receive time out), and users should have to check the FIFO status and read out the rest.

UART MODEM CONTROL REGISTER

There are two UART MODEM control registers, UMCON0 and UMCON1 in the UART block.

Register	Address	R/W	Description	Reset Value
UMCON0	0x1017 000C	R/W	UART channel 0 Modem control register	0x0000 0000
UMCON1	0x1018 000C	R/W	UART channel 1 Modem control register	0x0000 0000

UMCONn	Bit	Description	Initial State
Reserved	[31:2]	Reserved	
AFC(Auto Flow Control)	[1]	0 = Disable 1 = Enable	0
Request to Send	[0]	If AFC bit is enabled, this value will be ignored. In this case the S3C2800X will control nRTS automatically. If AFC bit is disabled, you have to control nRTS by S/W. 0 = 'H' level(Inactivate nRTS) 1 = 'L' level(Activate nRTS)	0

UART TX/RX STATUS REGISTER

There are two UART Tx/Rx status registers, UTRSTAT0 and UTRSTAT1 in the UART block.

Register	Address	R/W	Description	Reset Value
UTRSTAT0	0x1017 0010	R	UART channel 0 Tx/Rx status register	0x0000 0006
UTRSTAT1	0x1018 0010	R	UART channel 1 Tx/Rx status register	0x0000 0006

UTRSTATn	Bit	Description	Initial State
Reserved	[31:3]	Reserved	
Transmit shifter empty	[2]	This bit is automatically set to 1 when the transmit shift register has no valid data to transmit and the transmit shift register is empty. 0 = Not empty 1 = Transmit holding & shifter register empty	1
Transmit FIFO empty/ Transmit buffer empty	[1]	This bit is automatically set to 1 when the transmit FIFO/buffer register does not contain valid data. 0 = 1-byte ≤ FIFO ≤ 16-byte/The buffer register is not empty 1 = Empty	1
Receive FIFO data ready/ Receive buffer data ready	[0]	This bit is automatically set to 1 whenever the receive FIFO/buffer data register contains valid data received over the RXDn port. 0 = Completely empty 1 = 1-byte ≤ FIFO ≤ 16-byte/The buffer register has a received data	0

UART ERROR STATUS REGISTER

There are two UART Rx error status registers, UERSTAT0 and UERSTAT1 in the UART block.

Register	Address	R/W	Description	Reset Value
UERSTAT0	0x1017 0014	R	UART channel 0 Rx error status register	0x0000 0000
UERSTAT1	0x1018 0014	R	UART channel 1 Rx error status register	0x0000 0000

UERSTATn	Bit	Description	Initial State
Reserved	[31:4]	Reserved	
Break Detect	[3]	This bit is automatically set to 1 to indicate that a break signal has been received. 0 = No break receive 1 = Break receive	0
Frame Error	[2]	This bit is automatically set to 1 whenever a frame error occurs during receive operation. 0 = No frame error during receive 1 = Frame error	0
Parity Error	[1]	This bit is automatically set to 1 whenever a parity error occurs during receive operation. 0 = No parity error during receive 1 = Parity error	0
Overrun Error	[0]	This bit is automatically set to 1 whenever an overrun error occurs during receive operation. 0 = No overrun error during receive 1 = Overrun error	0

NOTE : These bits (UERSATn[3:0]) are automatically cleared to 0 when you read the UART error status register.

UART FIFO STATUS REGISTER

Only the UARTn has a 16-byte transmit FIFO & a 16-byte receive FIFO.

There are two UART FIFO status registers, UFSTAT0 and UFSTAT1 in the UART block.

Register	Address	R/W	Description	Reset Value
UFSTAT0	0x1017 0018	R	UART channel 0 FIFO status register	0x0000 0000
UFSTAT1	0x1018 0018	R	UART channel 1 FIFO status register	0x0000 0000

UFSTATn	Bit	Description	Initial State
Reserved	31:10]		0
Tx FIFO Full	[9]	This bit is automatically set to 1 whenever transmit FIFO is full during transmit operation 0 = 0-byte ≤ Tx FIFO data ≤ 15-byte 1 = Full	0
Rx FIFO Full	[8]	This bit is automatically set to 1 whenever receive FIFO is full during receive operation 0 = 0-byte ≤ Rx FIFO data ≤ 15-byte 1 = Full	0
Tx FIFO Count	[7:4]	Number of data in Tx FIFO	0
Rx FIFO Count	[3:0]	Number of data in Rx FIFO	0

UART MODEM STATUS REGISTER

There are two UART modem status register, UMSTAT0 and UMSTAT1 in the UART block.

Register	Address	R/W	Description	Reset Value
UMSTAT0	0x1017 001C	R	UART channel 0 Modem status register	0x0000 0000
UMSTAT1	0x1018 001C	R	UART channel 1 Modem status register	0x0000 0000

UMSTATn	Bit	Description	Initial State
Reserved	[31:2]	Reserved	0
Delta CTS	[1]	This bit indicates that the nCTS input to S3C2800X has changed state since the last time it was read by CPU. (Refer to Fig. 10-7) 0 = Has not changed 1 = Has changed	0
Clear to Send	[0]	0 = CTS signal is not activated(nCTS pin is high) 1 = CTS signal is activated(nCTS pin is low)	0

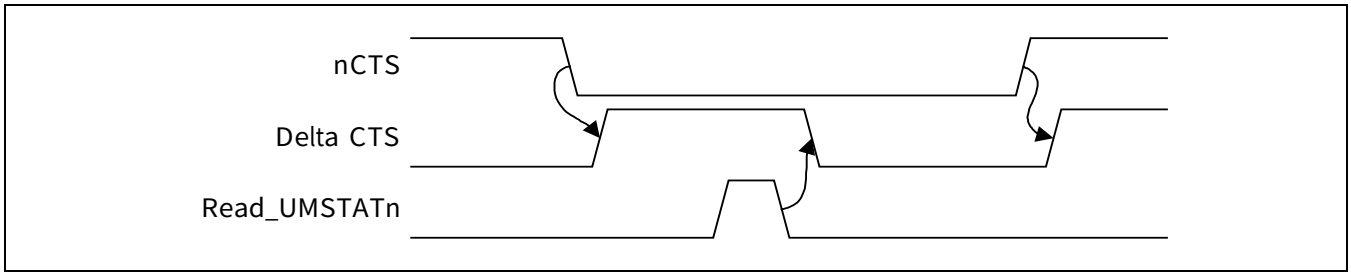


Figure 7-7. nCTS and Delta CTS Timing diagram

UART TRANSMIT HOLDING(BUFFER) REGISTER & FIFO REGISTER

UTXHn has an 8-bit data for transmissive data (Byte access only)

Register	Address	R/W	Description	Reset Value
UTXH0	0x1017 0020(L) 0x1017 0023(B)	W (by byte)	UART channel 0 transmit holding register	-
UTXH1	0x1018 0020(L) 0x1018 0023(B)	W (by byte)	UART channel 1 transmit holding register	-

UTXHn	Bit	Description	Initial State
TXDATAn	[7:0]	Transmit data for UARTn	-

NOTE :

(L) : When the endian mode is Little endian
(B) : When the endian mode is Big endian.

UART RECEIVE HOLDING (BUFFER) REGISTER & FIFO REGISTER

URXHn has an 8-bit data for received data (Byte access only).

Register	Address	R/W	Description	Reset Value
URXH0	0x1017 0024(L) 0x1017 0027(B)	R (by byte)	UART channel 0 receive buffer register	-
URXH1	0x1018 0024(L) 0x1018 0027(B)	R (by byte)	UART channel 1 receive buffer register	-

URXHn	Bit	Description	Initial State
RXDATAn	[7:0]	Receive data for UARTn	-

NOTE:

When an overrun error is occurred, the URXHn has to be read out. If not, the next received data will also make an overrun error, although the overrun bit of USTATn is cleared.
(L) : When the endian mode is Little endian
(B) : When the endian mode is Big endian.

UART BAUD RATE DIVISION REGISTER

The value stored in the baud rate divisor register, UBRDIV, is used to determine the serial Tx/Rx clock rate (baud rate) as follows:

UBRDIVn = (round_off)(APBCLK / (bps x 16)) -1

where the divisor should be from 1 to (2^{16}-1).
For example1, if the baud-rate is 230.4Kbps and APBCLK is 25MHz , UBRDIVn is:

UBRDIVn = (int)(25000000 / (230400 x 16)+0.5) -1
= (int)(6.8+0.5) -1
= 7 -1 = 6 (=0x6)

For example2, if the baud-rate is 115.2Kbps and APBCLK is 25MHz , UBRDIVn is:

UBRDIVn = (int)(25000000 / (115200 x 16)+0.5) -1
= (int)(13.6+0.5) -1
= 14 -1 = 13 (=0xD)

Register	Address	R/W	Description	Reset Value
UBRDIV0	0x1017 0028	R/W	Baud rate divisior register 0	0x0000 000D
UBRDIV1	0x1018 0028	R/W	Baud rate divisior register 1	0x0000 000D

UBRDIV n	Bit	Description	Initial State
UBRDIV	[15:0]	Baud rate division value UBRDIVn >0	0x000D

UART Register

Register	Address	R/W	Description	Reset Value
ULCON0	0x1017 0000	R/W	UART channel 0 line control register	0x0000 0000
UCON0	0x1017 0004	R/W	UART channel 0 control register	0x0000 0000
UFCON0	0x1017 0008	R/W	UART channel 0 FIFO control register	0x0000 0000
UMCON0	0x1017 000C	R/W	UART channel 0 Modem control register	0x0000 0000
UTRSTAT0	0x1017 0010	R	UART channel 0 Tx/Rx status register	0x0000 0006
UERSTAT0	0x1017 0014	R	UART channel 0 Rx error status register	0x0000 0000
UFSTAT0	0x1017 0018	R	UART channel 0 FIFO status register	0x0000 0000
UMSTAT0	0x1017 001C	R	UART channel 0 Modem status register	0x0000 0000
UTXH0	0x1017 0020(L) 0x1017 0023(B)	W (by byte)	UART channel 0 transmit holding register	-
URXH0	0x1017 0024(L) 0x1017 0027(B)	R (by byte)	UART channel 0 receive buffer register	-
UBRDIV0	0x1017 0028	R/W	Baud rate divisior register 0	0x0000 000D
ULCON1	0x1018 0000	R/W	UART channel 1 line control register	0x0000 0000
UCON1	0x1018 0004	R/W	UART channel 1 control register	0x0000 0000
UFCON1	0x1018 0008	R/W	UART channel 1 FIFO control register	0x0000 0000
UMCON1	0x1018 000C	R/W	UART channel 1 Modem control register	0x0000 0000
UTRSTAT1	0x1018 0010	R	UART channel 1 Tx/Rx status register	0x0000 0006
UERSTAT1	0x1018 0014	R	UART channel 1 Rx error status register	0x0000 0000
UFSTAT1	0x1018 0018	R	UART channel 1 FIFO status register	0x0000 0000
UMSTAT1	0x1018 001C	R	UART channel 1 Modem status register	0x0000 0000
UTXH1	0x1018 0020(L) 0x1018 0023(B)	W (by byte)	UART channel 1 transmit holding register	-
URXH1	0x1018 0024(L) 0x1018 0027(B)	R (by byte)	UART channel 1 receive buffer register	-
UBRDIV1	0x1018 0028	R/W	Baud rate divisior register 1	0x0000 000D

8 INTERRUPT CONTROLLER(Preliminary)

OVERVIEW

Interrupt controller in S3C2800X receives 29 interrupt requests from interrupt sources such as DMA, UART, etc.

The role of the interrupt controller is to generate FIQ or IRQ interrupt request to the ARM920T core after the arbitration(FIQ or IRQ, Interrupt mask) process when there are multiple interrupt requests from internal peripherals and/or external interrupt request pins.

The arbitration process is performed by Interrupt mode(IRQ or FIQ) & interrupt mask logic and the result is written to the interrupt pending register(FIQ/IRQ) that can be read by the users in the interrupt service routine..

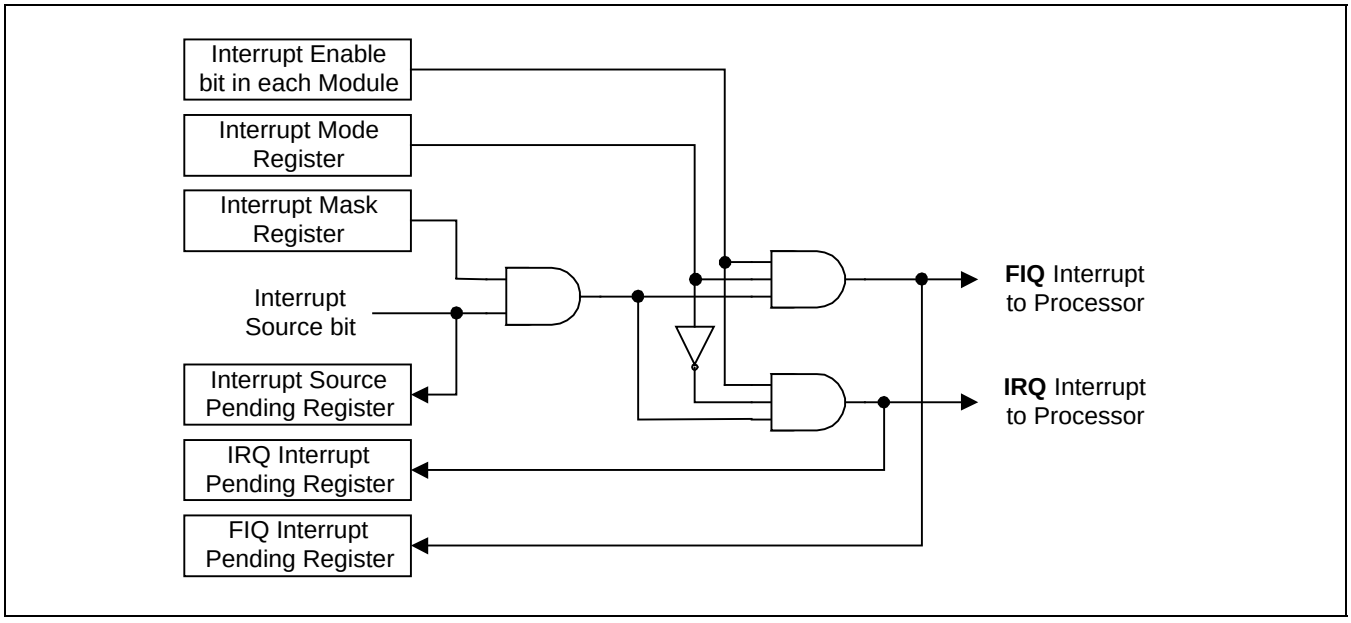


Figure 8-1. Interrupt Controller Block Diagram

INTERRUPT CONTROLLER OPERATION

F-bit and I-bit of PSR (program status register)

If the F-bit of PSR (program status register in ARM920T CPU) is set to 1, the FIQ (fast interrupt request) of the interrupt controller is not accepted by CPU. If I-bit of PSR (program status register in ARM920T CPU) is set to 1, the IRQ (interrupt request) of the interrupt controller is not accepted by CPU. So, to enable the interrupt reception, the F-bit or I-bit of PSR has to be cleared to 0 and also the corresponding bit of INTMSK has to be cleared to 0.

Interrupt Mode

ARM920T has 2 types of interrupt mode, FIQ or IRQ. All the interrupt sources determine what mode of interrupt will be used at requesting the interrupt.

CONTROL REGISTERS

There are five control registers in the interrupt controller: source pending register**(SRCPND)**, interrupt mode register**(INTMOD)**, mask register**(INTMSK)**, and interrupt pending registers(**IRQPND**,**FIQPND**).

All the interrupt requests from the interrupt sources are first registered in the source pending register. They are divided into two groups based on the interrupt mode register, i.e., one FIQ request and the remaining IRQ requests. Masked interrpt source is don't set in the interrpt pending registers. The details of each control registers are as follows.

SOURCE PENDING REGISTER (SRCPND)

SRCPND register is composed of 29 bits each of which is related to an interrupt source. Each bit is set to 1 if the corresponding interrupt source generates the interrupt request and waits for the interrupt to be serviced. Note that each bit of SRCPND register is automatically set by the interrupt sources regardless of the masking bits in the INTMSK register.

In the interrupt service routine for a specific interrupt source, the corresponding bit of SRCPND register has to be cleared to get the interrupt request from the same source correctly. If you return from the ISR without clearing the bit, interrupt controller operates as if another interrupt request comes in from the same source. In other words, if a specific bit of SRCPND register is set to 1, it is always considered as a valid interrupt request waiting to be serviced.

You can clear the specific bit of SRCPND register as follows: In the interrupt service routine for IRQ or FIQ, write 1 to SRCPND register. And then automatically It clears the interrupt pending registers(IRQPND,FIQPND).

INTERRUPT MODE REGISTER (INTMOD)

This register is composed of 29 bits each of which is related to an interrupt source. If a specific bit is set to 1, the corresponding interrupt is processed in the FIQ (fast interrupt) mode. Otherwise, it is processed in the IRQ mode (normal interrupt).

Note that at most only one interrupt source can be serviced in the FIQ mode in the interrupt controller. (You should use the FIQ mode only for the urgent interrupt.) Thus, only one bit of INTMOD can be set to 1 at most.

INTERRUPT MASK REGISTER (INTMSK)

Each of the 29 bits in the interrupt mask register is related to an interrupt source. If you clear a specific bit to 0, the interrupt request from the corresponding interrupt source is not serviced by the CPU. (Note that even in such a case, the corresponding bit of SRCPND register is set to 1). If the mask bit is 1, the interrupt request can be serviced.

INTERRUPT PENDING REGISTER (IRQPND,FIQPND)

The IRQPND and the FIQPND contain one flag per interrupt (29 total) that indicates an interrupt request has been made by a unit. Inside the interrupt service routine, the IRQPND and FIQPND are read to determine the interrupt source.

Bits within the IRQPND and FIQPND are read only. Once an interrupt has been serviced, the handler clears the pending bit at the interrpt service routine by writing a one to the necessary bit in the source pendign register(SRCPND). Clearing the interrupt source pending bit at the interrupt service routine, automatically clears the corresponding bit in the IRQPND and FIQPND register.

This is a read-only register.

INTERRUPT SOURCES

Interrupt controller supports 29 interrupt sources as follows table 11-1. User can get to know the interrupt source in the interrupt service routine by reading the IRQPND & FIQPND register.

Table 8-1. Interrupt Source & Corresponding Bit

Corresponding bit	Sources	Descriptions
[28]	INT_RTC	RTC alarm interrupt
[27]	INT_TICK	RTC Time tick interrupt
[26]	INT_FULL	Remocon data FIFO full interrupt
[25]	INT_RMT	Remote control signal input interrupt
[24]	INT_UERR1	UART 1 error Interrupt
[23]	INT_UERR0	UART 0 error Interrupt
[22]	INT_TxD1	UART1 transmit interrupt
[21]	INT_TxD0	UART0 transmit interrupt
[20]	INT_ RxD1	UART 1 receive interrupt
[19]	INT_RxD0	UART 0 receive interrupt
[18]	INT_IIC1	IIC 1 interrupt
[17]	INT_ IIC0	IIC 0 interrupt
[16]	INT_TIMER2	Timer 2 interrupt
[15]	INT_TIMER1	Timer 1 interrupt
[14]	INT_TIMER0	Timer 0 interrupt
[13]	INT_DMA3	General DMA 3 interrupt
[12]	INT_DMA2	General DMA 2 interrupt
[11]	INT_DMA1	General DMA 1 interrupt
[10]	INT_DMA0	General DMA 0 interrupt
[9]	*INT_SERR*	*External PCI SERR interrupt*
[8]	*INT_PCI*	*PCI interrupt*
[7]	EXTINT7	External interrupt 7
[6]	EXTINT6	External interrupt 6
[5]	EXTINT5	External interrupt 5
[4]	EXTINT4	External interrupt 4
[3]	EXTINT3	External interrupt 3
[2]	EXTINT2	External interrupt 2
[1]	EXTINT1	External interrupt 1
[0]	EXTINT0	External interrupt 0

INTERRUPT CONTROLLER SEPCIAL REGISTERS

INTERRUPT SOURCE PENDING REGISTER (SRCPND)

Each of the 29 bits in the interrupt source pending register, SRCPND, corresponds to an interrupt source (**Refer to Table 11-1**). When an interrupt request is generated, it will be set by 1. The interrupt service routine must then clear the pending condition by writing '1' to the corresponding bit. Although several interrupt sources generate requests simultaneously, the SRCPND will indicate all interrupt sources that generate the interrupt requests. Although the interrupt source is masked by INTMSK, the corresponding pending bit is able to be set to 1.

Register	Address	R/W	Description	Reset Value
SRCPND	0x1002 0000	R/W	Indicates the interrupt request status.	0x0000 0000

SRCPND	Bit	Description	Initial State
EIN_xx (Refer to Table 11-1)	[28:0]	Indicates the interrupt request status 0 = Not requested, 1 = Requested	0x0000 0000

INTERRUPT MODE REGISTER (INTMOD)

Each of the 29 bits in the interrupt mode register, INTMOD, corresponds to an interrupt source (**Refer to Table 11-1**). When the interrupt mode bit for each source is set to 1, the interrupt is processed by the ARM920T core in the FIQ (fast interrupt) mode. Otherwise, it is processed in the IRQ mode (normal interrupt).

Register	Address	R/W	Description	Reset Value
INTMOD	0x1002 0004	R/W	Interrupt mode Register	0x0000 0000

INTMOD	Bit	Description	initial state
INT_xx (Refer to Table 11-1)	[28:0]	Interrupt mode Register 0 = IRQ mode 1 = FIQ mode	0x0000 0000

INTERRUPT MASK REGISTER (INTMSK)

Each of the 29 bits in the interrupt mask register, INTMSK, corresponds to an interrupt source (**Refer to Table 11-1**). When a source interrupt mask bit is 0 and the corresponding interrupt event occurs, the interrupt is not serviced by the CPU. If the mask bit is 1, the interrupt is serviced upon a request.

Register	Address	R/W	Description	Reset Value
INTMSK	0x1002 0008	R/W	Determines which interrupt source is masked. The masked interrupt source will not be serviced.	0x0000 0000

INTMSK	Bit	Description	initial state
INT_xx (Refer to Table 11-1)	[28:0]	Determines which interrupt source is masked. The masked interrupt source will not be serviced. 0 = Masked 1 = Service available	0x0000 0000

IRQ/FIQ INTERRUPT PENDING REGISTER (IRQPND/FIQPND)

The IRQPND and the FIQPND contain one flag per interrupt (29 total-refer to Table 11-1) that indicates an interrupt request has been made by a unit. Inside the interrupt service routine, the IRQPND and FIQPND are read to determine the interrupt source.

Register	Address	R/W	Description	Reset Value
IRQPND	0x1002 000C	R	IRQ interrupt service pending register	0x0000 0000
FIQPND	0x1002 0010	R	FIQ interrupt service pending register	0x0000 0000

IRQPND/FIQPND	Bit	Description	Initial State
INT_xx (Refer to Table 11-1)	[28:0]	IRQ/FIQ interrupt service pending register 0 = not requested 1 = requested now	0x0000 0000

IMPORTANT NOTE

To clear the IRQPND/FIQPND, the following two rules has to be obeyed.

1) The pending bit in source pending register(SRCPND) should have to clear by writing 1.

2) And then it is cleared the pending bit in interrupt pending register(IRQPND/FIQPND) auatomatically.

NOTES

Interrupt Control Register

Register	Address	R/W	Description	Reset Value
SRCPND	0x1002 0000	R/W	Indicates the interrupt request status.	0x0000 0000
INTMOD	0x1002 0004	R/W	Interrupt mode Register	0x0000 0000
INTMSK	0x1002 0008	R/W	Determines which interrupt source is masked.	0x0000 0000
IRQPND	0x1002 000C	R	IRQ interrupt service pending register	0x0000 0000
FIQPND	0x1002 0010	R	FIQ interrupt service pending register	0x0000 0000

9 REMOCON RECEIVER

OVERVIEW

The S3C2800X has the ability to capture pulse signals which are externally input using H/W. It is able to transmit up to 8 different 8-bit capture data using the remocon receiver control register, RRCR, and FIFOD. The remocon receiver block operates with the remocon input interrupt bit, RRCR[10] set to “1”. It can choose rising edge, falling edge or rising/falling edge, and is the input pulse width from 32,768Hz for filtering. The frequency division of the 8-bit counter clock input is chosen from 1, 2, 4, or 8 of 32768 Hz. The FIFOs empty status flag is set when all FIFOs are empty, and the FIFOs full status flag is set when all FIFOs are full. An interrupt is generated when data is transmitted to all 8 FIFOs.

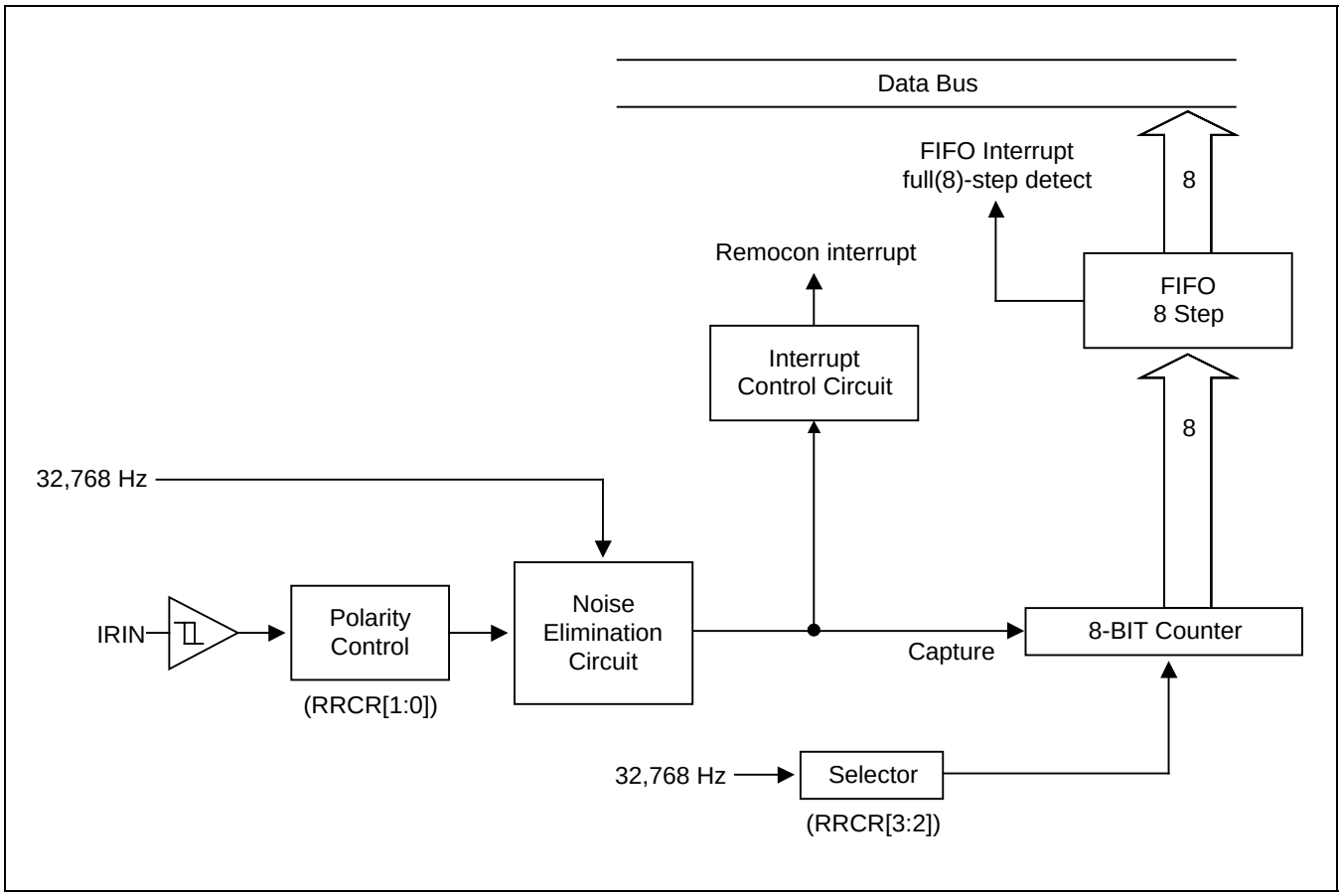


Figure 9-1. Remocon Receiver Circuit Block Diagram

REMOCON RECEIVER SPECIAL REGISTERS

REMOCON RECEIVER CONTROL REGISTER (RRCR)

Register	Address	R/W	Description	Reset Value
RRCR	0x1011 0000	R/W	Remocon receiver control register	0x0000 0010

RRCR	Bit	Description	Initial State
Reserved	[31:9]	Reserved	
Counter overflow status flag	[8]	Counter overflow status flag 0 = Not overflow 1 = Overflow	0
FIFO full (8)-step detect interrupt	[7]	Enable FIFO full(8)-step detect interrupt 0 = Disable the FIFO full (8)-step detect interrupt 1 = Enable the FIFO full (8)-step detect interrupt	0
Remocon Input Interrupt	[6]	Enable reomocon input interrupt 0 = Disable the remocon input interrupt 1 = Enable the remocon input interrupt	0
FIFO full Status flag	[5]	FIFO full(8) status flag (Read only) 0 = Not full 1 = Full	0
FIFO Empty Status flag	[4]	FIFO empty status flag (Read only) 0 = Not empty 1 = Empty	1
Counter clock selection	[3:2]	8-bit counter clock selection Maximum pulse width 00 = 32,768 Hz/1 01 = 32,768 Hz/2 10 = 32,768 Hz/4 11 = 32,768 Hz/8	00
Polarity control flag	[1:0]	Polarity control flag for remocon input interrupt 0x = Rising edge mode 10: Falling edge mode 11: Rising & Falling edge mode	00

NOTE: If all FIFOs are full, the next input data does not go into FIFO.

REMOCON FIFO DATA REGISTER (FIFOD)

Register	Address	R/W	Description	Reset Value
FIFOD	0x1011 0004	R	FIFO Data register	0xX

RRCR	Bit	Description	Initial State
Reserved	[31:8]	Reserved	
FIFO Data	[7:0]	FIFO Data (8-bit)	x

NOTES

Reomcon receiver control Register

Register	Address	R/W	Description	Reset Value
RRCR	0x1011 0000	R/W	Remocon receiver control register	0x0000 0040
FIFOD	0x1011 0004	R	FIFO Data register	-

10 RTC (REAL TIME CLOCK)-Preliminary

OVERVIEW

The RTC (Real Time Clock) unit can be operated by the backup battery although the system power is turned off. The RTC can transmit 8-bit data to CPU as BCD (Binary Coded Decimal) values using STRB/LDRB ARM operation. The data include second, minute, hour, date, day, month, and year. The RTC unit works with an external 32.768 KHz crystal and also can perform the alarm function.

FEATURE

— BCD number : second, minute, hour, date, day, month, year

— Leap year generator

— Alarm function : alarm interrupt

— Year 2000 problem is removed.

— Supports millisecond tick time interrupt for RTOS kernel time tick.

— Round reset function

REAL TIME CLOCK OPERATION

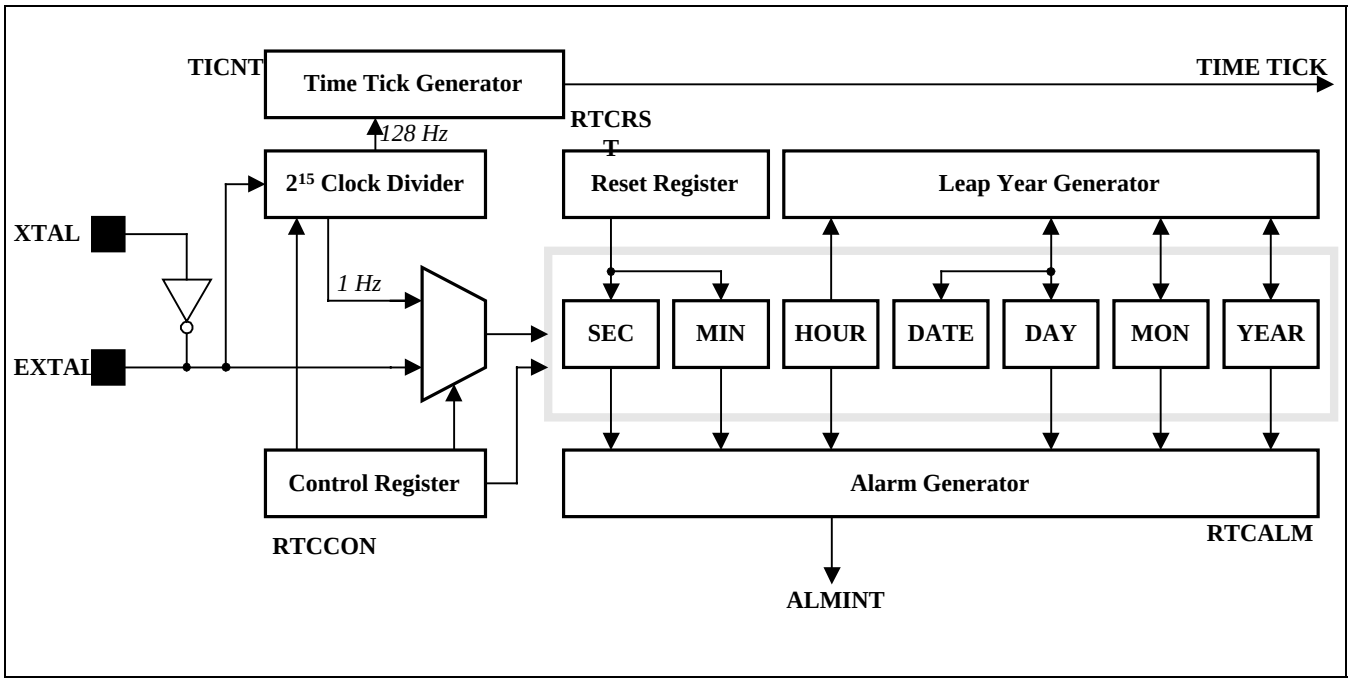


Figure 10-1. Real Time Clock Block Diagram

LEAP YEAR GENERATOR

This block can determine whether the last date of each month is 28, 29, 30, or 31, based on data from BCDDAY, BCDMON, and BCDYEAR. This block can also consider the leap year in deciding the last date. An 8-bit counter can only represent 2 BCD digits, so it cannot decide whether 00 year is a leap year or not. For example, it can not discriminate between 1900 and 2000. To solve this problem, the RTC block in S3C2800X has hard-wired logic to support the leap year in 2000. Please note 1900 is not leap year while 2000 is leap year. Therefore, two digits of 00 in S3C2800X denote 2000, not 1900.

READ/WRITE REGISTERS

It is required to set bit 0 of the RTCCON register to read and write the register in RTC block. To display the sec., min., hour, day, month, and year, the CPU should read the data in BCDSEC, BCDMIN, BCDHOUR, BCDDAY, BCDDATE, BCDMON, and BCDYEAR register in RTC block. But, there may be one second deviation because of multiple register read. For example, when user read registers from BCDYEAR to BCDMIN register, we assume that the result was 1959(Year), 12(Month), 31(Date), 23(Hour) and 59(Minute). When user read BCDSEC register, if the result is value from 1 to 59(Second), there is no problem. But, if the result is 0 sec., there will be possibility for year, month, data, hour, and minute to be changed into 1960(Year), 1(Month), 1(Date), 0(Hour) and 0(Minute) because of one second deviation as above-mentioned. In this case, user should read from BCDYEAR to BCDSEC again if BCDSEC is zero.

ALARM FUNCTION

The RTC generates an alarm signal at a specified time. The alarm interrupt (ALMINT) is activated. The RTC alarm register, RTCALM, can determine the alarm enable/disable and the condition of the alarm time setting.

TICK TIME INTERRUPT

The RTC tick time is used for interrupt request. The TICNT register has a interrupt enable bit and the count value for interrupt. The value of count is reached to '0' the tick time interrupt is occur and the period of interrupt is as follow:

Period = (n+1) / 128 second
n : Tick time count value (1~127)

This RTC time tick may be used for RTOS(real time operating system) kernel time tick. If time tick is generated by RTC time tick, the time related function of RTOS will always synchronized with real time.

ROUND RESET FUNCTION

The round reset function can be performed by the RTC round reset register, RTCRST. You can select the round boundary (30, 40, or 50 sec) of the second carry generation and the second value is rounded to zero value in the round reset operation. For example, when the current time is 23:37:47 and the round boundary is selected as 40 sec, the round reset operation changes the current time with 23:38:00.

32.768KHZ X-TAL CONNECTION EXAMPLE

The Figure 13-2 is example circuit for 32.768Khz oscillation for RTC unit.

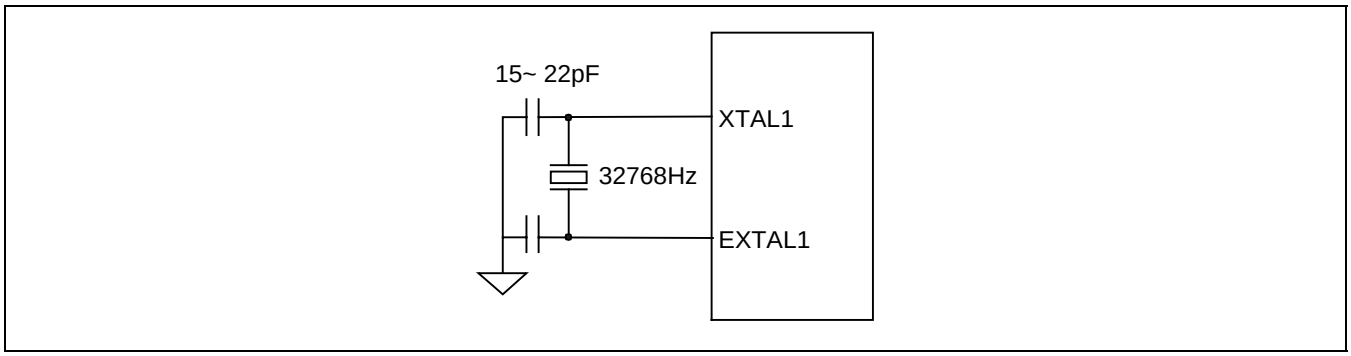


Figure 10-2. Main Oscillator Circuit Examples

REAL TIME CLOCK SPECIAL REGISTERS

REAL TIME CLOCK CONTROL REGISTER (RTCCON)

The RTCCON register consists of 4 bits such as RTCEN which controls the read/write enable of the BCD registers, CLKSEL, CNTSEL, and CLKRST for testing.

RTCEN bit can control all interfaces between the CPU and the RTC, so it should be set to 1 in an RTC control routine to enable data read/write after a system reset. Also before power off, the RTCEN bit should be cleared to 0 to prevent an inadvertent writing into RTC registers.

Register	Address	R/W	Description	Reset Value
RTCCON	0x1016 0000	R/W	RTC control Register	0x0000 0000

RTCCON	Bit	Description	Initial State
CLKRST	[3]	RTC clock count reset 0 = No reset, 1 = Reset	0
CNTSEL	[2]	BCD count select 0 = Merge BCD counters 1 = Reserved (Separate BCD counters)	0
CLKSEL	[1]	BCD clock select 0 = XTAL $1/2^{15}$ divided clock 1 = Reserved (XTAL clock)	0
RTCEN	[0]	RTC read/write enable 0 = Disable, 1 = Enable	0

RTC ALARM CONTROL REGISTER (RTCALM)

RTCALM register determines the alarm enable and the alarm time. Note that the RTCALM register generates the alarm signal through ALMINT.

Register	Address	R/W	Description	Reset Value
RTCALM	0x1016 0004	R/W	RTC alarm control Register	0x0000 0000

RTCALM	Bit	Description	Initial State
Reserved	[7]		0
ALMEN	[6]	Alarm global enable 0 = Disable, 1 = Enable	0
YEAREN	[5]	Year alarm enable 0 = Disable, 1 = Enable	0
MONREN	[4]	Month alarm enable 0 = Disable, 1 = Enable	0
DAYEN	[3]	Day alarm enable 0 = Disable, 1 = Enable	0
HOUREN	[2]	Hour alarm enable 0 = Disable, 1 = Enable	0
MINEN	[1]	Minute alarm enable 0 = Disable, 1 = Enable	0
SECEN	[0]	Second alarm enable 0 = Disable, 1 = Enable	0

ALARM SECOND DATA REGISTER (ALMSEC)

Register	Address	R/W	Description	Reset Value
ALMSEC	0x1016 0008	R/W	Alarm second data Register	0x0000 0000

ALMSEC	Bit	Description	Initial State
Reserved	[7]		0
SECDATA	[6:4]	BCD value for alarm second from 0 to 5	000
	[3:0]	from 0 to 9	0000

ALARM MIN DATA REGISTER (ALMMIN)

Register	Address	R/W	Description	Reset Value
ALMMIN	0x1016 000C	R/W	Alarm minute data Register	0x0000 0000

ALMMIN	Bit	Description	Initial State
Reserved	[7]		0
MINDATA	[6:4]	BCD value for alarm minute from 0 to 5	000
	[3:0]	from 0 to 9	0000

ALARM HOUR DATA REGISTER (ALMHOUR)

Register	Address	R/W	Description	Reset Value
ALMHOUR	0x1016 0010	R/W	Alarm hour data Register	0x0000 0000

ALMHOUR	Bit	Description	Initial State
Reserved	[7:6]		0
HOURDATA	[5:4]	BCD value for alarm hour from 0 to 2	00
	[3:0]	from 0 to 9	0000

ALARM DAY DATA REGISTER (ALMDAY)

Register	Address	R/W	Description	Reset Value
ALMDAY	0x1016 0014	R/W	Alarm day data Register	0x0000 0001

ALMDAY	Bit	Description	Initial State
Reserved	[7:6]		0
DAYDATA	[5:4]	BCD value for alarm day, from 0 to 28, 29, 30, 31 from 0 to 3	00
	[3:0]	from 0 to 9	0001

ALARM MON DATA REGISTER (ALMMON)

Register	Address	R/W	Description	Reset Value
ALMMON	0x1016 0018	R/W	Alarm month data Register	0x0000 0001

ALMMON	Bit	Description	Initial State
Reserved	[7:5]		0
MONDATA	[4]	BCD value for alarm month from 0 to 1	0
	[3:0]	from 0 to 9	0001

ALARM YEAR DATA REGISTER (ALMYEAR)

Register	Address	R/W	Description	Reset Value
ALMYEAR	0x1016 001C	R/W	Alarm hour data Register	0x0000 0000

ALMYEAR	Bit	Description	Initial State
YEARDATA	[7:0]	BCD value for year from 00 to 99	0x00

BCD SECOND REGISTER (BCDSEC)

Register	Address	R/W	Description	Reset Value
BCDSEC	0x1016 0020	R/W	BCD second Register	Undef.

BCDSEC	Bit	Description	Initial State
Reserved	[7]		-
SECDATA	[6:4]	BCD value for second from 0 to 5	-
	[3:0]	from 0 to 9	-

BCD MINUTE REGISTER (BCDMIN)

Register	Address	R/W	Description	Reset Value
BCDMIN	0x1016 0024	R/W	BCD minute Register	Undef.

BCDMIN	Bit	Description	Initial State
Reserved	[7]		-
MINDATA	[6:4]	BCD value for minute from 0 to 5	-
	[3:0]	from 0 to 9	-

BCD HOUR REGISTER (BCDHOUR)

Register	Address	R/W	Description	Reset Value
BCDHOUR	0x1016 0028	R/W	BCD hour Register	Undef.

BCDHOUR	Bit	Description	Initial State
Reserved	[7:6]		-
HOURDATA	[5:4]	BCD value for hour from 0 to 2	-
	[3:0]	from 0 to 9	-

BCD DAY REGISTER (BCDDAY)

Register	Address	R/W	Description	Reset Value
BCDDAY	0x1016 002C	R/W	BCD day Register	Undef

BCDDAY	Bit	Description	Initial State
Reserved	[7:6]		-
DAYDATA	[5:4]	BCD value for day from 0 to 3	-
	[3:0]	from 0 to 9	-

BCD DATE REGISTER (BCDDATE)

Register	Address	R/W	Description	Reset Value
BCDDATE	0x1016 0030	R/W	BCD date Register	Undef.

BCDDATE	Bit	Description	Initial State
Reserved	[7:3]		-
DATEDATA	[2:0]	BCD value for date from 1 to 7	-

BCD MONTH REGISTER (BCDMON)

Register	Address	R/W	Description	Reset Value
BCDMON	0x1016 0034	R/W	BCD month Register	Undef.

BCDMON	Bit	Description	Initial State
Reserved	[7:5]		-
MONDATA	[4]	BCD value for month from 0 to 1	-
	[3:0]	from 0 to 9	-

BCD YEAR REGISTER (BCDYEAR)

Register	Address	R/W	Description	Reset Value
BCDYEAR	0x1016 0038	R/W	BCD year Register	Undef.

BCDYEAR	Bit	Description	Initial State
YEARDATA	[7:0]	BCD value for year from 00 to 99	-

TICK TIME COUNT REGISTER (TICNT)

Register	Address	R/W	Description	Reset Value
TICNT	0x1016 0040	R/W	Tick time count Register	0x0000 0000

TICNT	Bit	Description	Initial State
TICK INT ENABLE	[7]	Tick time interrupt enable 0 = disable 1 = enable	0
TICK TIME COUNT	[6:0]	Tick time count value. (1~127) This counter value decrease internally, users can not read this real counter value on processing.	000000

RTC ROUND RESET REGISTER (RTCRST)

Register	Address	R/W	Description	Reset Value
RTCRST	0x1016 0044	R/W	RTC round reset Register	Undef.

RTCRST	Bit	Description	Initial State
SRSTEN	[2]	Round second reset enable 0 = Disable, 1 = Enable When this bit is set , it automatically will be cleared.	-
SECCR	[1:0]	Round boundary for second carry generation. (note) 00 = over than 30 sec 01 = over than 40 sec 1x = over than 50 sec	-

NOTE: Otherwise, no second carry is generated.

RTC Register

Register	Address	R/W	Description	Reset Value
RTCCON	0x1016 0000	R/W	RTC control Register	0x0000 0000
RTCALM	0x1016 0004	R/W	RTC alarm control Register	0x0000 0000
ALMSEC	0x1016 0008	R/W	Alarm second data Register	0x0000 0000
ALMMIN	0x1016 000C	R/W	Alarm minute data Register	0x0000 0000
ALMHOUR	0x1016 0010	R/W	Alarm hour data Register	0x0000 0000
ALMDAY	0x1016 0014	R/W	Alarm day data Register	0x0000 0001
ALMMON	0x1016 0018	R/W	Alarm month data Register	0x0000 0001
ALMYEAR	0x1016 001C	R/W	Alarm hour data Register	0x0000 0000
BCDSEC	0x1016 0020	R/W	BCD second Register	-
BCDMIN	0x1016 0024	R/W	BCD minute Register	-
BCDHOUR	0x1016 0028	R/W	BCD hour Register	-
BCDDAY	0x1016 002C	R/W	BCD day Register	-
BCDDATE	0x1016 0030	R/W	BCD date Register	-
BCDMON	0x1016 0034	R/W	BCD month Register	-
BCDYEAR	0x1016 0038	R/W	BCD year Register	-
TICNT	0x1016 0040	R/W	Tick time count Register	0x0000 0000
RTCRST	0x1016 0044	R/W	RTC round reset Register	-

11 WATCH-DOG TIMER(Preliminary)

OVERVIEW

The S3C2800X watchdog timer is used to resume the controller operation when it is disturbed by malfunctions such as noise and system errors. The watchdog timer generates the reset signal with the duration of 128 processor clock (APBCLK) cycles.

FEATURES

— Internal reset signal is activated during 128(3.41uS @37.5MHz) APBCLK cycles when the time-out occurs.

CONSIDERATION OF DEBUGGING ENVIRONMENT

When S3C2800X is in debug mode using Embedded ICE. the watch-dog timer must not operate for debugging. The watch-dog timer can determine whether or not the current mode is the debug mode by the CPU core signal (DBGACK signal). Once the DBGACK signal is asserted, the reset output of the watch-dog timer isn't activated when the watchdog timer is expired.

WATCH-DOG TIMER OPERATION

The functional block diagram of the watchdog timer is shown in Figure 14-1. The watchdog timer uses APBCLK as its only source clock. To generate the corresponding watchdog timer clock, the APBCLK frequency is prescaled first, and the resulting frequency is input to 16-bit counter.

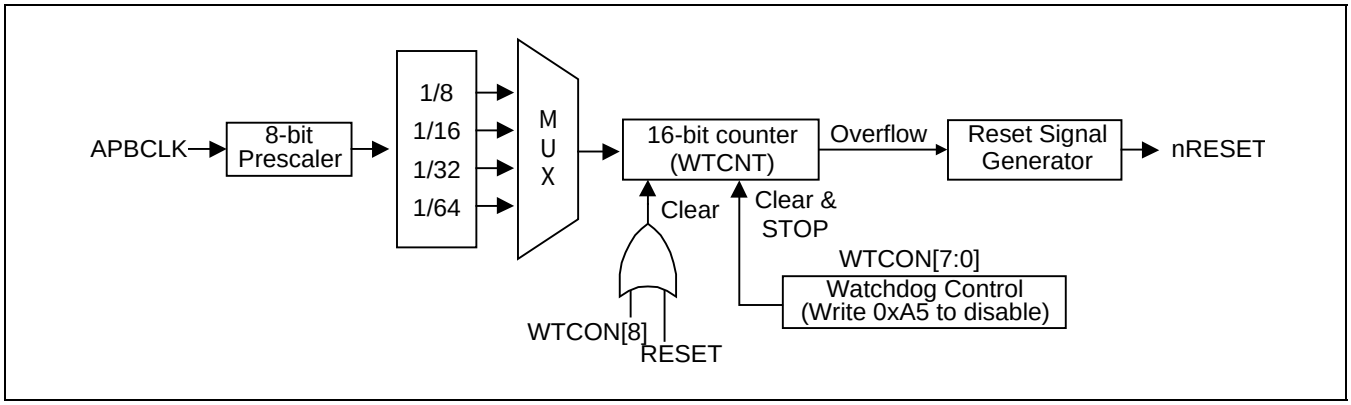


Figure 11-1. Watch-Dog Timer Block Diagram

The prescaler value and the frequency division factor are specified in the watchdog timer control register, WTCON. The valid prescaler values range from 1 to 2^8-1. Use the following formulas to calculate the watchdog timer interval time :

$$t\_watchdog = (1/(\ APBCLK\ /\ (Prescaler\ value + 1)/Divider\ value)) * 2^{16}\ (16\text{-}bit\ counter)$$

Table 11-1. Watch-dog Timer Interval Time Example

Divider settings	Minimum resolution (prescaler = 1)	Maximum resolution (prescaler = 255)	maximum interval (WTCNT = 65535)
1/8 (APBCLK = 50 MHz)	0.32 us (3.125 MHz)	40.96 us (24.42 KHz)	2.684 sec
1/16 (APBCLK = 50 MHz)	0.64 us (1.563 MHz)	81.92 us (12.21 KHz)	5.368 sec
1/32 (APBCLK = 50 MHz)	1.28 us (0.782 MHz)	163.84 us (6.11 KHz)	10.736 sec
1/64 (APBCLK = 50 MHz)	2.56 us (0.391 MHz)	327.68 us (3.06 KHz)	21.472 sec
1/8 (APBCLK = 37.5 MHz)	0.42 us (2.344 MHz)	54.61 us (18.31 KHz)	3.579 sec
1/16 (APBCLK = 37.5 MHz)	0.84 us (1.172 MHz)	109.22 us (9.16 KHz)	7.158 sec
1/32 (APBCLK = 37.5 MHz)	1.71 us (0.586 MHz)	218.44 us (4.58 KHz)	14.316 sec
1/64 (APBCLK = 37.5 MHz)	3.41 us (0.293 MHz)	436.9 us (2.28 KHz)	28.63 sec

WATCH-DOG TIMER SPECIAL REGISTERS

WATCH-DOG TIMER PRESCALER VALUE REGISTER (WTSCLR)

The valid prescaler values range from 1 to 2^8-1

Register	Address	R/W	Description	Reset Value
WTPSCLR	0x1012 0000	R/W	Watch-dog timer prescaler value Register	0x0000 0080

WTPSCLR	Bit	Description	Initial State
Pre-Scaler	[7:0]	8-bit pre-scaler value (1 ~ 255) 0 = Not supported	0x80

WATCH-DOG TIMER CONTROL REGISTER (WTCON)

Using the Watch-Dog Timer Control register, WTCON, you can enable/disable the watch-dog timer, and clear to watch-dog timer counter.
Because Watch-dog timer is used to resume the S3C2800X restart on mal-function after power-on, if users don't like to resume the controller restart, users should disable the Watch-dog timer or clear to 16-bit watch-dog timer counter(WTCNT – read only).

Register	Address	R/W	Description	Reset Value
WTCON	0x1012 0004	R/W	Watch-dog timer control Register	0x0000 0000

WTCON	Bit	Description	Initial State
Mux	[11:10]	Select Mux input 00 = 1/8 01 = 1/16 10 = 1/32 11 = 1/32	00
Reserved	[9]	Reserved	0
Watch-dog timer counter clear	[8]	Clear to watch-dog timer count value 0 = No effect 1 = Clear to count value When this bit is set , it automatically will be cleared after the counter is lodaded with all zero value.	0
Watch-dog timer Enable	[7:0]	This bits determine enable or disable of Watch-dog timer output for reset signal. 1010 0101b = Disable the reset function of the watch-dog timer. The 16-bit counter is clear to 0x0, and then it is stop. Other Value = Assert reset signal of the S3C2800X at watch-dog time out. The 16-bit counter start counting from 0x0 again after re-load the prescaler value.	0x00

WATCH-DOG TIMER COUNTER REGISTER (WTCNT)

The watchdog timer counter register, WTCNT, contains the current count values for the watchdog timer during normal operation.

Register	Address	R/W	Description	Reset Value
WTCNT	0x1012 0008	R	Watch-dog timer counter Register	0x0000 0000

WTCNT	Bit	Description	Initial State
Count value	[15:0]	The current count value of the watch-dog timer counter	0x0000

NOTES

Watch-dog Timer Register

Register	Address	R/W	Description	Reset Value
WTPSCLR	0x1012 0000	R/W	Watch-dog timer prescaler value Register	0x0000 0080
WTCON	0x1012 0004	R/W	Watch-dog timer control Register	0x0000 0000
WTCNT	0x1012 0008	R	Watch-dog timer count Register	0x0000 0000

12 IIC-BUS INTERFACE(Preliminary)

OVERVIEW

The S3C2800X RISC microprocessor can support 2channel multi-master IIC-bus serial interface. A dedicated serial data line(SDAn) and a serial clock line (SCLn) carry information between bus masters and peripheral devices which are connected to the IIC-bus. The SDAn and SCLn lines are bi-directional.

In multi-master IIC-bus mode, multiple S3C2800X RISC microprocessor can receive or transmit serial data to or from slave devices. The master S3C2800X which can initiate a data transfer over the IIC-bus, is responsible for terminating the transfer. Standard bus arbitration procedure is used in this IIC-bus in S3C2800X.

To control multi-master IIC-bus operations, you write values to the following registers:

— Multi-master IIC-bus control register, IICCON0,1

— Multi-master IIC-bus control/status register, IICSTAT0,1

— Multi-master IIC-bus Tx/Rx data shift register, IICDS0,1

— Multi-master IIC-bus address register, IICADD0,1

When the IIC-bus is free, the SDA and SCL lines should be both at High level. A High-to-Low transition of SDA can initiate a Start condition. A Low-to-High transition of SDA can initiate a Stop condition while SCL remains steady at High Level.

The Start and Stop conditions can always be generated by the master devices. A 7-bit address value in the first data byte which is put onto the bus after the Start condition is initiated, can determine the slave device which the bus master device has selected. The 8^{th} bit determines the direction of the transfer (read or write).

Every data byte that is put onto the SDA line should be total eight bits. The number of bytes which can be sent or received during the bus transfer operation is unlimited. Data is always sent from most-significant bit (MSB) first and every byte should be immediately followed by an acknowledge (ACK) bit.

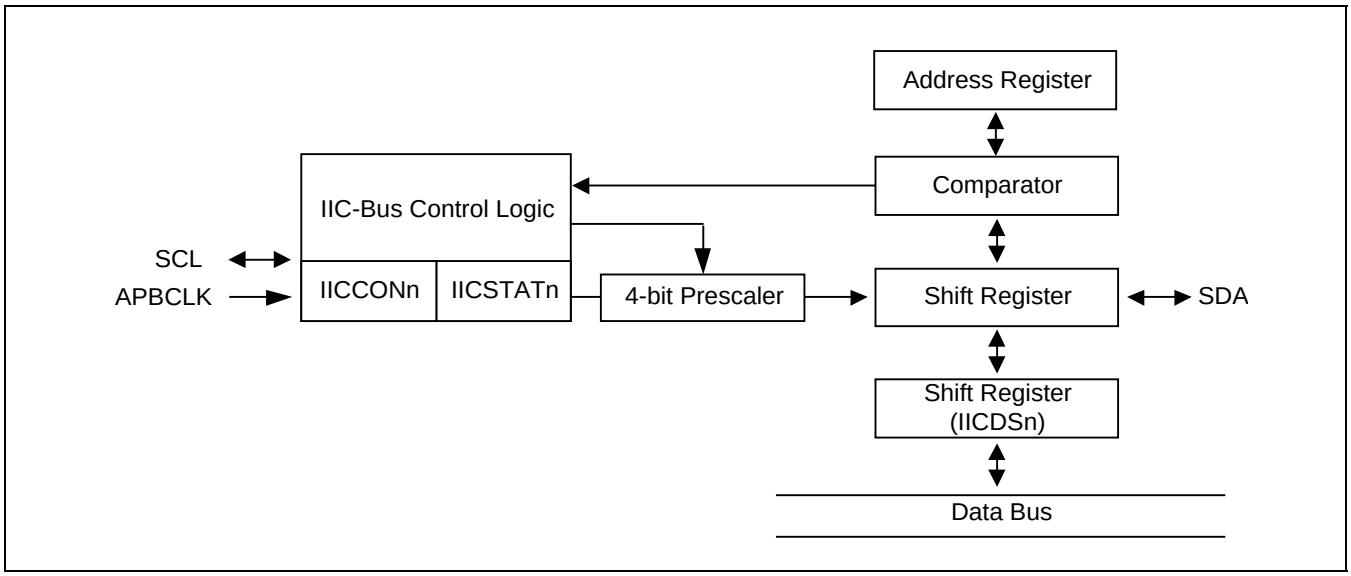


Figure 12-1. IIC-Bus Block Diagram

THE IIC-BUS INTERFACE

The S3C2800X IIC-bus interface has four operation modes:

— Master transmitter mode

— Master receive mode

— Slave transmitter mode

— Slave receive mode

Functional relationships among these operating modes are described below.

START AND STOP CONDITIONS

When the IIC-bus interface is in inactive state, it is usually in slave mode. In other word, the state of interface should be in slave mode before detecting a Start condition on the SDA line.(A Start condition can be initiated by having a High-to-Low transition of the SDA line while the clock signal of SCL is High) When the state of interface is changed into the master mode, it can initiate a data transfer on the SDA line as well as generating the SCL signal.

A Start condition can initiate a one-byte serial data transfer over the SDA line and stop condition can initiate the termination of data transfer. A stop condition is a Low-to-High transition of the SDA line while SCL is High. Start and Stop conditions are always generated by the master. The IIC-bus is busy when a Start condition is generated. A few clocks after a Stop condition, the IIC-bus will be free, again.

When a master initiates a Start condition, it should send slave address to give a notice to the slave device. The one byte of address field consist of a 7-bit address and a 1-bit transfer direction indicator (that is, write or read). If bit 8 is 0, it indicates a write operation(transmit operation). If bit 8 is 1, it indicates a request for data read(receive operation).

The master will finish the transfer operation by transmitting a Stop condition. If the master wants to continue the data transmission the bus, it should generate another Start condition as well as slave address. In this way, the read-write operation can be performed in various format.

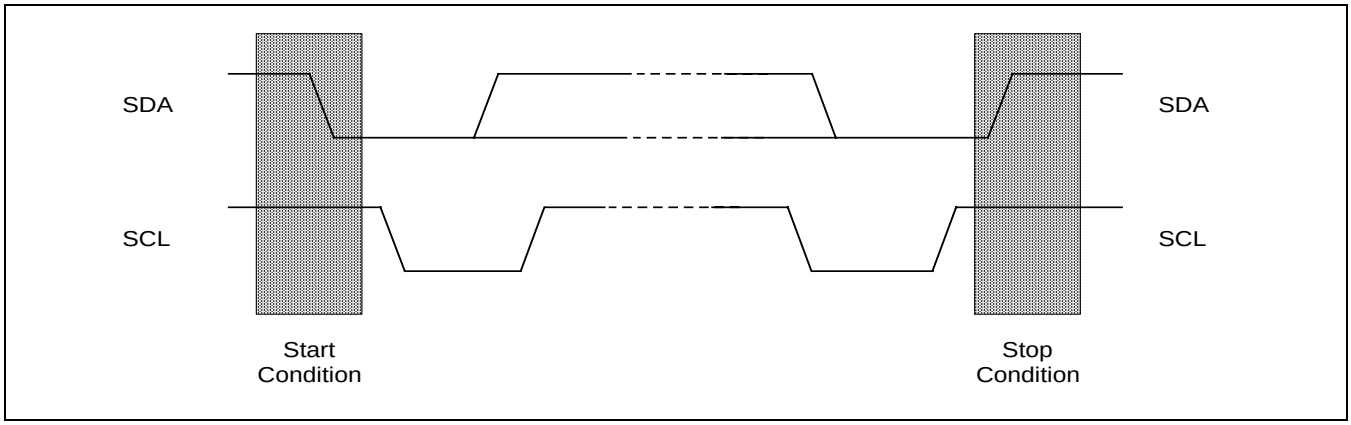


Figure 12-2. Start and Stop Condition

DATA TRANSFER FORMAT

Every byte put on the SDA line should have eight bits in length. The number of bytes which can be transmitted per transfer is unlimited. The first byte following a Start condition should have the address field. The address field can be transmitted by the master when the IIC-bus is operating in master mode. Each byte should be followed by an acknowledge (ACK) bit. The MSB bit of serial data and addresses are always sent first.

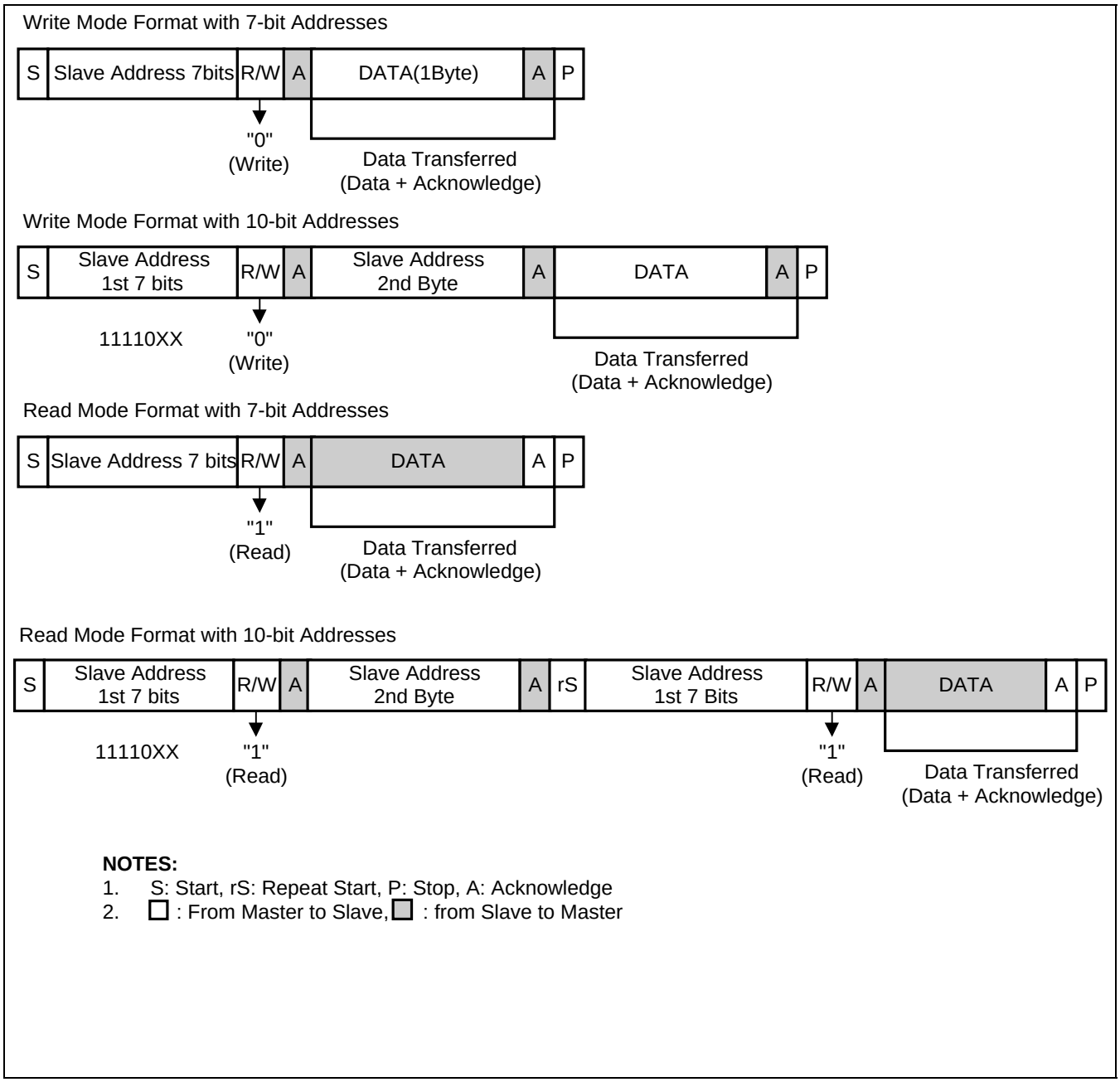


Figure 12-3. IIC-Bus Interface Data Format

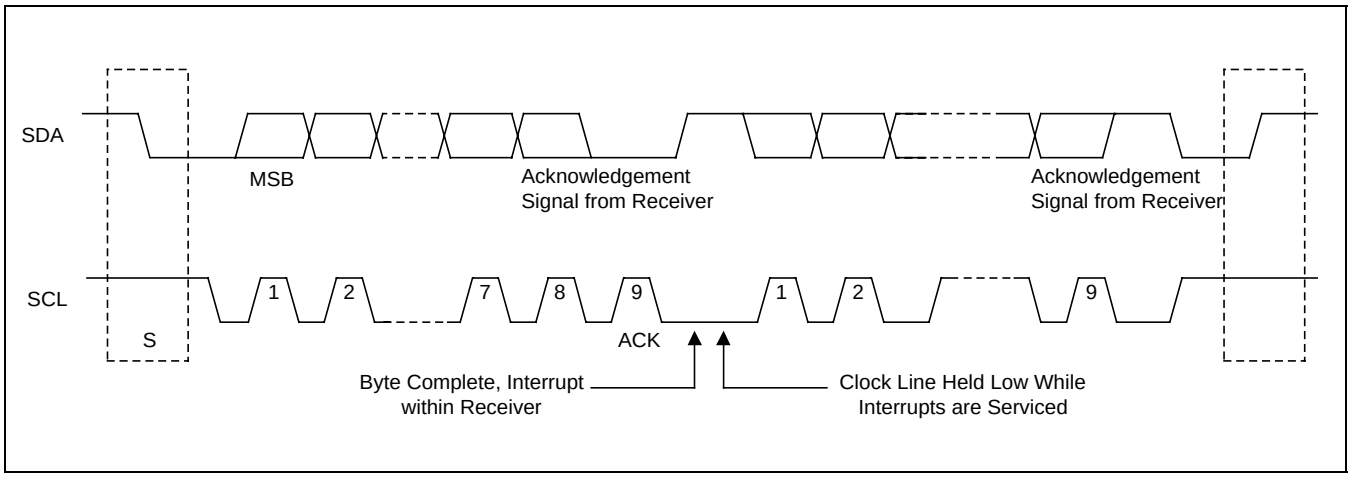


Figure 12-4. Data Transfer on the IIC-Bus

ACK SIGNAL TRANSMISSION

To finish a one-byte transfer operation completely, the receiver should send an ACK bit to the transmitter. The ACK pulse should occur at the ninth clock of the SCL line. Eight clocks are required for the one-byte data transfer. The clock pulse required for the transmission of the ACK bit, should be generated by the master.

The transmitter should release the SDA line by making the SDA line High when the ACK clock pulse is received. The receiver should also drive the SDA line Low during the ACK clock pulse so that the SDA is Low during the High period of the ninth SCL pulse.

The ACK bit transmit function can be enabled or disabled by software (IICSTATn). However, the ACK pulse on the ninth clock of SCL is required to complete a one-byte data transfer operation.

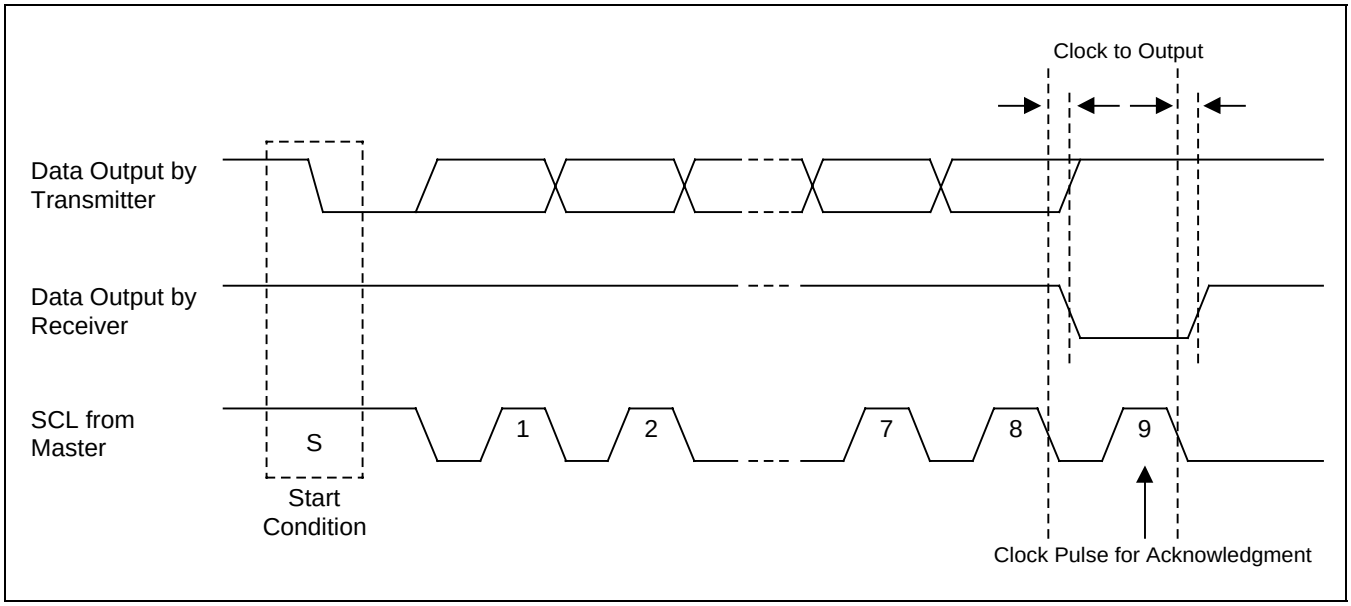


Figure 12-5. Acknowledge on the IIC-Bus

READ-WRITE OPERATION

In case of transmitter mode, after a data was transferred, the IIC-bus interface will wait until IICDSn(IIC-bus Data Shift Register) is written by a new data. Until the new data is written, the SCL line will be held low. After the new data is written to IICDSn register, the SCL line will be released. The S3C2800X should wait the interrupt to know the completion of transmission of current data. After getting the interrupt request, the CPU should write a new data into IICDSn, again.

In case of receive mode, after a data is received, the IIC-bus interface will wait until IICDSn register is read. Until the new data is read out, the SCL line will be held low. After the new data is read out from IICDSn register, the SCL line will be released. The S3C2800X should wait the interrupt to know the completion of reception of new data. After getting the interrupt request, the CPU should read data from IICDSn.

BUS ARBITRATION PROCEDURES

Arbitration takes place on the SDA line to prevent the contention on the bus between two masters. If a master with a SDA High level detects another master with a SDA active Low level, it will not initiate a data transfer because the current level on the bus dose not correspond to its own. The arbitration procedure will be extended until the SDA line will be High.

But, in case of simultaneous lowering of the SDA line from masters, each master should evaluate whether or not the mastership is allocated to itself. For the purpose of evaluation, each master should detect the address bits. While each master generate the slaver address, it should also detect the address bit on the SDA line because the lowering of SDA line is stronger than maintaining High on the line. For example, one master generate Low as first address bit, while the other master is maintaining High. In this case, both master will be detect Low on the bus because Low is stronger than High even if first master is trying to maintain High on the line. In this case, Low-generating master as first address bit will get the mastership and High-generating master as first address bit should withdraw the mastership. If both master generate Low as first address bit, there should be arbitration for second address bit, again. This arbitration will be continued up to the end of last address bit.

ABORT CONDITIONS

If a slave receiver can not acknowledge the confirmation of the slave address, it should hold the level of the SDA line High. In this case, the master should generate a Stop condition and to abort the transfer.

If a master receiver is involved in the aborted transfer, it should signal the end of the slave transmit operation. It does this by canceling the generation of an ACK after the last data byte received from the slave. The slave transmitter should then release the SDA to allow a master to generate a Stop condition.

CONFIGURING THE IIC-BUS

To control the frequency of the serial clock (SCL), you program the 4-bit prescaler value in the IICCONn register. The IIC-bus interface address is stored in the IIC-bus address register, IICADDn. (By default, the IIC-bus interface address is an unknown value.)

IIC-BUS INTERFACE SPECIAL REGISTERS

MULTI-MASTER IIC-BUS CONTROL REGISTER (IICCON0,1)

Register	Address	R/W	Description	Reset Value
IICCON0	0x1019 0000	R/W	IIC-Bus control register0	0x0000 0020
IICCON1	0x101A 0000	R/W	IIC-Bus control register1	0x0000 0020

IICCONn	Bit	Description	Initial State
Reserved	[31:7]	Reserved	
Acknowledge enable (1)	[6]	IIC-bus acknowledge enable bit 0=Disable ACK generation 1=Enable ACK generation In Tx mode, the IICSDA is free in the ack time In Rx mode, the IICSDA is L in the ack time.	0
Tx clock source selection	[5]	Source clock of IIC-bus transmit clock prescaler selection bit 0= IICCLK = APBCLK /16 1= IICCLK = APBCLK /256	1
Tx/Rx Interrupt enable	[4]	IIC-Bus Tx/Rx interrupt enable/disable bit 0=Disable interrupt, 1=Enable interrupt	0
Transmit clock value (2)	[3:0]	IIC-Bus transmit clock prescaler IIC-Bus transmit clock frequency is determined by this 4-bit prescaler value, according to the following formula: Tx clock = IICCLK/(IICCON[3:0]+1)	0x0

NOTES:

1. Interfacing EEPROM, the ack generation may be disabled before reading the last data in order to generate the STOP condition in Rx mode.
2. IICCLK is determined by IICCON[5].
   Tx clock can vary by SCL transition time.

Table 12-1. Example for setting of the IIC-SCL

IIC_SCL (KHz)	APBCLK = 37.5MHz		APBCLK = 25MHz	
	IICCON[5]	IICCON[3:0]	IICCON[5]	IICCON[3:0]
100 (Real =73.2)	1=APBCLK/256	0x1=IICCLK/2	-	-
100 (Real = 97.7)	-	-	1=APBCLK/256	0x0=IICCLK
400 (Real = 390.6)	0=APBCLK/16	0x5=IICCLK/6	0=APBCLK/16	0x3=IICCLK/4

MULTI-MASTER IIC-BUS CONTROL/STATUS REGISTER (IICSTAT0,1)

Register	Address	R/W	Description	Reset Value
IICSTAT0	0x1019 0004	R/W	IIC-Bus control/status register0	0x0000 0000
IICSTAT1	0x101A 0004	R/W	IIC-Bus control/status register1	0x0000 0000

IICSTATn	Bit	Description	Initial State
Reserved	[31:8]	Reserved	
Mode selection	[7:6]	IIC-bus master/slave Tx/Rx mode select bits: 00: Slave receive mode 01: Slave transmit mode 10: Master receive mode 11: Master transmit mode	0
Busy signal status / START STOP condition	[5]	IIC-Bus busy signal status bit: 0 = read) IIC-bus not busy(when read) write) IIC-bus STOP signal generation 1 = read) IIC-bus busy(when read) write) IIC-bus START signal generation. The data in IICDS will be transfered automatically just after the start signal.	0
Serial output enable	[4]	IIC-bus data output enable/disable bit: 0=Disable Rx/Tx, 1=Enable Rx/Tx	0
Arbitration status flag	[3]	IIC-bus arbitration procedure status flag bit: 0 = Bus arbitration status okay 1 = Bus arbitration failed during serial I/O	0
Address-as-slave status flag	[2]	IIC-bus address-as-slave status flag bit: 0 = cleared when START/STOP condition was detected 1 = Received slave address matches the address value in the IICADD.	0
Address zero status flag	[1]	IIC-bus address zero status flag bit: 0 = cleared when START/STOP condition was detected. 1 = Received slave address is 00000000b	0
Last-received bit status flag	[0]	IIC-bus last-received bit status flag bit 0 = Last-received bit is 0 (ACK was received) 1 = Last-receive bit is 1 (ACK was not received)	0

MULTI-MASTER IIC-BUS ADDRESS REGISTER (IICADD0,1)

Register	Address	R/W	Description	Reset Value
IICADD0	0x1019 0008	R/W	IIC-Bus address register 0	-
IICADD1	0x101A 0008	R/W	IIC-Bus address register 1	-

IICADDn	Bit	Description	Initial State
Slave address	[7:0]	7-bit slave address, latched from the IIC-bus: When serial output enable=0 in the IICSTAT, IICADD is write-enabled. You can read the IICADD value at any time, regardless of the current serial output enable bit (IICSTAT) setting. Slave address = [7:1] Not mapped = [0]	-

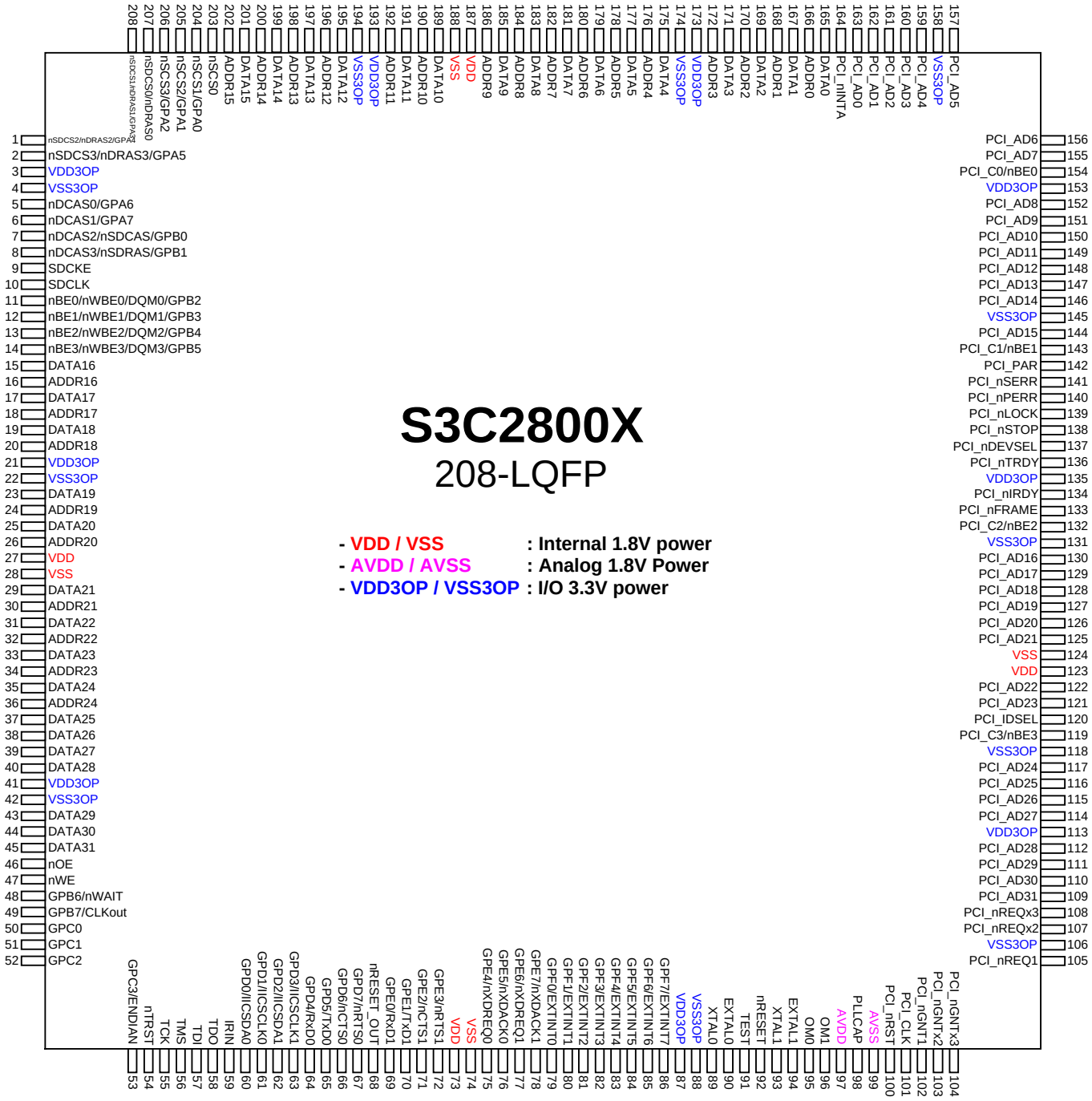
MULTI-MASTER IIC-BUS TRANSMIT/RECEIVE DATA SHIFT REGISTER (IICDS0,1)

Register	Address	R/W	Description	Reset Value
IICDS0	0x1019 000C	R/W	IIC-Bus transmit/receive data shift register 0	-
IICDS1	0x101A 000C	R/W	IIC-Bus transmit/receive data shift register 1	-

IICDSn	Bit	Description	Initial State
Data shift	[7:0]	8-bit data shift register for IIC-bus Tx/Rx operation: When serial output enable = 1 in the IICSTAT, IICDS is write-enabled. You can read the IICDS value at any time, regardless of the current serial output enable bit (IICSTAT) setting	-

IIC Control Register

Register	Address	R/W	Description	Reset Value
IICCON0	0x1019 0000	R/W	IIC-Bus 0 control register	0x0000 0020
IICSTAT0	0x1019 0004	R/W	IIC-Bus 0 control/status register	0x0000 0000
IICADD0	0x1019 0008	R/W	IIC-Bus 0 address register	-
IICDS0	0x1019 000C	R/W	IIC-Bus 0 transmit/receive data shift register	-
IICCON1	0x101A 0000	R/W	IIC-Bus 1 control register	0x0000 0000
IICSTAT1	0x101A 0004	R/W	IIC-Bus 1 control/status register	0x0000 0020
IICADD1	0x101A 0008	R/W	IIC-Bus 1 address register	-
IICDS1	0x101A 000C	R/W	IIC-Bus 1 transmit/receive data shift register	-


1 nSDCS2/nDRAS2/GPA4
2 nSDCS3/nDRAS3/GPA5
3 VDD3OP
4 VSS3OP
5 nDCAS0/GPA6
6 nDCAS1/GPA7
7 nDCAS2/nSDCAS/GPB0
8 nDCAS3/nSDRAS/GPB1
9 SDCKE
10 SDCLK
11 nBE0/nWBE0/DQM0/GPB2
12 nBE1/nWBE1/DQM1/GPB3
13 nBE2/nWBE2/DQM2/GPB4
14 nBE3/nWBE3/DQM3/GPB5
15 DATA16
16 ADDR16
17 DATA17
18 ADDR17
19 DATA18
20 ADDR18
21 VDD3OP
22 VSS3OP
23 DATA19
24 ADDR19
25 DATA20
26 ADDR20
27 VDD
28 VSS
29 DATA21
30 ADDR21
31 DATA22
32 ADDR22
33 DATA23
34 ADDR23
35 DATA24
36 ADDR24
37 DATA25
38 DATA26
39 DATA27
40 DATA28
41 VDD3OP
42 VSS3OP
43 DATA29
44 DATA30
45 DATA31
46 nOE
47 nWE
48 GPB6/nWAIT
49 GPB7/CLKout
50 GPC0
51 GPC1
52 GPC2
53 GPC3/ENDIAN
54 nTRST
55 TCK
56 TMS
57 TDI
58 TDO
59 IRIN
60 GPD0/IICSDA0
61 GPD1/IICSCLK0
62 GPD2/IICSDA1
63 GPD3/IICSCLK1
64 GPD4/RxD0
65 GPD5/TxD0
66 GPD6/nCTS0
67 GPD7/nRTS0
68 nRESET_OUT
69 GPE0/RxD1
70 GPE1/TxD1
71 GPE2/nCTS1
72 GPE3/nRTS1
73 VDD
74 VSS
75 GPE4/nXDREQ0
76 GPE5/nXDACK0
77 GPE6/nXDREQ1
78 GPE7/nXDACK1
79 GPF0/EXTINT0
80 GPF1/EXTINT1
81 GPF2/EXTINT2
82 GPF3/EXTINT3
83 GPF4/EXTINT4
84 GPF5/EXTINT5
85 GPF6/EXTINT6
86 GPF7/EXTINT7
87 VDD3OP
88 VSS3OP
89 XTAL0
90 EXTAL0
91 TEST
92 nRESET
93 XTAL1
94 EXTAL1
95 OM0
96 OM1
97 AVDD
98 PLLCAP
99 AVSS
100 PCI_nRST
101 PCI_CLK
102 PCI_nGNT1
103 PCI_nGNTx2
104 PCI_nGNTx3
105 PCI_nREQ1
106 VSS3OP
107 PCI_nREQx2
108 PCI_nREQx3
109 PCI_AD31
110 PCI_AD30
111 PCI_AD29
112 PCI_AD28
113 VDD3OP
114 PCI_AD27
115 PCI_AD26
116 PCI_AD25
117 PCI_AD24
118 VSS3OP
119 PCI_C3/nBE3
120 PCI_IDSEL
121 PCI_AD23
122 PCI_AD22
123 VDD
124 VSS
125 PCI_AD21
126 PCI_AD20
127 PCI_AD19
128 PCI_AD18
129 PCI_AD17
130 PCI_AD16
131 VSS3OP
132 PCI_C2/nBE2
133 PCI_nFRAME
134 PCI_nIRDY
135 VDD3OP
136 PCI_nTRDY
137 PCI_nDEVSEL
138 PCI_nSTOP
139 PCI_nLOCK
140 PCI_nPERR
141 PCI_nSERR
142 PCI_PAR
143 PCI_C1/nBE1
144 PCI_AD15
145 VSS3OP
146 PCI_AD14
147 PCI_AD13
148 PCI_AD12
149 PCI_AD11
150 PCI_AD10
151 PCI_AD9
152 PCI_AD8
153 VDD3OP
154 PCI_C0/nBE0
155 PCI_AD7
156 PCI_AD6
157 PCI_AD5
158 VSS3OP
159 PCI_AD4
160 PCI_AD3
161 PCI_AD2
162 PCI_AD1
163 PCI_AD0
164 PCI_nINTA
165 DATA0
166 ADDR0
167 DATA1
168 ADDR1
169 DATA2
170 ADDR2
171 DATA3
172 ADDR3
173 VDD3OP
174 VSS3OP
175 DATA4
176 ADDR4
177 DATA5
178 ADDR5
179 DATA6
180 ADDR6
181 DATA7
182 ADDR7
183 DATA8
184 ADDR8
185 DATA9
186 ADDR9
187 VDD
188 VSS
189 DATA10
190 ADDR10
191 DATA11
192 ADDR11
193 VDD3OP
194 VSS3OP
195 DATA12
196 ADDR12
197 DATA13
198 ADDR13
199 DATA14
200 ADDR14
201 DATA15
202 ADDR15
203 nSCS0
204 nSCS1/GPA0
205 nSCS2/GPA1
206 nSCS3/GPA2
207 nSDCS0/nDRAS0
208 nSDCS1/nDRAS1/GPA3
S3C2800X
208-LQFP
- VDD / VSS : Internal 1.8V power
- AVDD / AVSS : Analog 1.8V Power
- VDD3OP / VSS3OP : I/O 3.3V power

DNIe2nd Data Sheet
(Simple Vesion)

CONTENTS

1. General Description

2. Feature
   2.1 Input
   2.2 Output
   2.3 Function

3. Functional Block Diagram

4. Pin Description

5. Package

6. Function Description
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   6.2 TIMING_GEN
   6.3 NRP(Noise Reduction Processor)
   6.4 SOURCE DETECTION

1. General Description

This second DNIe project for Screen Quality Enhancement was proceeded conducted following the first CFT project. It proceeded was conducted from April to December of 2002 and resolved the problems that occurred during the first CFT project and added several algorithms to enhance screen quality.

For the 2nd DNIe 2nd, 10 major 10 algorithms were applied:
4 algorithms used in the first CFT project: NR (Noise Reduction), DE (Detail Enhancement), CE (Contrast Enhancement), and WtEP (White-tone Enhancement Processor). and 6 Nhewly added 6 algorithms: DCE (Detail Contrast Enhancement), CTI (Color Transition Improvement), BWS (Black & White Stretch), CTE (Color Tone Enhancement), Deblocking, Source Characteristics Analysis.

▶ Noise Reduction

- Spatial N/R introduction

=> In During the 1st DNIe 1st, only a temporal N/R was performed, and the N/R effect was not maximized. EspeciallyMost notably, there was occurred thea side effect thatof screen dragging which occuroccurred s when the temporal N/R gain iswas set toat a large value for the signals that have muchhad a lot of noise.

InDuring the 2nd DNIe 2nd, a spatial N/R equippeding with a built-in edge detection circuit was added to overcome this shortcoming, and the N/R effect was successfully maximized without screen dragging even for the signals that havehad a lot of much noise.

▶ Detail Enhancement

- Resolution to Noise Boost

=> InDuring the 1st DNIe 1st, there was also the problem that noise iswas boosted.

Though the noise boost was suppressed with a coring circuit, there was a limitation and it cannotcould not engage a large gain to the signal such as an RF that hashad a lot of much noise.

The 2nd DNIe 2nd added a back noise detection circuit beside the coring circuit and onlythe signal was enhanced without noise boost.

▶ Contrast Enhancement

- Removal of Flickering that Occurred dDuring Rapid Screen Switching

=> InDuring the 1st DNIe 1st, there was a flickering problem because the mapping function changeds too rapidly according to the variation of the input histogram.

InDuring the 2nd DNIe 2nd, an IIR filter was used forto input the screen histogram and the flickering that occurred during the rapid screen switching was

minimized.

- Suppression of Noise Boost in Enhanced Contrast

=> The 1st DNIe 1st has also had the problem thatof boosted noise is boosted when the contrast i was enhanced.

The 2nd DNIe 2nd applied an LPF for the amount of contrast enhancement and suppressed the noise boost.

▶ White-tone Enhancement Processor

- Color Temperature Enhancement for Achromatic Area

▶ Detail Contrast Enhancement

- Enhanced contrast in local area.
- Suppressed noise boost during local contrast enhancement.

▶ Colot Transition Improvement

- Sharpened color boundaries

▶ Black and White Stretch

- The Ddark area was made darker and the bright area was made brighter.

▶ Color Tone Enhancement

- The Ccolor density of the input signal was optimized so that it becomesbecame adaptive.

▶ Source Characteristics Analysis

- Detects frequency characteristics for the input signal and changes gain automatically in each algorithm.

▶ De-blocking

- Removes the block artifact that is generateds in an MPEG signal.

BesidesIn addition, the 2nd DNIe 2nd has added these functions: of Built-in Test Pattern Generation, Color Matrix Conversion, and Response to Various Display Sizes.
Overall development proceeded with the following stages: of ① Algorithm vVerification , ② High lLevel dDesign (VHDL), ③ Simulation & mModification, ④ Synthesis & Layout. The fourth stage proceeded was conducted in cooperation with SMT, an external company.
The developed 2nd DNIe IC developed 2ndIC is planned to be applied to the DLP first. It seems that it can also be applied to LCD and CRT TV.

2. Feature

2.1 Input

- ▶ Digital RGB or Digital YCbCr (Each has 8-bit 4:4:4, 656, or 601 format.)
- ▶ I2C cControl bBus (SCL and SDA)
  - Device aAddress: Supports 4 different settings.
  - 16-bit aAddress / 16-bit dData
- ▶ Provides thea built-in halftone function with OSD inputs (inputs of YS and YM).
- ▶ Provides thea built-in MUX function with HD data inputs (For data input only).
- ▶ Sync sSignal: Usesd H/V. Each edge is selectable.
- ▶ Input cClock: Provides thean internal phase inversion function.
- ▶ Operating fFrequency: 80 MHz or less
- ▶ Provides RGB to YCbCr and YCbCr to YCbCr range conversions using a built-in 10-bit counter of 3X3 matrix.
- ▶ Internal operations are processed in YCbCr format.

2.2 Output

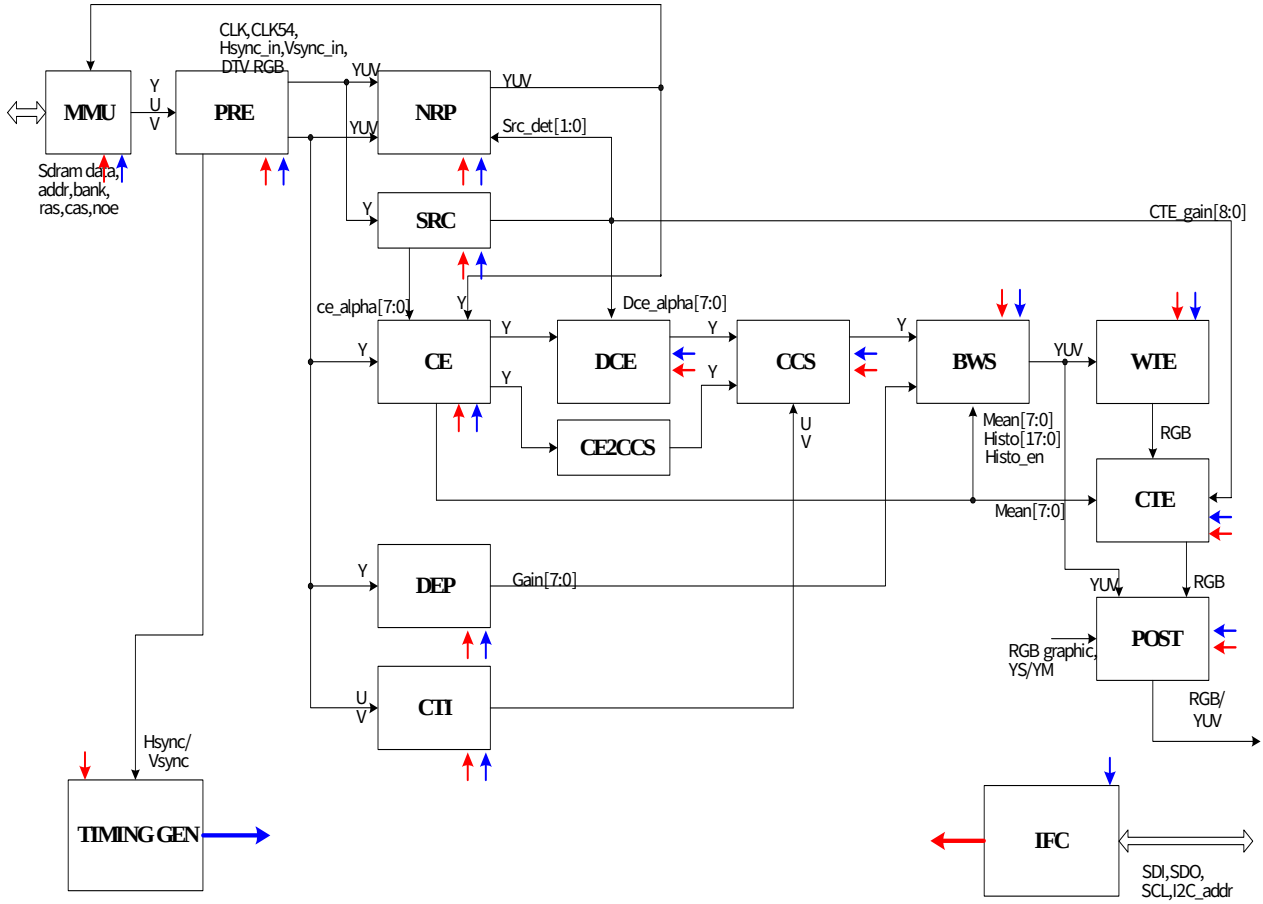
- ▶ Digital RGB (8/10/16-bit 4:4:4), Digital YCbCr (8/10/16-bit 4:4:4) Output modes:
- ▶ Output mode :
  - Outputs 8 bits for RGB/YCbCr per clock
  - Outputs 10 bits for RGB/YCbCr per clock
  - Outputs 16 bits (even/odd) for RGB/YCbCr per 1/2 clock
- ▶ Resolution rRange: Variation is possible within the range of the 2048 horizontal 2048 pixels by 1000 vertical 1000 lines.
  (Ex.720*480p,720*576i,852*480p,1024*768p,1280*720p,1280*768p,1366*768p, 1920*1080i등)
- ▶ Output sSync sSignal: H/V and DE (Phase, width, and position can be specified for both of them.)
- ▶ Provides YCbCr to RGB range conversion using a built-in 10-bit counter of 3X3 matrix.

2.3 Function

- ▶ Internal tTest pPattern gGeneration (No sync signal is required for operation.)
  - Pattern : Full Window Pattern, 9 point box Pattern, Color Bar Pattern, Cross Hatch Pattern, Dot Array Pattern, Horizontal & Vertical RampPattern

- RGB to YCbCr or YCbCr to YCbCr rRange cConversion
  - For CMC (Color Matrix Conversion), nine (9) 11-bit counters can be set from the externally.
  - If YCbCr has the range of Y[16~235], CB, and CR[16~240], it can be converted to a full range signal using the CMC.
  - Possible to adjust tint, color gain control, contrast, and brightness using the CMC.
- Provides the sScreen mMute and sStill fFunctions
- 3D Noise Reduction
- De-blocking
- Detail Enhancement
  - LTI (Luminance Transition Improvement) function, uUnder-sShoot/oOver-sShoot sSuppression
  - Noise bBoost sSuppression
- Contrast Enhancement
  - Uses hHistogram.
  - Maintains hues of the color area.
  - Compensates for the pale orange color.
  - Adapts to the flickering prevention circuit.
- Detail Contrast Enhancement
- Color Transition Improvement
- Black & White Stretch
- White-tone Enhancement Processor
- Color Tone Enhancement
- Source Detection
- Contrast/Brightness Control

3. Functional Block Diagram



4. Pin Description

PIN no.	PIN Name	I/O	Function
1	B_I2C_SDA	B	I2C Serial data
	I_I2C_SCL	I	I2C Serial clock
3	I_I2C_ADDR1	I	In the I2C device address, the usable (setting-possible) bits are the 2 bits that remain when the high 5 bits, fixed to "11001", are removed from the 7 bits (except the LSB bit for R/W).
4	I_I2C_ADDR0	I	
5	O_OUT_DIVCLK	O	2-bBranch oOutput cClock (Used in the even/odd data output mode)
6	I_SCAN_MODE	I	normal operation, connect to ground. IC Test
7	I_SCAN_ENABLE	I	normal operation, connect to ground. IC Test
8	O_OUT_DENAB	O	Output data enable
9	O_OUT_VSYNC	O	Output vertical sync
10	O_OUT_HSYNC	O	Output horizontal sync
11	VDD_3V3	P	3.3V power (Pad power)
12	O_OUT_CLK	O	Output cClock. 4 different phases can be selected with the OUTPUT_CLK_PHASE register.
13	VSS_3V3	G	Ground (Pad Ground)
14	O_OUTD_B15	O	Blue_data(15) output
15	O_OUTD_B14	O	Blue_data(14) output
16	O_OUTD_B13	O	Blue_data(13) output
17	O_OUTD_B12	O	Blue_data(12) output
18	O_OUTD_B11	O	Blue_data(11) output
19	O_OUTD_B10	O	Blue_data(10) output
20	O_OUTD_B9	O	Blue_data(9) output
21	VDD_1V8	P	1.8V power (Core power)
22	O_OUTD_B8	O	Blue_data(8) output
23	VSS_1V8	G	Ground (Core Ground)
24	B_OUTD_B7	B	R_OUTCON=0 output → Blue_data(7) output R_OUTCON=1 input → DTV_BIN(7)input(R_DTV_SWITCH=1)
25	B_OUTD_B6	B	R_OUTCON=0 output → Blue_data(6) output R_OUTCON=1 input → DTV_BIN(6)input(R_DTV_SWITCH=1)
26	B_OUTD_B5	B	R_OUTCON=0 output → Blue_data(5) output R_OUTCON=1 input → DTV_BIN(5)input(R_DTV_SWITCH=1) → OSD_Blue(5)input(R_DTV_SWITCH=0)

27	B_OUTD_B4	B	R_OUTCON=0 output → Blue_data(4) output R_OUTCON=1 input → DTV_BIN(4)input(R_DTV_SWITCH=1) → OSD_Blue(4)input(R_DTV_SWITCH=0)

Pin No.	Pin Name	I/O	Function
28	B_OUTD_B3	B	R_OUTCON=0 output → Blue_data(3) output R_OUTCON=1 input → DTV_BIN(3)input(R_DTV_SWITCH=1) → OSD_Blue(3)input(R_DTV_SWITCH=0)
29	B_OUTD_B2	B	R_OUTCON=0 output → Blue_data(2) output R_OUTCON=1 input → DTV_BIN(2)input(R_DTV_SWITCH=1) → OSD_Blue(2)input(R_DTV_SWITCH=0)
30	B_OUTD_B1	B	R_OUTCON=0 output → Blue_data(1) output R_OUTCON=1 input → DTV_BIN(1)input(R_DTV_SWITCH=1) → OSD_Blue(1)input(R_DTV_SWITCH=0)
31	B_OUTD_B0	B	R_OUTCON=0 output → Blue_data(0) output R_OUTCON=1 input → DTV_BIN(0)input(R_DTV_SWITCH=1) → OSD_Blue(0)input(R_DTV_SWITCH=0)
32	VDD_3V3	P	3.3V power (Pad power)
33	O_OUTD_G15	O	Green_data(15) output
34	VSS_3V3	G	Ground (Pad Ground)
35	O_OUTD_G14	O	Green_data(14) output
36	O_OUTD_G13	O	Green_data(13) output
37	O_OUTD_G12	O	Green_data(12) output
38	O_OUTD_G11	O	Green_data(11) output
39	O_OUTD_G10	O	Green_data(10) output
40	O_OUTD_G9	O	Green_data(9) output
41	VDD_1V8	P	1.8V power (Core power)
42	O_OUTD_G8	O	Green_data(8) output
43	VSS_1V8	G	Ground (Core Ground)
44	B_OUTD_G7	B	R_OUTCON=0 output → Green_data(7) output R_OUTCON=1 input → DTV_GIN(7)input(R_DTV_SWITCH=1)
45	B_OUTD_G6	B	R_OUTCON=0 output → Green_data(6) output R_OUTCON=1 input → DTV_GIN(6)input(R_DTV_SWITCH=1) → YMinput(R_DTV_SWITCH=0)
46	B_OUTD_G5	B	R_OUTCON=0 output → Green_data(5) output R_OUTCON=1 input → DTV_GIN(5)input(R_DTV_SWITCH=1) → OSD_G(5)input(R_DTV_SWITCH=0)

47	B_OUTD_G4	B	R_OUTCON=0 output → Green_data(4) output R_OUTCON=1 input → DTV_GIN(4)input(R_DTV_SWITCH=1) → OSD_G(4)input(R_DTV_SWITCH=0)
48	B_OUTD_G3	B	R_OUTCON=0 output → Green_data(3) output R_OUTCON=1 input → DTV_GIN(3)input(R_DTV_SWITCH=1) → OSD_G(3)input(R_DTV_SWITCH=0)
49	B_OUTD_G2	B	R_OUTCON=0 output → Green_data(2) output R_OUTCON=1 input → DTV_GIN(2)input(R_DTV_SWITCH=1) → OSD_G(2)input(R_DTV_SWITCH=0)
50	B_OUTD_G1	B	R_OUTCON=0 output → Green_data(1) output R_OUTCON=1 input → DTV_GIN(1)input(R_DTV_SWITCH=1) → OSD_G(1)input(R_DTV_SWITCH=0)
51	VDD_3V3	P	3.3V power (Pad power)
52	B_OUTD_G0	B	R_OUTCON=0 output → Green_data(0) output R_OUTCON=1 input → DTV_GIN(0)입력(R_DTV_SWITCH=1) → OSD_G(0)입력(R_DTV_SWITCH=0)
53	VSS_3V3	G	Ground (Pad Ground)
54	O_OUTD_R15	O	Red_data(15) output
55	O_OUTD_R14	O	Red_data(14) output
56	O_OUTD_R13	O	Red_data(13) output
57	O_OUTD_R12	O	Red_data(12) output
58	O_OUTD_R11	O	Red_data(11) output
59	O_OUTD_R10	O	Red_data(10) output
60	O_OUTD_R9	O	Red_data(9) output
61	O_OUTD_R8	O	Red_data(8) output
62	B_OUTD_R7	B	R_OUTCON=0 output → Red_data(7) output R_OUTCON=1 input → DTV_RIN(7)input(R_DTV_SWITCH=1)
63	VDD_3V3	P	3.3V power (Pad power)
64	B_OUTD_R6	B	R_OUTCON=0 output → Red_data(6) output R_OUTCON=1 input → DTV_RIN(6)input(R_DTV_SWITCH=1) → YS input(R_DTV_SWITCH=0)
65	VSS_3V3	G	Ground (Pad Ground)
66	B_OUTD_R5	B	R_OUTCON=0 output → Red_data(5) output R_OUTCON=1 input → DTV_RIN(5)input(R_DTV_SWITCH=1) → OSD_R(5)input(R_DTV_SWITCH=0)
67	B_OUTD_R4	B	R_OUTCON=0 output → Red_data(4) output R_OUTCON=1 input → DTV_RIN(4)input(R_DTV_SWITCH=1) → OSD_R(4)input(R_DTV_SWITCH=0)

Pin No.	Pin Name	I/O	Function
68	B_OUTD_R3	B	R_OUTCON=0 output → Red_data(3) output R_OUTCON=1 input → DTV_RIN(3)input(R_DTV_SWITCH=1) → OSD_R(3)input(R_DTV_SWITCH=0)
69	B_OUTD_R2	B	R_OUTCON=0 output → Red_data(2) output R_OUTCON=1 input → DTV_RIN(2)input(R_DTV_SWITCH=1) → OSD_R(2)input(R_DTV_SWITCH=0)
70	B_OUTD_R1	B	R_OUTCON=0 output → Red_data(1) output R_OUTCON=1 input → DTV_RIN(1)input(R_DTV_SWITCH=1) → OSD_R(1)input(R_DTV_SWITCH=0)
71	B_OUTD_R0	B	R_OUTCON=0 output → Red_data(0) output R_OUTCON=1 input → DTV_RIN(0)input(R_DTV_SWITCH=1) → OSD_R(0)input(R_DTV_SWITCH=0)
72	I_BIST_MODE	I	normal operation,connect to ground. IC Test
73	VDD_1V8	P	1.8V power (Core power)
74	I_nRESET	I	Asynchronous Reset
75	VSS_1V8	G	Ground (Core Ground)
76	B_SDRAM_DQ63	B	SDRAM_DATA(63) Input-output pot
77	B_SDRAM_DQ62	B	SDRAM_DATA(62) Input-output pot
78	B_SDRAM_DQ61	B	SDRAM_DATA(61) Input-output pot
79	B_SDRAM_DQ60	B	SDRAM_DATA(60) Input-output pot
80	B_SDRAM_DQ59	B	SDRAM_DATA(59) Input-output pot
81	B_SDRAM_DQ58	B	SDRAM_DATA(58) Input-output pot
82	VDD_3V3	P	3.3V power (Pad power)
83	B_SDRAM_DQ57	B	SDRAM_DATA(57) Input-output pot
84	VSS_3V3	G	Ground (Pad Ground)
85	B_SDRAM_DQ56	B	SDRAM_DATA(56) Input-output pot
86	B_SDRAM_DQ55	B	SDRAM_DATA(55) Input-output pot
87	B_SDRAM_DQ54	B	SDRAM_DATA(54) Input-output pot
88	B_SDRAM_DQ53	B	SDRAM_DATA(53) Input-output pot
89	B_SDRAM_DQ52	B	SDRAM_DATA(52) Input-output pot
90	B_SDRAM_DQ51	B	SDRAM_DATA(51) Input-output pot
91	B_SDRAM_DQ50	B	SDRAM_DATA(50) Input-output pot
92	B_SDRAM_DQ49	B	SDRAM_DATA(49) Input-output pot
93	VDD_1V8	P	1.8V power (Core power)
94	B_SDRAM_DQ48	B	SDRAM_DATA(48) Input-output pot

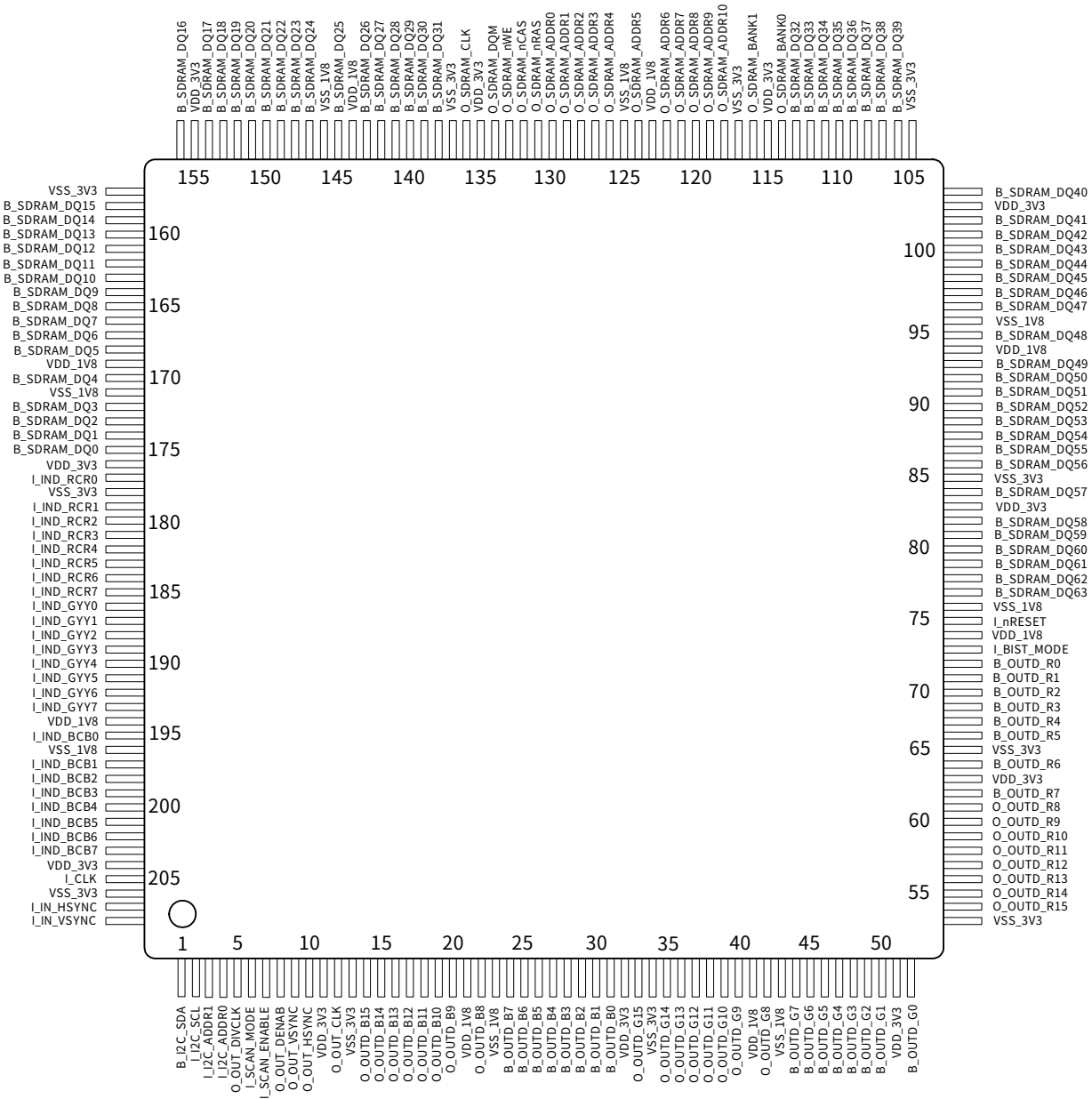
Pin No.	Pin Name	I/O	Function
95	VSS_1V8	G	Ground (Core Ground)
96	B_SDRAM_DQ47	B	SDRAM_DATA(47) Input-output pot
97	B_SDRAM_DQ46	B	SDRAM_DATA(46) Input-output pot
98	B_SDRAM_DQ45	B	SDRAM_DATA(45) Input-output pot
99	B_SDRAM_DQ44	B	SDRAM_DATA(44) Input-output pot
100	B_SDRAM_DQ43	B	SDRAM_DATA(43) Input-output pot
101	B_SDRAM_DQ42	B	SDRAM_DATA(42) Input-output pot
102	B_SDRAM_DQ41	B	SDRAM_DATA(41) Input-output pot
103	VDD_3V3	P	3.3V power (Pad power)
104	B_SDRAM_DQ40	B	SDRAM_DATA(40) Input-output pot
105	VSS_3V3	G	Ground (Pad Ground)
106	B_SDRAM_DQ39	B	SDRAM_DATA(39) Input-output pot
107	B_SDRAM_DQ38	B	SDRAM_DATA(38) Input-output pot
108	B_SDRAM_DQ37	B	SDRAM_DATA(37) Input-output pot
109	B_SDRAM_DQ36	B	SDRAM_DATA(36) Input-output pot
110	B_SDRAM_DQ35	B	SDRAM_DATA(35) Input-output pot
111	B_SDRAM_DQ34	B	SDRAM_DATA(34) Input-output pot
112	B_SDRAM_DQ33	B	SDRAM_DATA(33) Input-output pot
113	B_SDRAM_DQ32	B	SDRAM_DATA(32) Input-output pot
114	O_SDRAM_BANK0	O	SDRAM BANK0 (4 BANK used for sdram)
115	VDD_3V3	P	3.3V power (Pad power)
116	O_SDRAM_BANK1	O	SDRAM BANK1
117	VSS_3V3	G	Ground (Pad Ground)
118	O_SDRAM_ADDR10	O	SDRAM ADDRESS(10) output
119	O_SDRAM_ADDR9	O	SDRAM ADDRESS(9) output
120	O_SDRAM_ADDR8	O	SDRAM ADDRESS(8) output
121	O_SDRAM_ADDR7	O	SDRAM ADDRESS(7) output
122	O_SDRAM_ADDR6	O	SDRAM ADDRESS(6) output
123	VDD_1V8	P	1.8V power (Core power)
124	O_SDRAM_ADDR5	O	SDRAM ADDRESS(5) output
125	VSS_1V8	G	Ground (Core Ground)
126	O_SDRAM_ADDR4	O	SDRAM ADDRESS(4) output
127	O_SDRAM_ADDR3	O	SDRAM ADDRESS(3) output
128	O_SDRAM_ADDR2	O	SDRAM ADDRESS(2) output

Pin No.	Pin Name	I/O	Function
129	O_SDRAM_ADDR1	O	SDRAM ADDRESS(1) output
130	O_SDRAM_ADDR0	O	SDRAM ADDRESS(0) output
131	O_SDRAM_nRAS	O	SDRAM /RAS output
132	O_SDRAM_nCAS	O	SDRAM /CAS output
133	O_SDRAM_nWE	O	SDRAM /WE output
134	O_SDRAM_DQM	O	SDRAM DQM output
135	VDD_3V3	P	3.3V power (Pad power)
136	O_SDRAM_CLK	O	SDRAM CLK output
137	VSS_3V3	G	Ground (Pad Ground)
138	B_SDRAM_DQ31	B	SDRAM_DATA(31) Input-output pot
139	B_SDRAM_DQ30	B	SDRAM_DATA(30) Input-output pot
140	B_SDRAM_DQ29	B	SDRAM_DATA(29) Input-output pot
141	B_SDRAM_DQ28	B	SDRAM_DATA(28) Input-output pot
142	B_SDRAM_DQ27	B	SDRAM_DATA(27) Input-output pot
143	B_SDRAM_DQ26	B	SDRAM_DATA(26) Input-output pot
144	VDD_1V8	P	1.8V power (Core power)
145	B_SDRAM_DQ25	B	SDRAM_DATA(25) Input-output pot
146	VSS_1V8	G	Ground (Core Ground)
147	B_SDRAM_DQ24	B	SDRAM_DATA(24) Input-output pot
148	B_SDRAM_DQ23	B	SDRAM_DATA(23) Input-output pot
149	B_SDRAM_DQ22	B	SDRAM_DATA(22) Input-output pot
150	B_SDRAM_DQ21	B	SDRAM_DATA(21) Input-output pot
151	B_SDRAM_DQ20	B	SDRAM_DATA(20) Input-output pot
152	B_SDRAM_DQ19	B	SDRAM_DATA(19) Input-output pot
153	B_SDRAM_DQ18	B	SDRAM_DATA(18) Input-output pot
154	B_SDRAM_DQ17	B	SDRAM_DATA(17) Input-output pot
155	VDD_3V3	P	3.3V power (Pad power)
156	B_SDRAM_DQ16	B	SDRAM_DATA(16) Input-output pot
157	VSS_3V3	G	Ground (Pad Ground)
158	B_SDRAM_DQ15	B	SDRAM_DATA(15) Input-output pot
159	B_SDRAM_DQ14	B	SDRAM_DATA(14) Input-output pot
160	B_SDRAM_DQ13	B	SDRAM_DATA(13) Input-output pot
161	B_SDRAM_DQ12	B	SDRAM_DATA(12) Input-output pot
162	B_SDRAM_DQ11	B	SDRAM_DATA(11)Input-output pot
163	B_SDRAM_DQ10	B	SDRAM_DATA(10) Input-output pot

Pin No.	Pin Name	I/O	Function
164	B_SDRAM_DQ9	B	SDRAM_DATA(9) Input-output pot
165	B_SDRAM_DQ8	B	SDRAM_DATA(8) Input-output pot
166	B_SDRAM_DQ7	B	SDRAM_DATA(7) Input-output pot
167	B_SDRAM_DQ6	B	SDRAM_DATA(6) Input-output pot
168	B_SDRAM_DQ5	B	SDRAM_DATA(5) Input-output pot
169	VDD_1V8	P	1.8V power (Core power)
170	B_SDRAM_DQ4	B	SDRAM_DATA(4) Input-output pot
171	VSS_1V8	G	Ground (Core Ground)
172	B_SDRAM_DQ3	B	SDRAM_DATA(3) Input-output pot
173	B_SDRAM_DQ2	B	SDRAM_DATA(2) Input-output pot
174	B_SDRAM_DQ1	B	SDRAM_DATA(1) Input-output pot
175	B_SDRAM_DQ0	B	SDRAM_DATA(0) Input-output pot
176	VDD_3V3	P	3.3V power (Pad power)
177	I_IND_RCR0	I	RGB mode: R0, YCbCr mode: Cr0 Data input
178	VSS_3V3	G	Ground (Pad Ground)
179	I_IND_RCR1	I	RGB mode: R1, YCbCr mode: Cr1 Data input
180	I_IND_RCR2	I	RGB mode: R2, YCbCr mode: Cr2 Data input
181	I_IND_RCR3	I	RGB mode: R3, YCbCr mode: Cr3 Data input
182	I_IND_RCR4	I	RGB mode: R4, YCbCr mode: Cr4 Data input
183	I_IND_RCR5	I	RGB mode: R5, YCbCr mode: Cr5 Data input
184	I_IND_RCR6	I	RGB mode: R6, YCbCr mode: Cr6 Data input
185	I_IND_RCR7	I	RGB mode: R7, YCbCr mode: Cr7 Data input
186	I_IND_GYY0	I	RGB mode: G0, YCbCr mode: Y0 Data input
187	I_IND_GYY1	I	RGB mode: G1, YCbCr mode: Y1 Data input
188	I_IND_GYY2	I	RGB mode: G2, YCbCr mode: Y2 Data input
189	I_IND_GYY3	I	RGB mode: G3, YCbCr mode: Y3 Data input
190	I_IND_GYY4	I	RGB mode: G4, YCbCr mode: Y4 Data 입input
191	I_IND_GYY5	I	RGB mode: G5, YCbCr mode: Y5 Data input
192	I_IND_GYY6	I	RGB mode: G6, YCbCr mode: Y6 Data input
193	I_IND_GYY7	I	RGB mode: G7, YCbCr mode: Y7 Data input
194	VDD_1V8	P	1.8V power (Core power)
195	I_IND_BCB0	I	RGB mode: B0, YCbCr mode: Cb0 Data input
196	VSS_1V8	G	Ground (Core Ground)
197	I_IND_BCB1	I	RGB mode: B1, YCbCr mode: Cb1 Data input
198	I_IND_BCB2	I	RGB mode: B2, YCbCr mode: Cb2 Data input

Pin No.	Pin Name	I/O	Function
199	I_IND_BCB3	I	RGB mode: B3, YCbCr mode: Cb3 Data input
200	I_IND_BCB4	I	RGB mode: B4, YCbCr mode: Cb4 Data input
201	I_IND_BCB5	I	RGB mode: B5, YCbCr mode: Cb5 Data input
202	I_IND_BCB6	I	RGB mode: B6, YCbCr mode: Cb6 Data input
203	I_IND_BCB7	I	RGB mode: B7, YCbCr mode: Cb7 Data input
204	VDD_3V3	P	3.3V power (Pad power)
205	I_CLK	I	CLK input
206	VSS_3V3	G	Ground (Pad Ground)
207	I_IN_HSYNC	I	Horizontal sSync sSignal iInput
208	I_IN_VSYNC	I	Vertical sSync sSignal iInput

5. Package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VDD_3V3
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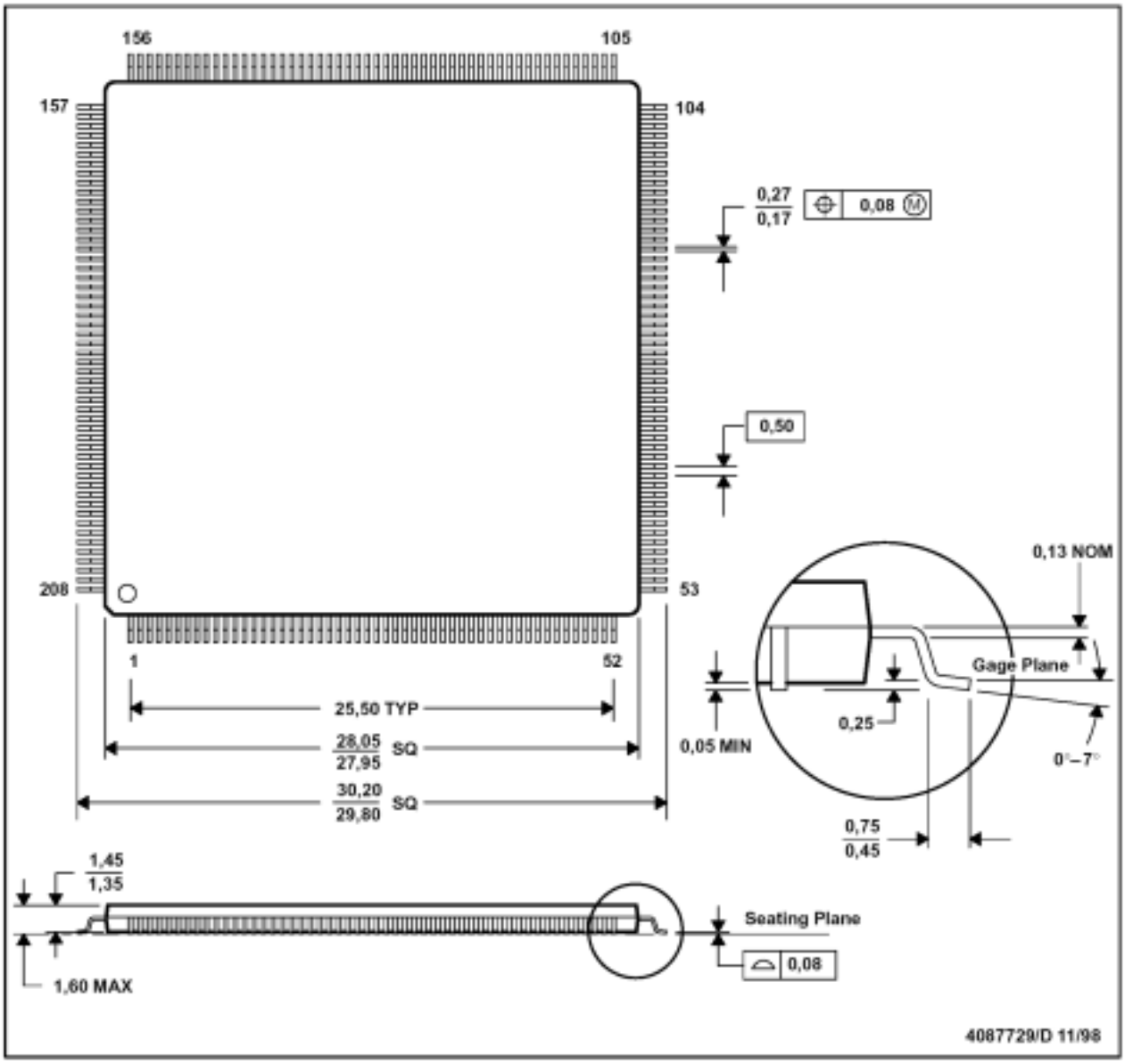
B_SDRAM_DQ18
B_SDRAM_DQ19
B_SDRAM_DQ20
B_SDRAM_DQ21
B_SDRAM_DQ22
B_SDRAM_DQ23
B_SDRAM_DQ24
VSS_1V8
B_SDRAM_DQ25
VDD_1V8
B_SDRAM_DQ26
B_SDRAM_DQ27
B_SDRAM_DQ28
B_SDRAM_DQ29
B_SDRAM_DQ30
B_SDRAM_DQ31
VSS_3V3
O_SDRAM_CLK
VDD_3V3
O_SDRAM_DQM
O_SDRAM_nWE
O_SDRAM_nCAS
O_SDRAM_nRAS
O_SDRAM_ADDR0
O_SDRAM_ADDR1
O_SDRAM_ADDR2
O_SDRAM_ADDR3
O_SDRAM_ADDR4
VSS_1V8
O_SDRAM_ADDR5
VDD_1V8
O_SDRAM_ADDR6
O_SDRAM_ADDR7
O_SDRAM_ADDR8
O_SDRAM_ADDR9
O_SDRAM_ADDR10
VSS_3V3
O_SDRAM_BANK1
VDD_3V3
O_SDRAM_BANK0
B_SDRAM_DQ32
B_SDRAM_DQ33
B_SDRAM_DQ34
B_SDRAM_DQ35
B_SDRAM_DQ36
B_SDRAM_DQ37
B_SDRAM_DQ38
B_SDRAM_DQ39
VSS_3V3
155
150
145
140
135
130
125
120
115
110
105
VSS_3V3
B_SDRAM_DQ15
B_SDRAM_DQ14
B_SDRAM_DQ13
B_SDRAM_DQ12
B_SDRAM_DQ11
B_SDRAM_DQ10
B_SDRAM_DQ9
B_SDRAM_DQ8
B_SDRAM_DQ7
B_SDRAM_DQ6
B_SDRAM_DQ5
VDD_1V8
B_SDRAM_DQ4
VSS_1V8
B_SDRAM_DQ3
B_SDRAM_DQ2
B_SDRAM_DQ1
B_SDRAM_DQ0
VDD_3V3
I_IND_RCR0
VSS_3V3
I_IND_RCR1
I_IND_RCR2
I_IND_RCR3
I_IND_RCR4
I_IND_RCR5
I_IND_RCR6
I_IND_RCR7
I_IND_GYY0
I_IND_GYY1
I_IND_GYY2
I_IND_GYY3
I_IND_GYY4
I_IND_GYY5
I_IND_GYY6
I_IND_GYY7
VDD_1V8
I_IND_BCB0
VSS_1V8
I_IND_BCB1
I_IND_BCB2
I_IND_BCB3
I_IND_BCB4
I_IND_BCB5
I_IND_BCB6
I_IND_BCB7
VDD_3V3
I_CLK
VSS_3V3
I_IN_HSYNC
I_IN_VSYNC
160
165
170
175
180
185
190
195
200
205
1
5
10
15
20
25
30
35
40
45
50
100
95
90
85
80
75
70
65
60
55
B_SDRAM_DQ40
VDD_3V3
B_SDRAM_DQ41
B_SDRAM_DQ42
B_SDRAM_DQ43
B_SDRAM_DQ44
B_SDRAM_DQ45
B_SDRAM_DQ46
B_SDRAM_DQ47
VSS_1V8
B_SDRAM_DQ48
VDD_1V8
B_SDRAM_DQ49
B_SDRAM_DQ50
B_SDRAM_DQ51
B_SDRAM_DQ52
B_SDRAM_DQ53
B_SDRAM_DQ54
B_SDRAM_DQ55
B_SDRAM_DQ56
VSS_3V3
B_SDRAM_DQ57
VDD_3V3
B_SDRAM_DQ58
B_SDRAM_DQ59
B_SDRAM_DQ60
B_SDRAM_DQ61
B_SDRAM_DQ62
B_SDRAM_DQ63
VSS_1V8
I_nRESET
VDD_1V8
I_BIST_MODE
B_OUTD_R0
B_OUTD_R1
B_OUTD_R2
B_OUTD_R3
B_OUTD_R4
B_OUTD_R5
VSS_3V3
B_OUTD_R6
VDD_3V3
B_OUTD_R7
O_OUTD_R8
O_OUTD_R9
O_OUTD_R10
O_OUTD_R11
O_OUTD_R12
O_OUTD_R13
O_OUTD_R14
O_OUTD_R15
VSS_3V3
B_I2C_SDA
I_I2C_SCL
I_I2C_ADDR1
I_I2C_ADDR0
O_OUT_DIVCLK
I_SCAN_MODE
I_SCAN_ENABLE
O_OUT_DENAB
O_OUT_VSYNC
O_OUT_HSYNC
VDD_3V3
O_OUT_CLK
VSS_3V3
O_OUTD_B15
O_OUTD_B14
O_OUTD_B13
O_OUTD_B12
O_OUTD_B11
O_OUTD_B10
O_OUTD_B9
VDD_1V8
O_OUTD_B8
VSS_1V8
B_OUTD_B7
B_OUTD_B6
B_OUTD_B5
B_OUTD_B4
B_OUTD_B3
B_OUTD_B2
B_OUTD_B1
B_OUTD_B0
VDD_3V3
O_OUTD_G15
VSS_3V3
O_OUTD_G14
O_OUTD_G13
O_OUTD_G12
O_OUTD_G11
O_OUTD_G10
O_OUTD_G9
VDD_1V8
O_OUTD_G8
VSS_1V8
B_OUTD_G7
B_OUTD_G6
B_OUTD_G5
B_OUTD_G4
B_OUTD_G3
B_OUTD_G2
B_OUTD_G1
VDD_3V3
B_OUTD_G0



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

6. Function Description

6.1 IFC(InterFace Control)

The Interface Control Block (henceforth, IFC) controls the internal register value changes via I2C communications and downloads the LUT RAM to be used for internal processing (contrast enhancement).
The use of I2C protocol supports 16-bit addressing and 16-bit data width.
The basic I2C protocol requires 8-bit device addressing (incl. read/write flag) and 8-bit local base addressing. Hence, the designed I2C Control Block has a different sequence from the basic I2C control block for 16-bit operation.
Micom requires one device addressing device (write) and two 8-bit local addressing functions for data transfer to the slave. It requires one device addressing device (write), two 8-bit local addressing, and one additional device addressing device (read) for data reception from the slave.
The designedI2C Control Block is designed to can send/receive data to/from an asynchronous block. If the arriving timing of the arriving request data to the I2C block is delayed, the falling time of the SCL is pushed forward at acknowledge to decode the data properly.
Besides transferring register settings and LUT values, the IFC generates control signals for initialization, complete notification and mute control, etc.

6.1.1 Feature

- 7-bit Slave Addressing
- 16-bit Base Addressing Mode
- 16-bit Data Processing
- Asynchronous Data transmission

6.1.2 Operation

When the salve is determined by a 7-bit slave address after setting the start condition, data send/receiving is determined by the LSB bit. Then, forWhen sending data sending, the 2-byte internal base address is written in the order of high andto low byte and then the data is transferred in the order of high andto low byte.
When the data transfer finishes, the write sequence is reset with the stop condition.
More than 1-word data areis transferred in burst mode as shown in **Figure 6.1-1**. Each byte of the transferred data is saved to the corresponding address in incrementsed byof one, sequentially starting from the base address transferred.
In **Figure 6.1-1**, the black color indicates the space occupied by the master bus, and the blue color indicates the space occupied by the slave bus.

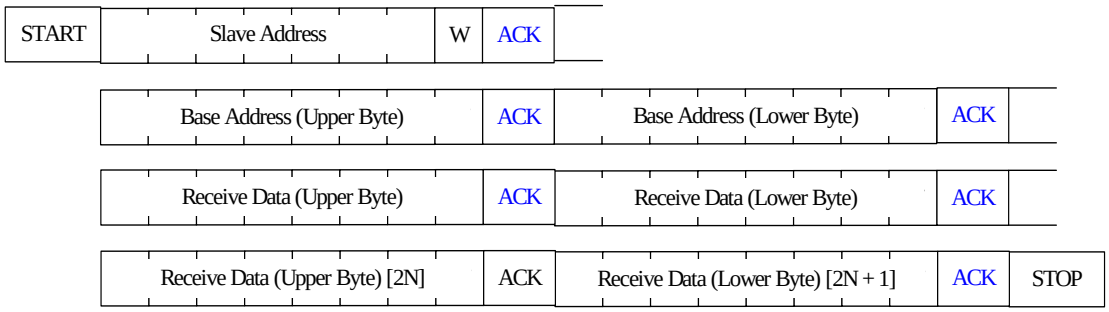


Figure 6.1-1 I2C 16-Bit Write Sequence

For receiving data receiving, the base address to read is written in write mode and the write sequence is initialized by loading the stop condition on the bus.
Then, the start condition is loaded onto the bus again and 7-bit slave addressing is performed in read mode. After thenthat, data areis received from the specified slave address, and the master sends an acknowledgmente signal every 8 bits and makes a word by combining the first byte as high byte and the second byte as low byte.
For received data received in burst mode, each byte of the transferred data is saved to the corresponding address in incrementsed byof one from the base address thatwhich is determined by the base addressing based on the transferred base address.

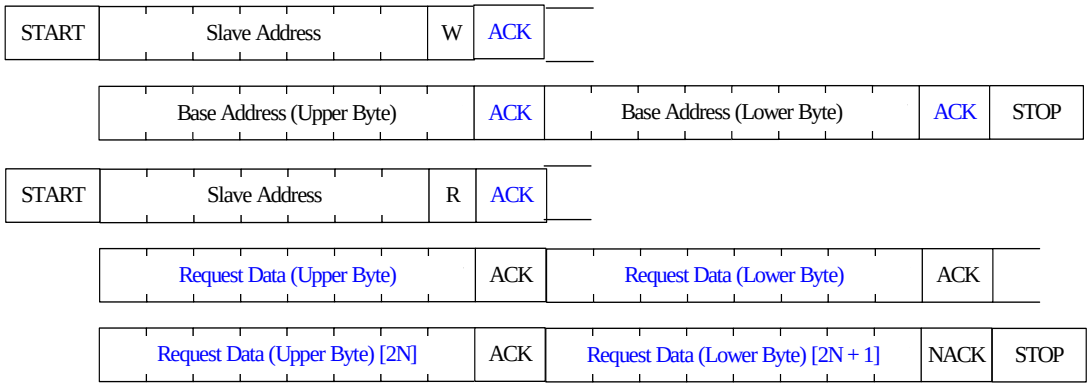


Figure 6.1-2 I2C 16-Bit Read Sequence

In case ofDuring a read sequence, if the receiving party (Master) wants to stop data reception from the slave addressed, it should first load no acknowledgmente first and then it can load stop the condition onto the bus.
If acknowledgmente is continuously loaded continuously, the bus is continuously occupied continuously by the slave tofor sending data and the master cannot load any data onto the bus except at the time of acknowledgment.

6.2 Timing Generator

SNI2ND data input operates according to the register settings related to the vertical/horizontal sync signals. The vertical/horizontal raster and valid input data positions are determined accordingly.

Basically, the input raster size areis the same withas the output raster size and the frame rate does not change also.

The Pphase of the input vertical/horizontal sync signal can be selected through the VSYNC_POLARITY and HSYNC_POLARITY registers.

[Fig 6.2-1] shows an example of when the value of two phase-related registers is "0", i.e., active low.

The width of the sync signal has no effect on the operation.

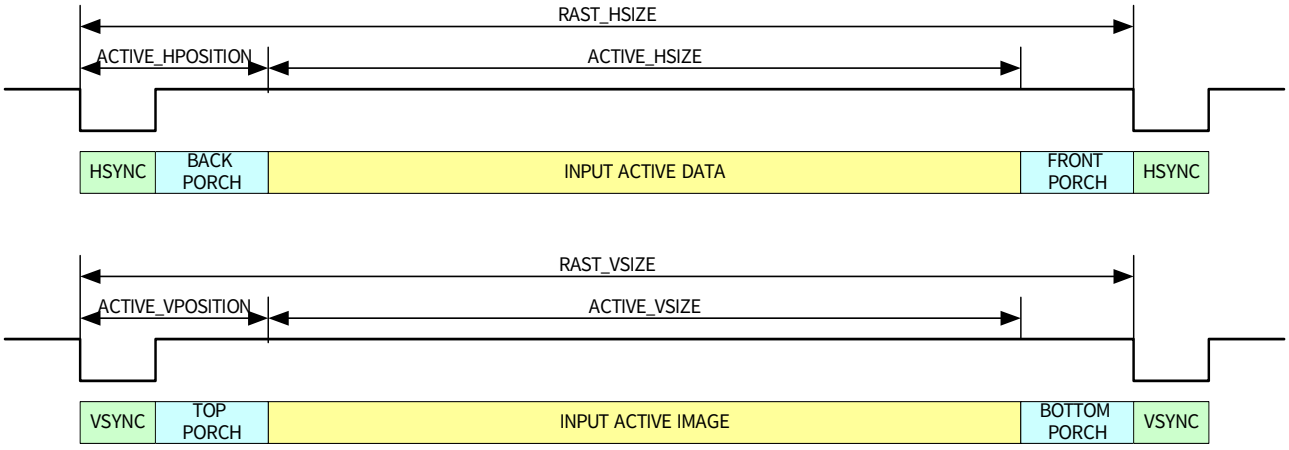


Figure 6.2-1 Registers Related to Vertical/Horizontal Input Sync Signals

6.3 NRP(Noise Reduction Process)

6.3.1 Feature

● Advantages of the 2nd DNIe 2nd NRP

☞ When there is little noise, itsthe noise removal function does not occurcause any damage to the image and acquirescreates a correctclear image by measuring the noise and motion of the motion adaptive temporal filter.
☞ When there is a lot of much noise, itsthe noise removal function occurscreates a minimum of damage to the edge by using the noise value measured by Temporal NR adapting (the noise adaptive spatial noise reduction function).

● Differences of between the 2nd DNIe 2nd and the 1st DNIe

☞ The 2D Spatial NR function is has been added.
☞ 2D NR's threshold value is obtained by using the noise value measured by the Temporal NR.
☞ Improved rounding for of the recursive filter resolves the problem of a colored after image.

The NR algorithm applied into the 2nd DNIe 2nd is a 3D Adaptive Noise Reduction algorithm that combines Temporal Noise Reduction to remove noise in the temporal space between frames and Spatial Noise Reduction to remove noise in 2-dimensinal space.

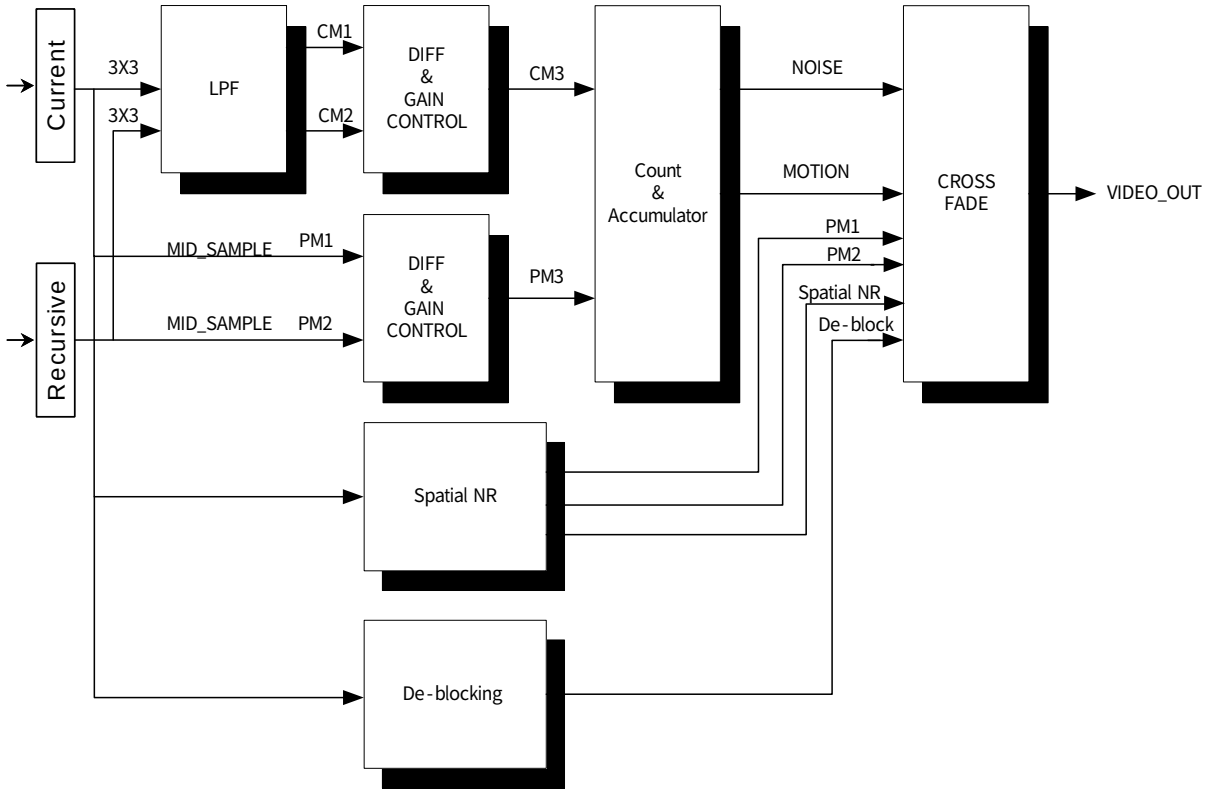


Figure 6.3-1 NRP Block Diagram

6.3.2 Operation

▶ The effect of **Temporal NR** can be increased or decreased by adjusting the following registers.

☞ **R_SCALE_MAX_Y**: Max value of the adaptive range that determines the NR effect for the brightness signal
☞ **R_SCALE_MIN_Y**: Min value of the adaptive range that determines the NR effect for the brightness signal
☞ **R_SCALE_MAX_C**: Max value of the adaptive range that determines the NR effect for the color signal
☞ **R_SCALE_MIN_C**: Min value of the adaptive range that determines the NR effect for the color signal
☞ ▶ The effect of the **Spatial NR** can be increased or decreased by adjusting the following registers.

☞ **R_Y_TH_HPF:** Threshold value for the high pass filter of the Spatial NR. [Range: 1/2, 1/4, 1/8 ~ 1/256] The larger this value is, the less the effect ofthe Spatial NR has.
☞ **R_Y_TH_EDGE:** Threshold value for the edge filter of the Spatial NR. [Range: 1/2, 1/4, 1/8 ~ 1/256] The larger this value is, the less the effect ofthe Spatial NR has.

SCALEMAX	SCALEMIN	Afterimage	NR eEffect
Large	Large	Decreased	Decreased
Large	Small	Increased	Adaptivity is increased.
Small	Large	Decreased	Adaptivity is decreased.
Small	Small	Increased	Increased

▶ De-bBlocking mMode can be selected by adjusting the following registers.

☞ **R_DEB_MODE :** Determines whether to enable or disable the dDe-bBlocking block operation.

R_DEB_MODE	00	01	10	11
Process	H,V Deblocking	H Deblocking	V Deblocking	LPF
Coefficient	0.25 0.75	0.25 0.75	0.25 0.75	[1 2 1]

▶ De-bBlocking mMode can be selected by adjusting the following registers.

☞ **R_MIX_MODE_EN**: Determines whether to mix the Spatial NR value with the De-bBlocking value.

☞ **R_DEB_EN**: Determines whether to enable or disable the dDe-bBlocking block operation.

☞ **R_NR_SEL**: Determines whether to select Spatial NR or Temporal NR for deblocking.

R_NR_SEL / R_DEB_EN	0	1		2	3	
		R_MIX_MODE_EN			R_MIX_MODE_EN	
		0	1		0	1
0	Deblocking + Temporal NR	Spatial NR	Spatial NR	Temporal NR	Spatial NR + Temporal NR	Spatial NR + Temporal NR
1	Deblocking	Deblocking	Deblocking + Spatial NR	Deblocking + Temporal NR	Deblocking + Temporal NR	Deblocking + Spatial NR + Temporal NR

6.4 SRC(Source Detection)

The SRC block controls the gain of the other blocks by detecting the RF characteristics of the input video.

1) Determines the RF characteristics by detecting the max frequency of the input video.
2) Controls gain by combining the RF characteristics detected and the noise information received from the noise reduction block.
3) Possible to extract the desired frequency by changing the register settings.
4) All processes in the SRC block are treated in the unit of a frame.

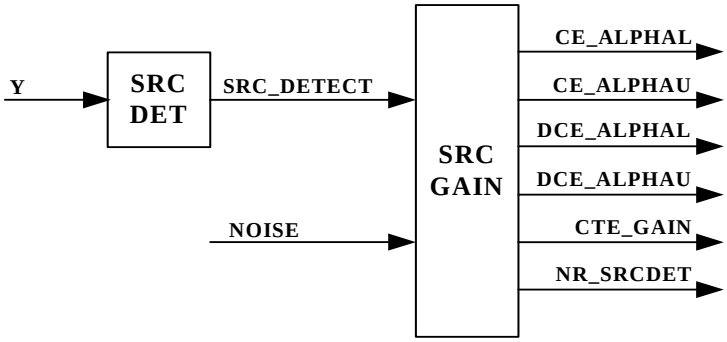


Figure 6.4-1 SRC Block Diagram

** Major Registers

FREQ 1 ~ 3 determines the boundaries for separation. Especially, FREQ1 and CTE give an eaffect to the gain of NR.
The CTE reduces gain for the images whose frequency is less than the FREQ1 value. SoTherefore, if the FREQ1 value is decreased, the gain decrease can be reduced but sensitivity to noise may be increased.
IIR_NOISE is the counter for the IIR Filter. If its value is small, the image can be followed fast because the gain matches it more nearlyclosely, but screen flickering can be generated.
HIGHNOISE and LOWNOISE reduce gain according to noise.
If their values are large, the gain increases but a noise boost may occur because the gain decrease is blocked.
In addition, if the difference between the HIGHNOISE and LOWNOISE values, i.e. if the slope is too steep, and gain may vary too rapidly.
NOISE_SLOPE value is determined by a formula that hasuses the HIGHNOISE and LOWNOISE values as parameters.

Multiformat SD, Progressive Scan/HDTV Video Encoder with Six NSV™ 12-Bit DACs

ADV7300A/ADV7301A

FEATURES

High Definition Input Formats
- YCrCb Compliant to SMPTE293M (525 p), ITU-R.BT1358 (625 p), SMPTE274M (1080 i), SMPTE296M (720 p), and Any Other High Definition Standard Using Async Timing Mode
- RGB in 3 × 10-Bit 4:4:4 Format
- BTA T-1004 EDTV2 525 p Parallel

High Definition Output Formats (525 p/625 p/720 p/1080 i)
- YPrPb Progressive Scan (EIA-770.1, EIA-770.2)
- YPrPb HDTV (EIA 770.3)
- RGB + H/V (HDTV 5-Wire Format)
- CGMS-A (720 p/1080 i)
- Macrovision Rev 1.0 (525 p/625 p)*
  - CGMS-A (525 p)

Standard Definition Input Formats
- CCIR-656 4:2:2 8-/10-Bit Parallel Input
- CCIR-601 4:2:2 16-/20-Bit Parallel Input

Standard Definition Output Formats
- Composite NTSC M, N;
  - PAL M, N, B, D, G, H, I, PAL-60
- SMPTE170M NTSC Compatible Composite Video
- ITU-R.BT470 PAL Compatible Composite Video
- S-Video (Y/C)
- EuroScart RGB
- Component YUV (Betacam, MII, SMPTE/EBU N10)
- Macrovision Rev 7.1*
  - CGMS/WSS
  - Closed Captioning

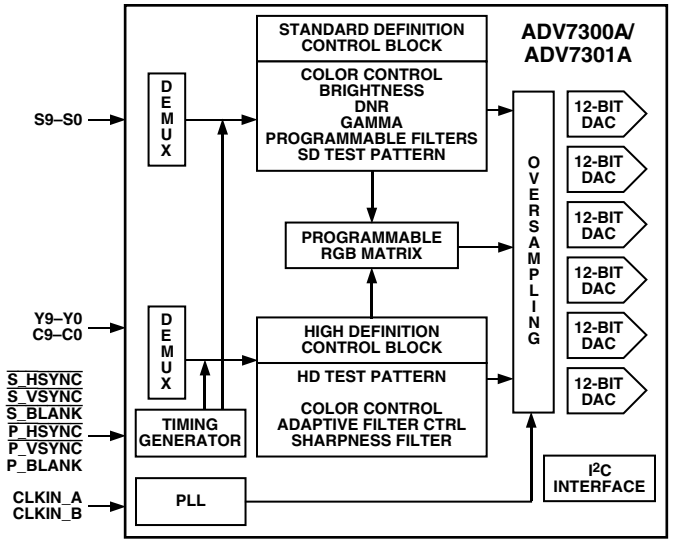
GENERAL FEATURES

- Simultaneous SD and HD Inputs and Outputs
- Oversampling (108 MHz/148.5 MHz)
- On-Board Voltage Reference
- 6 NSV Precision Video 12-Bit DACs
- 2-Wire Serial MPU Interface
- Dual I/O Supply 2.5 V/3.3 V Operation
- Analog and Digital Supply 2.5 V
- On-Board PLL
- 64-LQFP Package
- Lead-Free Product

APPLICATIONS

- High End DVD Players
- SD/Program Scan/HDTV Display Devices
- SD/Program Scan/HDTV Set-Top Boxes
- SD/HDTV Studio Equipment

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADV7300A/ADV7301A is a high speed, digital-to-analog encoder on a single monolithic chip. It includes six high speed video D/A converters with TTL compatible inputs.

The ADV7300A/ADV7301A has three separate 10-bit wide input ports that accept data in high definition and/or standard definition video format. For all standards, external horizontal, vertical, and blanking signals, or EAV/SAV timing codes, control the insertion of appropriate synchronization signals into the digital data stream and therefore the output signals.

NSV (Noise Shaped Video) is a trademark of Analog Devices, Inc.
*ADV7300A Only

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

ADV7300A/ADV7301A

DETAILED FEATURES

High Definition Programmable Features (720 p/1080 i)
- **2× Oversampling (148.5 MHz)**
- **Internal Test Pattern Generator (Color Hatch, Black Bar, Flat Field/Frame)**
- **Fully Programmable YCrCb to RGB Matrix**
- **Gamma Correction**
- **Programmable Adaptive Filter Control**
- **Programmable Sharpness Filter Control**
- **CGMS-A (720 p/1080 i)**

High Definition Programmable Features (525 p/625 p)
- **4× Oversampling (108 MHz Output)**
- **Internal Test Pattern Generator (Color Hatch, Black Bar, Flat Frame)**
- **Individual Y and PrPb Output Delay**
- **Gamma Correction**
- **Programmable Adaptive Filter Control**
- **Fully Programmable YCrCb to RGB Matrix**
- **Undershoot Limiter**
- **Macrovision Rev 1.0 (525 p/625 p)***
- **CGMS-A (525 p)**

Standard Definition Programmable Features
- **8× Oversampling (108 MHz)**
- **Internal Test Pattern Generator (Color Bars, Black Bar)**
- **Controlled Edge Rates for Sync, Active Video**
- **Individual Y and UV Output Delay**
- **Gamma Correction**
- **Digital Noise Reduction**
- **Multiple Chroma and Luma Filters**
- **Luma-SSAF™ Filter with Programmable Gain/ Attenuation**
- **UV SSAF**
- **Separate Pedestal Control on Component and Composite/S-Video Outputs**
- **VCR FF/RW Sync Mode**
- **Macrovision Rev 7.1***
- **CGMS/WSS**
- **Closed Captioning**

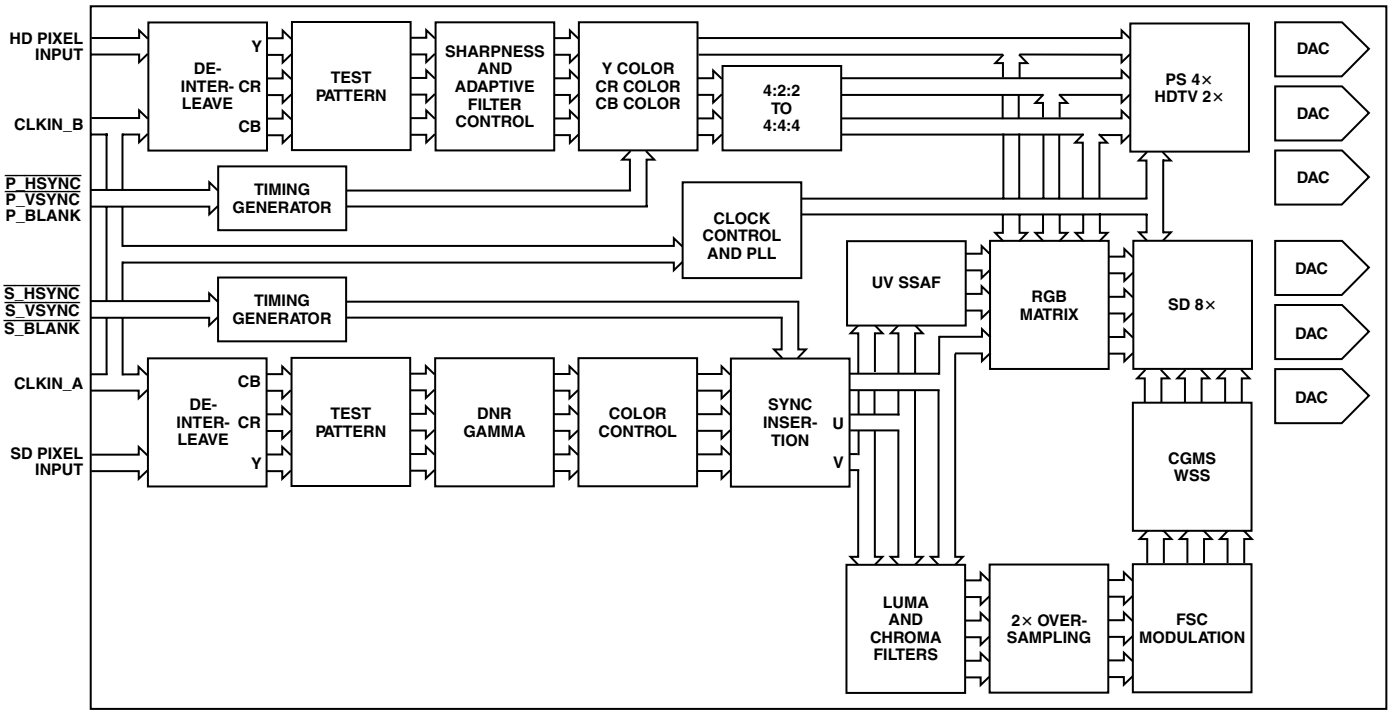


Figure 1. Functional Block Diagram

TERMS USED IN THIS DATA SHEET

SD Standard Definition Video, conforming to ITU-R.BT601/ITU-R.BT656.

HD High Definition Video, i.e., Progressive Scan or HDTV.

PS Progressive Scan Video, conforming to SMPTE293M or ITU-R.BT1358.

HDTV High Definition Television Video, conforming to SMPTE274M or SMPTE296M.

YCrCb SD or HD Component Digital Video.

YPrPb HD Component Analog Video.

YUV SD Component Analog Video.

SSAF is a trademark of Analog Devices, Inc.
*ADV7300A Only

ADV7300A/ADV7301A–SPECIFICATIONS

(V_{AA} = V_{DD} = 2.375 V–2.625 V, V_{DD_IO} = 2.375 V–3.600 V, V_{REF} = 1.235 V, R_{SET} = 760 Ω, R_{LOAD} = 150 Ω, T_{MIN} to T_{MAX} (0°C to 70°C), unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
STATIC PERFORMANCE[1]					
Resolution		12		Bits	
Integral Nonlinearity		±2.0		LSB	
Differential Nonlinearity, +ve[2]		0.25		LSB	V_{AA} = 2.5 V
Differential Nonlinearity, –ve[2]		2.0		LSB	V_{AA} = 2.5 V
DIGITAL OUTPUTS					
Output Low Voltage, V_{OL}			0.4 [0.4][3]	V	I_{SINK} = 3.2 mA
Output High Voltage, V_{OH}	2.4 [2.0][3]			V	I_{SOURCE} = 400 μA
Three-State Leakage Current		±1.0		μA	V_{IN} = 0.4 V, 2.4 V
Three-State Output Capacitance		2		pF	
DIGITAL AND CONTROL INPUTS					
Input High Voltage, V_{IH}	2			V	
Input Low Voltage, V_{IL}			0.8	V	
Input Leakage Current		1		μA	V_{IN} = 2.4 V
Input Capacitance, C_{IN}		2		pF	
ANALOG OUTPUTS					
Full-Scale Output Current	8.2	8.7	9.2	mA	
Output Current Range	8.2	8.7	9.2	mA	
Full-Scale Output Current	4.1	4.35	4.6	mA	$R_{SET1, 2}$ = 1520 Ω
Output Current Range	4.1	4.35	4.6	mA	$R_{SET1, 2}$ = 1520 Ω
DAC to DAC Matching		2.0		%	
Output Compliance Range, V_{OC}	0	1.0	1.4	V	
Output Capacitance, C_{OUT}		7		pF	
VOLTAGE REFERENCE					
Reference Range, V_{REF}	1.15	1.235	1.3	V	
POWER REQUIREMENTS					
Normal Power Mode					
I_{DD}[4]		93		mA	SD Only [8×]
		52		mA	PS Only [4×]
		84		mA	HDTV Only [2×]
		90	110	mA	SD and PS
		99		mA	SD [8×] and HDTV
		108		mA	SD and HDTV [2×]
I_{DD_IO}		0.2		mA	
I_{AA}[5,6]		70	75	mA	
Sleep Mode					
I_{DD}		130		μA	
I_{AA}		10		μA	
I_{DD_IO}		110		μA	
Power Supply Rejection Ratio		0.01		%/%	

NOTES

[1]Oversampling disabled. Static DAC performance will be improved with increased oversampling ratios.

[2]DNL measures the deviation of the actual DAC o/p voltage step from the ideal. For +ve DNL, the actual step value lies above the ideal step value; for –ve DNL, the actual step values lie below the ideal step value.

[3]Value in brackets for V_{DD_IO} = 2.375 V to 2.750 V.

[4]I_{DD} or the circuit current is the continuous current required to drive the digital core without the I_{PLL}.

[5]I_{AA} is the total current required to supply all DACs including the V_{REF} and PLL circuitry.

[6]All DACs on.

Specifications subject to change without notice.

ADV7300A/ADV7301A

DYNAMIC SPECIFICATIONS (V_{AA} = V_{DD} = 2.375 V–2.625 V, V_{DD_IO} = 2.375 V–3.600 V, V_{REF} = 1.235 V, R_{SET} = 760 Ω, R_{LOAD} = 150 Ω, T_{MIN} to T_{MAX} (0°C to 70°C), unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
PROGRESSIVE SCAN MODE					
Luma Bandwidth		12.5		MHz	
Chroma Bandwidth		5.8		MHz	
SNR		62		dB	Luma Ramp Unweighted
SNR		78		dB	Flat Field up to 5 MHz
SNR		72		dB	Flat Field Full Bandwidth
HDTV MODE					
Luma Bandwidth		30		MHz	
Chroma Bandwidth		13.75		MHz	
SNR		62		dB	Luma Ramp Unweighted
SNR		78		dB	Flat Field up to 5 MHz
SNR		72		dB	Flat Field Full Bandwidth
STANDARD DEFINITION MODE					
Hue Accuracy		0.2		Degrees	
Color Saturation Accuracy		0.5		%	
Chroma Nonlinear Gain		±0.4		%	Referenced to 40 IRE
Chroma Nonlinear Phase		±0.3		Degrees	
Chroma/Luma Intermodulation		±0.05		%	
Chroma/Luma Gain Inequality		±98		%	
Chroma/Luma Delay Inequality		0.9		ns	
Luminance Nonlinearity		±0.4		%	
Chroma AM Noise		84		dB	
Chroma PM Noise		74		dB	
Differential Gain		0.6		%	NTSC
Differential Phase		1.4		Degrees	NTSC
SNR		62		dB	Luma Ramp
SNR		78		dB	Flat Field up to 5 MHz
SNR		72		dB	Flat Field Full Bandwidth

Specifications subject to change without notice.

TIMING SPECIFICATIONS (V_{AA} = V_{DD} = 2.375 V–2.625 V, V_{DD_IO} = 2.375 V–3.600 V, V_{REF} = 1.235 V, R_{SET} = 760 Ω, R_{LOAD} = 150 Ω, T_{MIN} to T_{MAX} (0°C to 70°C), unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
MPU PORT[1]					
SCLOCK Frequency	0		400	kHz	
SCLOCK High Pulsewidth, t_1	0.6			µs	
SCLOCK Low Pulsewidth, t_2	1.3			µs	
Hold Time (Start Condition), t_3	0.6			µs	First Clock Generated after This Period
Setup Time (Start Condition), t_4	0.6			µs	Relevant for Repeated Start Condition
Data Setup Time, t_5	100			ns	
SDATA, SCLOCK Rise Time, t_6			300	ns	
SDATA, SCLOCK Fall Time, t_7			300	ns	
Setup Time (Stop Condition), t_8	0.6			µs	
$\overline{\text{RESET}}$ Low Time	100			ns	
ANALOG OUTPUTS					
Analog Output Delay[2]		8		ns	
Output Skew		1		ns	
CLOCK CONTROL AND PIXEL PORT[3]					
f_{CLK}			27	MHz	Progressive Scan Mode
f_{CLK}		81		MHz	HDTV Mode/Async Mode
Clock High Time, t_9	40			% 1 clkcycle	
Clock Low Time, t_{10}	40			% 1 clkcycle	
Data Setup Time, t_{11}	2.0			ns	
Data Hold Time, t_{12}	2.0			ns	
Output Access Time, t_{13}			14	ns	
Output Hold Time, t_{14}	4.0			ns	
Pipeline Delay		61		clkcycles	SD [2×]
		62.5		clkcycles	SD [8×]
		66.5		clkcycles	SD Component Filter [8×]
		33		clkcycles	PS [1×], HD [1×], Async Timing Mode
		43.5		clkcycles	PS [4×]
		36		clkcycles	HD [2×]

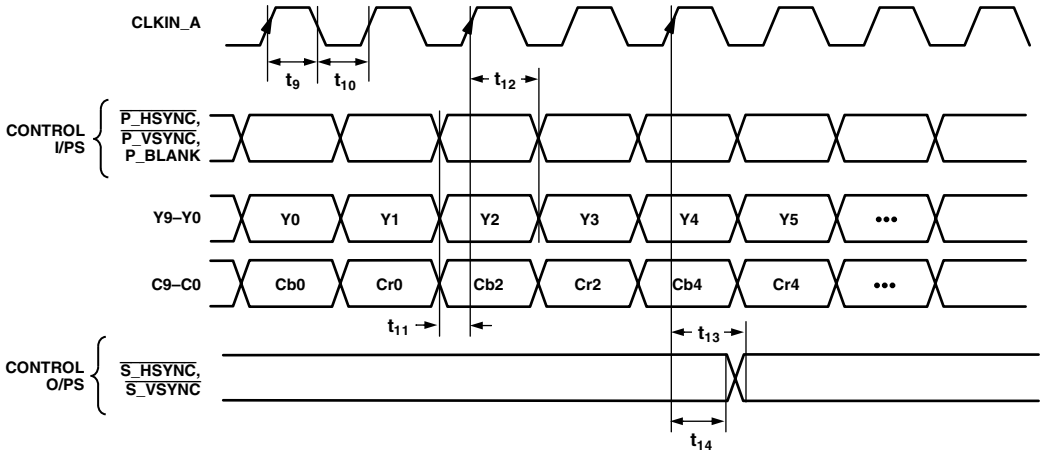
NOTES

[1]Guaranteed by characterization.

[2]Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of DAC output full-scale transition.

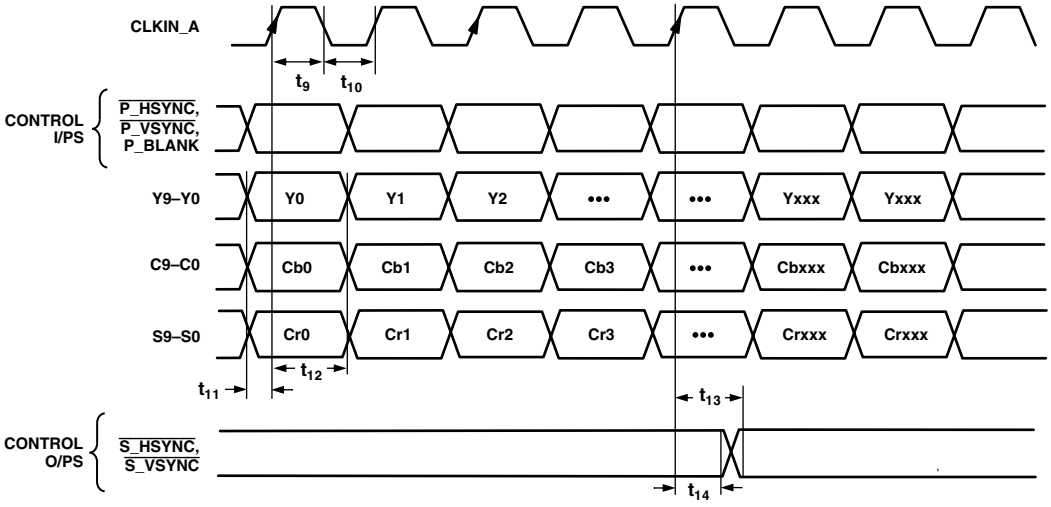
[3]Data: C[9:0]; S[9:0]; Y[9:0]
Control: $\overline{\text{P\_HSYNC}}$; $\overline{\text{P\_ VSYNC}}$; P_BLANK; $\overline{\text{S\_HSYNC}}$; $\overline{\text{S\_VSYNC}}$; $\overline{\text{S\_BLANK}}$

Specifications subject to change without notice.



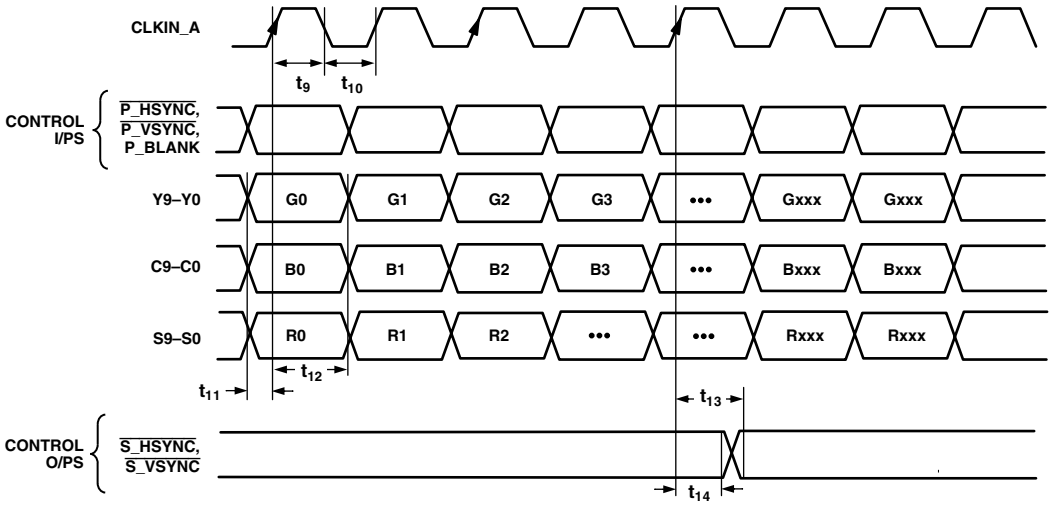
t_9 = CLOCK HIGH TIME, t_{10} = CLOCK LOW TIME, t_{11} = DATA SETUP TIME, t_{12} = DATA HOLD TIME

Figure 2. HD 4:2:2 Input Data Format Timing Diagram, Input Mode: PS Input Only, HDTV Input Only (Input Mode at Subaddress 01h = 001 or 010)



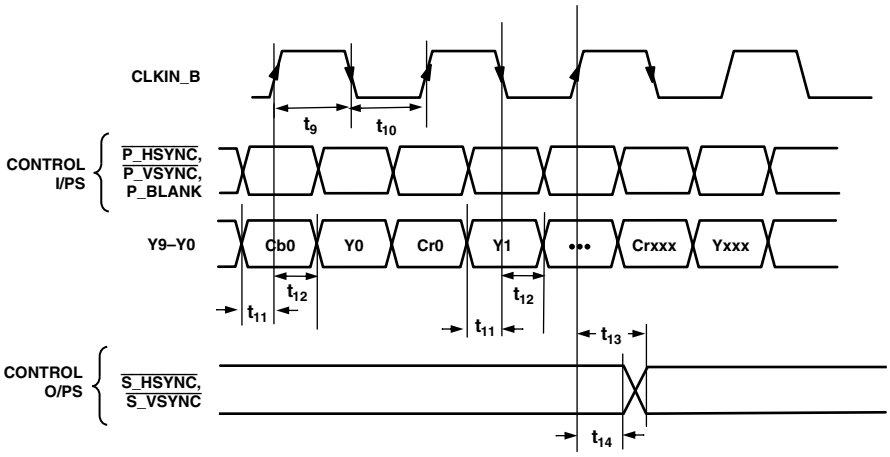
t_9 = CLOCK HIGH TIME, t_{10} = CLOCK LOW TIME, t_{11} = DATA SETUP TIME, t_{12} = DATA HOLD TIME

Figure 3. HD 4:4:4 YCrCb Input Data Format Timing Diagram, Input Mode: PS Input Only, HDTV Input Only (Input Mode at Subaddress 01h = 001 or 010)



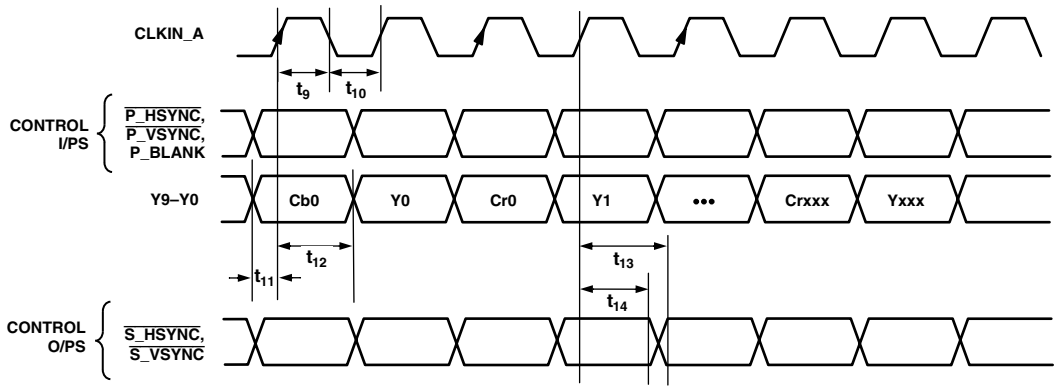
t_9 = CLOCK HIGH TIME, t_{10} = CLOCK LOW TIME, t_{11} = DATA SETUP TIME, t_{12} = DATA HOLD TIME

Figure 4. HD 4:4:4 RGB Input Data Format Timing Diagram, HD RGB Input Enabled (Input Mode at Subaddress 01h = 001 or 010)



t_9 = CLOCK HIGH TIME, t_{10} = CLOCK LOW TIME, t_{11} = DATA SETUP TIME, t_{12} = DATA HOLD TIME

Figure 5. PS 4:2:2 1 × 10-Bit Interleaved @ 27 MHz, Input Mode: PS Input Only (Input Mode at Subaddress 01h = 100)



t_9 = CLOCK HIGH TIME, t_{10} = CLOCK LOW TIME, t_{11} = DATA SETUP TIME, t_{12} = DATA HOLD TIME

Figure 6. PS 4:2:2 1 × 10-Bit Interleaved @ 54 MHz, Input Mode: PS 54 MHz Input (Input Mode at Subaddress 01h = 111)

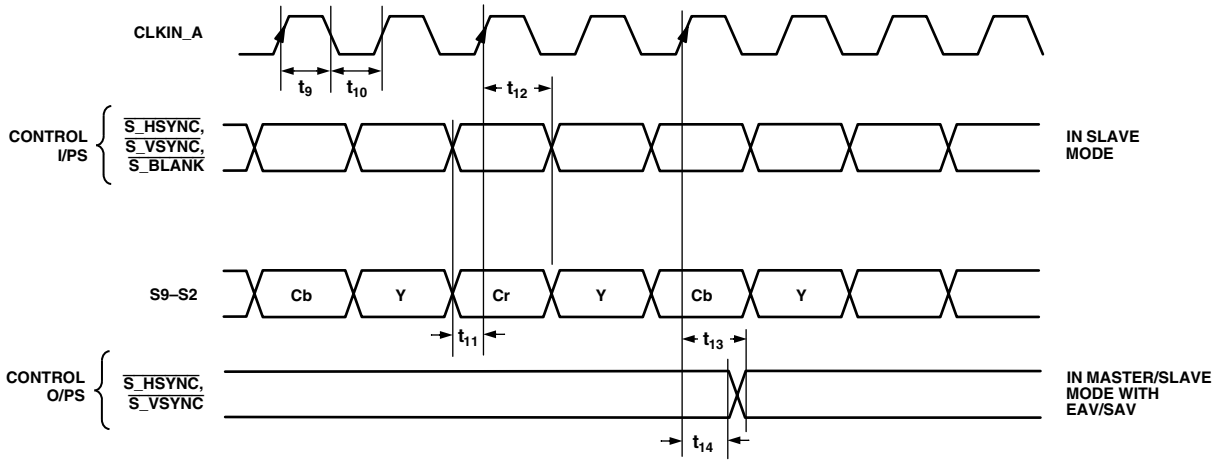


Figure 7. 8-Bit SD Pixel Input Timing Diagram, Input Mode: SD Input Only (Input Mode at Subaddress 01h = 000)

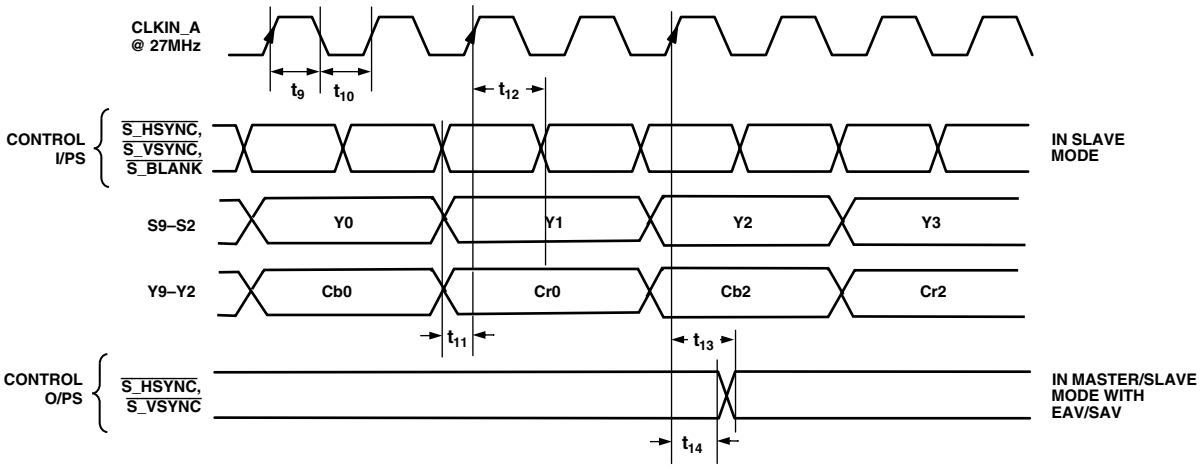


Figure 8. 16-Bit SD Pixel Input Timing Diagram, Input Mode: SD Input Only (Input Mode at Subaddress 01h = 000)

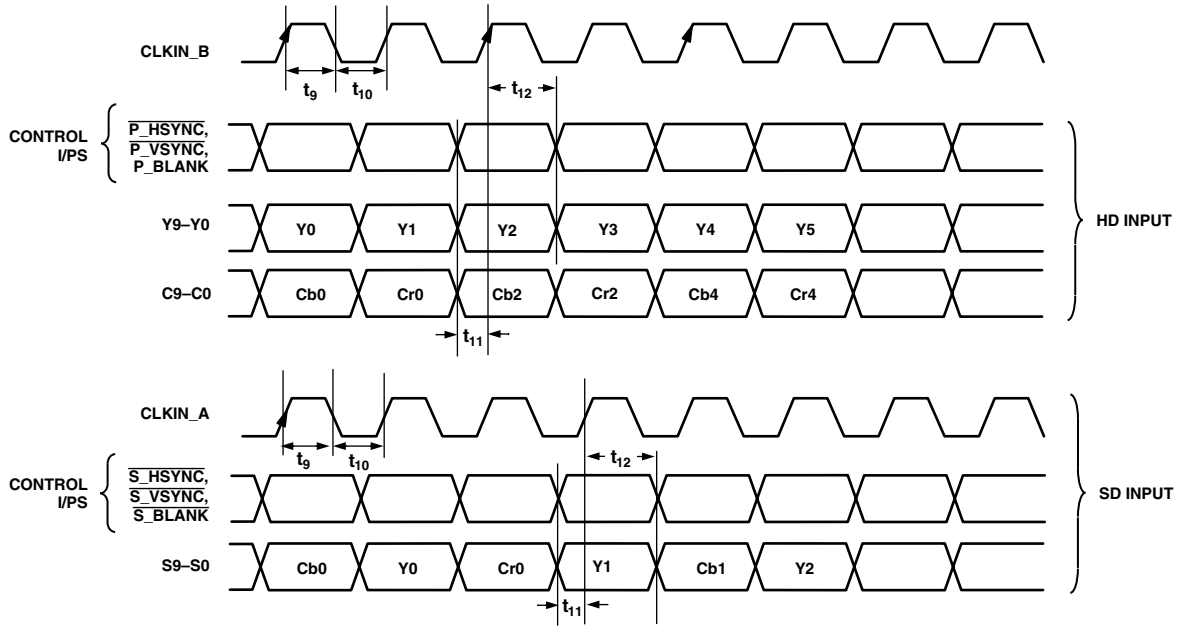


Figure 9. SD and HD Simultaneous Input, Input Mode: SD and PS 20-Bit or SD and HDTV (Input Mode at Subaddress 01h = 011, 101, or 110)

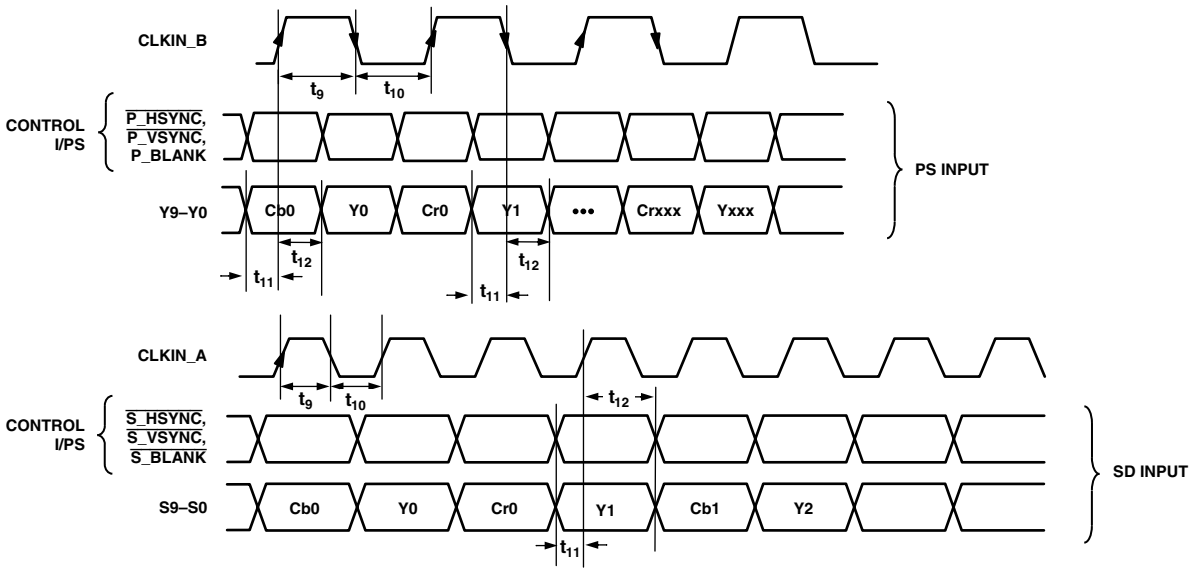


Figure 10. SD and HD Simultaneous Input, Input Mode: SD and PS 10-Bit (Input Mode at Subaddress 01h = 100)

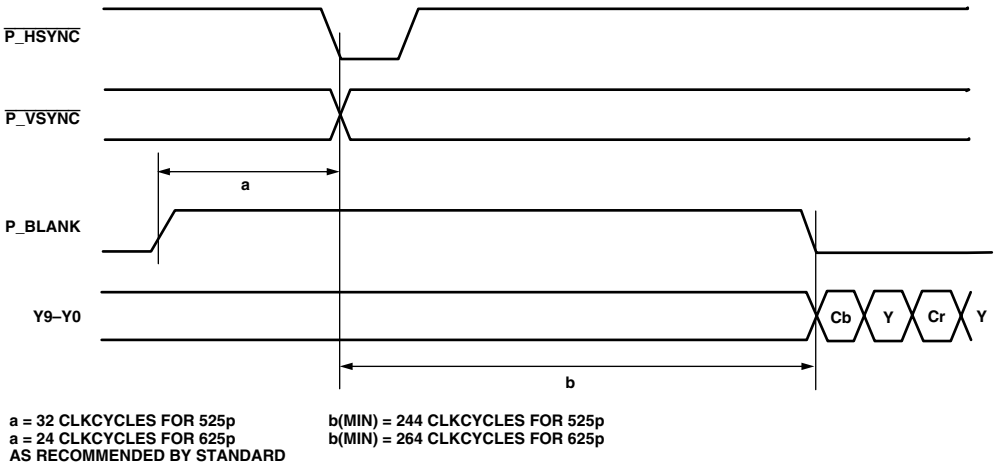
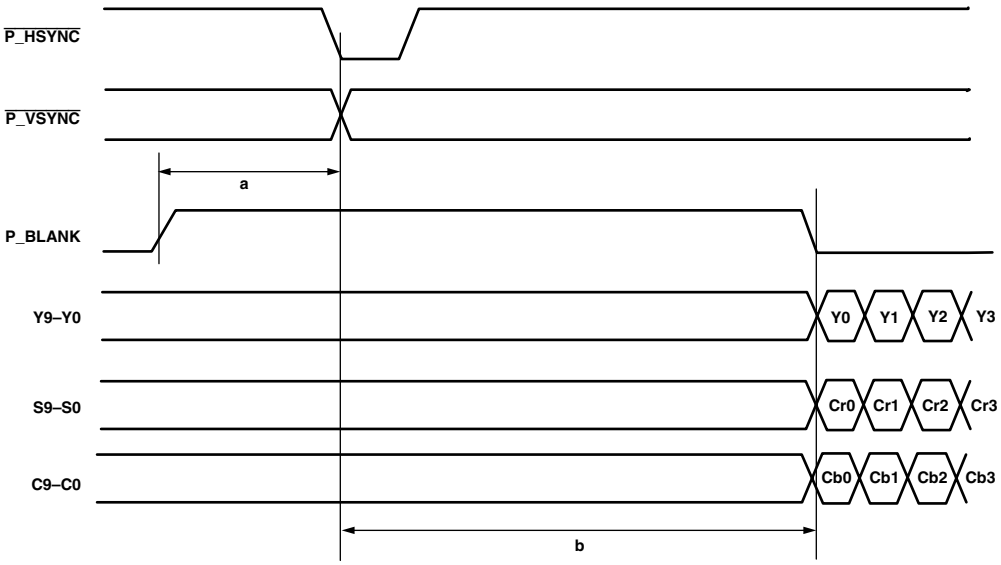


Figure 11. PS 4:2:2 1 × 10-Bit Interleaved @ 54 MHz Input Timing Diagram



a = 16 CLKCYCLES FOR 525p
a = 12 CLKCYCLES FOR 626p
a = 44 CLKCYCLES FOR 1080i
a = 70 CLKCYCLES FOR 720p
AS RECOMMENDED BY STANDARD

b(MIN) = 122 CLKCYCLES FOR 525p
b(MIN) = 132 CLKCYCLES FOR 625p
b(MIN) = 236 CLKCYCLES FOR 1080i
b(MIN) = 300 CLKCYCLES FOR 720p

Figure 12. HD Input Timing Diagram

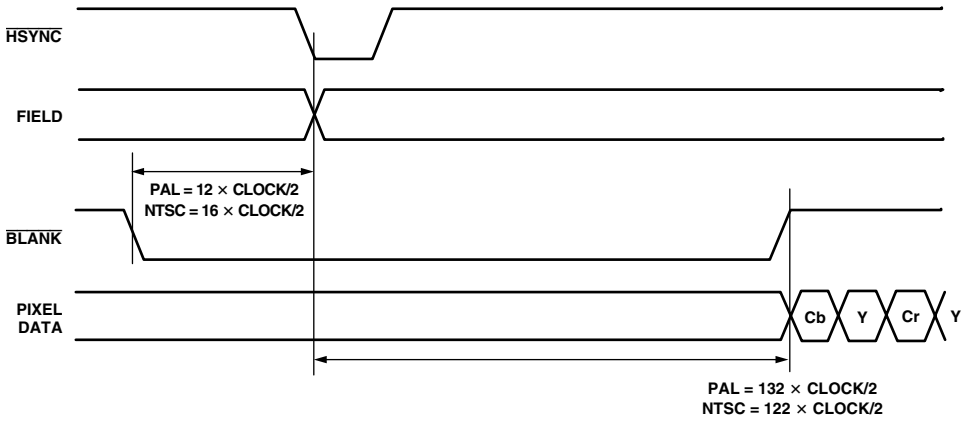


Figure 13. SD Timing Input for Timing Mode 1

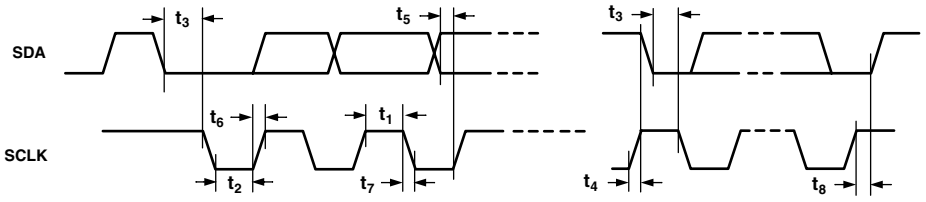


Figure 14. MPU Port Timing Diagram

ADV7300A/ADV7301A

ABSOLUTE MAXIMUM RATINGS*

V_{AA} to AGND . . . . . +3.0 V to –0.3 V
V_{DD} to GND . . . . . +3.0 V to –0.3 V
V_{DD_IO} to IO_GND . . . . . –0.3 to V_{DD_IO} to +0.3 V
Ambient Operating Temperature (T_A) . . . . . 0°C to +70°C
Storage Temperature (T_S) . . . . . –65°C to +150°C
Infrared Reflow Soldering (20 sec) . . . . . 260°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

T_{JC} = 11°C/W

T_{JA} = 47°C/W

The ADV7300A/ADV7301A is a lead-free environmentally friendly product. It is manufactured using the most up to date materials and processes. The coating on the leads of each device is 100% pure tin electroplate. The device is suitable for lead-free applications and is able to withstand surface-mount soldering up to 255°C (±5°C). In addition, it is backward compatible with conventional tin-lead soldering processes. This means that the electroplated tin coating can be soldered with tin-lead solder pastes at conventional reflow temperatures of 220°C to 235°C.

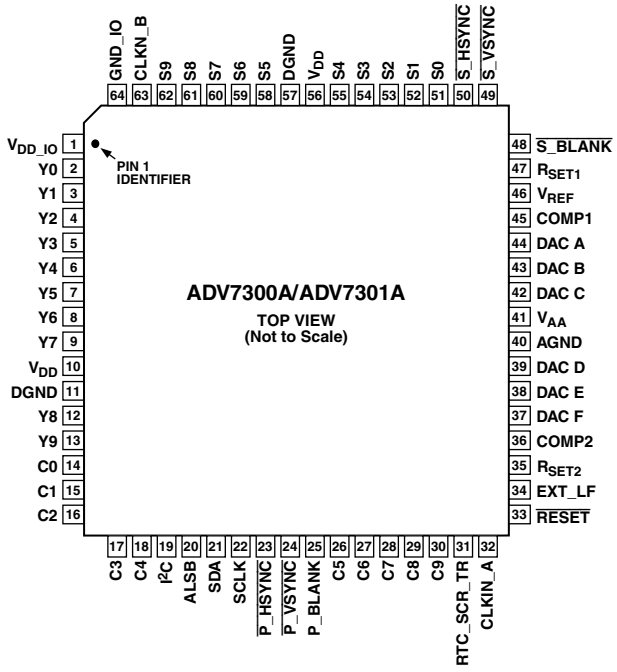
ORDERING GUIDE

Model	Package Description	Package Option
ADV7300AKST	Plastic Quad Flatpack	ST-64
ADV7301AKST	Plastic Quad Flatpack	ST-64

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7300A/ADV7301A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Input/Output	Function
1	V_{DD_IO}	P	Power Supply for Digital Inputs and Outputs
2–9, 12, 13	Y0–Y9	I	10-Bit Progressive Scan/HDTV Input Port for Y Data. The LSBs are set up on Pins Y0 and Y1. In Default Mode, the input on this port is output on DAC D.
10, 56	V_{DD}	P	Digital Power Supply
11, 57	DGND	G	Digital Ground

Pin No.	Mnemonic	Input/Output	Function
14–18, 26–30	C0–C9	I	10-Bit Progressive Scan/HDTV Input Port for CrCb color data in 4:2:2 Input Mode. In 4:4:4 Input Mode, this input port is used for the Cb (Blue/U) data. The LSBs are set up on Pins C0 and C1. In Default Mode, the input on this port is output on DAC E.
19	I^2C	I	This input pin must be tied high (V_{DD_IO}) for the ADV7300A/ADV7301A to interface over the I^2C port.
20	ALSB	I/O	TTL Address Input. This signal sets up the LSB of the MPU address. When this pin is tied low, the I^2C filter is activated, which reduces noise on the I^2C interface.
21	SDA	I/O	MPU Port Serial Data Input/Output
22	SCLK	I	MPU Port Serial Interface Clock Input
23	$\overline{\text{P\_HSYNC}}$	I	Video Horizontal Sync Control Signal for HD Sync in Simultaneous SD/HD Mode and HD Only Mode
24	$\overline{\text{P\_VSYNC}}$	I	Video Vertical Sync Control Signal for HD Sync in Simultaneous SD/HD Mode and HD Only Mode
25	P_BLANK	I	Video Blanking Control Signal for HD Sync in Simultaneous SD/HD Mode and HD Only Mode
31	RTC_SCR_TR	I	Multifunctional Input: Realtime Control (RTC) Input, Timing Reset Input, and Subcarrier Reset Input
32	CLKIN_A	I	Pixel Clock Input for HD Only or SD Only Modes
33	$\overline{\text{RESET}}$	I	This input resets the on-chip timing generator and sets the ADV7300A/ ADV7301A into default register setting. Reset is an active low signal.
34	EXT_LF	I	External Loop Filter for the internal PLL
35, 47	$R_{SET2, 1}$	I	A 760 Ω resistor must be connected from this pin to AGND and is used to control the amplitudes of the DAC outputs.
36, 45	COMP2, 1	O	Compensation Pin for DACs. Connect 0.1 μF capacitor from COMP pin to V_{AA}.
37	DAC F	O	In SD Only Mode: Chroma/Red/V Analog Output, in HD Only Mode and Simultaneous HD/SD: Pb/Blue (HD) Analog Output
38	DAC E	O	In SD Only Mode: Luma/Blue/U Analog Output, in HD Only Mode and Simultaneous HD/SD: Pr/Red (HD) Analog Output
39	DAC D	O	In SD Only Mode: CVBS/Green/Y Analog Output, in HD Only Mode and Simultaneous HD/SD: Y/Green (HD) Analog Output
40	AGND	G	Analog Ground
41	V_{AA}	P	Analog Power Supply
42	DAC C	O	Chroma/Red/V SD Analog Output
43	DAC B	O	Luma/Blue/U SD Analog Output
44	DAC A	O	CVBS/Green/Y SD Analog Output
46	V_{REF}	I/O	Optional External Voltage Reference Input for DACs or Voltage Reference Output (1.235 V)
48	$\overline{\text{S\_BLANK}}$	I/O	Video Blanking Control Signal for SD
49	$\overline{\text{S\_VSYNC}}$	I/O	Video Vertical Control Signal for SD. Option to output SD VSYNC or SD HSYNC in SD Slave Mode 0 and/or any HD Mode.
50	$\overline{\text{S\_HSYNC}}$	I/O	Video Horizontal Control Signal for SD. Option to output SD HSYNC or HD HSYNC in SD Slave Mode 0 and/or any HD Mode.
51–55, 58–62	S0–S9	I	10-Bit Standard Definition Input Port or Progressive Scan/HDTV Input Port for Cr (Red/V) color data in 4:4:4 Input Mode. The LSBs are set up on Pins S0 and S1. In Default Mode, the input on this port is output on DAC F.
63	CLKIN_B	I	Pixel Clock Input. Requires a 27 MHz reference clock for Progressive Scan Mode or a 74.25 MHz (74.1758 MHz) reference clock in HDTV Mode. This clock input pin is only used in Simultaneous SD/HD Mode.
64	GND_IO		Digital Ground

ADV7300A/ADV7301A

MPU PORT DESCRIPTION

The ADV7300A/ADV7301A supports a 2-wire serial (I^2C compatible) microprocessor bus driving multiple peripherals. Two inputs, serial data (SDA) and serial clock (SCLK), carry information between any device connected to the bus. Each slave device is recognized by a unique address. The ADV7300A/ADV7301A has four possible slave addresses for both read and write operations. These are unique addresses for each device and are illustrated in Figures 15 and 16. The LSB sets either a read or write operation. Logic Level "1" corresponds to a read operation, while Logic Level "0" corresponds to a write operation. A1 is set by setting the ALSB pin of the ADV7300A/ADV7301A to Logic Level "0" or Logic Level "1." When ALSB is set to "1," there is greater input bandwidth on the I^2C lines, which allows high speed data transfers on this bus. When ALSB is set to "0," there is reduced input bandwidth on the I^2C lines, which means that pulses of less than 50 ns will not pass into the I^2C internal controller. This mode is recommended for noisy systems.

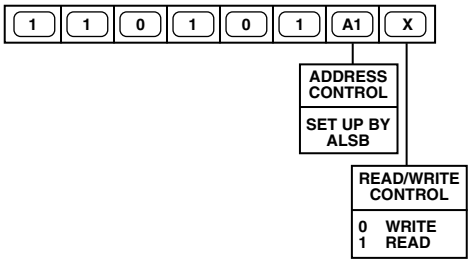


Figure 15. ADV7300A Slave Address = D4h

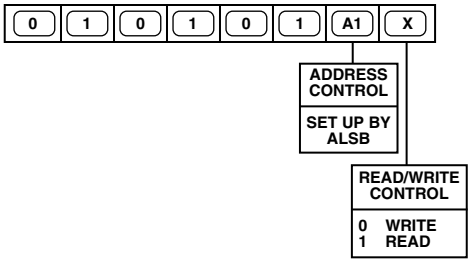


Figure 16. ADV7301A Slave Address = 54h

To control the various devices on the bus, the following protocol must be followed. First, the master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA, while SCLK remains high. This indicates that an address/data stream will follow. All peripherals respond to the start condition and shift the next 8 bits (7-bit address + R/$\overline{W}$ Bit). The bits are transferred from MSB down to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an Acknowledge Bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDA and SCLK lines waiting for the start condition and the correct transmitted address. The R/$\overline{W}$ Bit determines the direction of the data.

A Logic "0" on the LSB of the first byte means that the master will write information to the peripheral. A Logic "1" on the LSB of the first byte means that the master will read information from the peripheral.

The ADV7300A/ADV7301A acts as a standard slave device on the bus. The data on the SDA pin is eight bits long, supporting the 7-bit addresses plus the R/$\overline{W}$ Bit. It interprets the first byte as the device address and the second byte as the starting subaddress. The subaddresses autoincrement allows data to be written to or read from the starting subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without having to update all the registers.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, it will cause an immediate jump to the idle condition. During a given SCLK high period, the user should issue only one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADV7300A/ADV7301A will not issue an acknowledge and will return to the idle condition. If in Autoincrement Mode the user exceeds the highest subaddress, the following action will be taken:

1. In Read Mode, the highest subaddress register contents will continue to be output until the master device issues a no-acknowledge. This indicates the end of a read. A no-acknowledge condition is where the SDA line is not pulled low on the ninth pulse.
2. In Write Mode, the data for the invalid byte will not be loaded into any subaddress register, a no-acknowledge will be issued by the ADV7300A/ADV7301A, and the part will return to the idle condition.

Before writing to the subcarrier frequency registers, it is a requirement that the ADV7300A/ADV7301A has been reset at least once since power-up.

The four subcarrier frequency registers must be updated starting with subcarrier frequency register 0. The subcarrier frequency will not update until the last subcarrier frequency register byte has been received by the ADV7300A/ADV7301A.

Figure 17 illustrates an example of data transfer for a read sequence and the start and stop conditions.

Figure 18 shows bus write and read sequences.

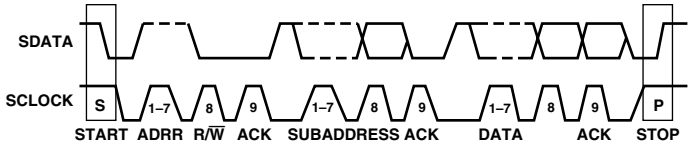


Figure 17. Bus Data Transfer

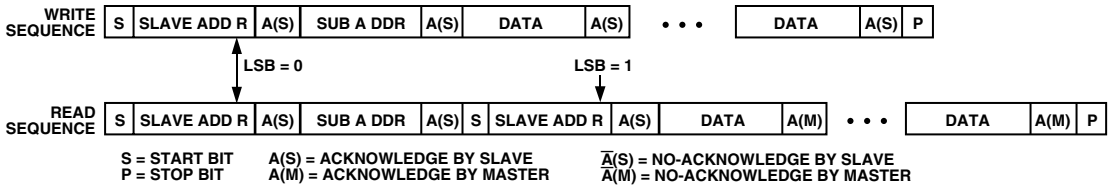


Figure 18. Read and Write Sequence

REGISTER ACCESSES

The MPU can write to or read from all of the registers of the ADV7300A/ADV7301A except the subaddress registers that are write-only registers. The subaddress register determines which register the next read or write operation accesses. All communications with the part through the bus start with an access to the subaddress register. Then a read/write operation is performed from/to the target address which then increments to the next address until a stop command on the bus is performed.

REGISTER PROGRAMMING

The following section describes the functionality of each register. All registers can be read from as well as written to unless otherwise stated.

Subaddress Register (SR7–SR0)

The Communications Register is an 8-bit write-only register. After the part has been accessed over the bus and a read/write operation is selected, the subaddress is set up. The Subaddress Register determines to/from which register the operation takes place.

Register Select (SR7–SR0)

These bits are set up to point to the required starting address.

Table I. Power Mode Register

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
00h	Power Mode Register	Sleep Mode[1]								0	Sleep Mode Off	$F_{C}h$
										1	Sleep Mode On	
		PLL and Oversampling Control[2]							0		PLL On	
									1		PLL Off	
		DAC F: Power On/Off						0			DAC F Off	
								1			DAC F On	
		DAC E: Power On/Off					0				DAC E Off	
							1				DAC E On	
		DAC D: Power On/Off				0					DAC D Off	
						1					DAC D On	
		DAC C: Power On/Off			0						DAC C Off	
					1						DAC C On	
		DAC B: Power On/Off		0							DAC B Off	
				1							DAC B On	
		DAC A: Power On/Off	0								DAC A Off	
			1								DAC A On	

NOTES
[1]When enabled, the current consumption is reduced to μA level. All DACs and the internal PLL circuit are disabled. I^2C registers can be read from and written to.
[2]This control allows the internal PLL circuit to be powered down and the oversampling to be switched off.

Table II. Input Mode Register

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
01h	Input Mode Register	BTA T-1004 Compatibility								0	Disabled	38h
										1	Enabled	
		Reserved							0		Zero must be written to this bit.	
		Pixel Align						0			Video input data starts with a Y0 bit. Only for PS Interleaved Mode.	
								1			Video input data starts with a Cb0 bit.	
		Clock Align					0					
							1				Must be set if the phase delay between the two input clocks is <9.25 ns or >27.75 ns. Only if two input clocks are used.	
		Input Mode		0	0	0					SD Input Only	
				0	0	1					PS Input Only	
				0	1	0					HDTV Input Only	
				0	1	1					SD and PS (20-Bit)	
				1	0	0					SD and PS (10-Bit)	
				1	0	1					SD and HDTV (SD Oversampled)	
				1	1	0					SD and HDTV (HDTV Oversampled)	
				1	1	1					PS 54 MHz Input	
		Reserved	0								Zero must be written to this bit.	

Table III. Mode Register

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
02h	Mode Register 0	Reserved							0	0	Zero must be written to these bits.	20h
		Test Pattern Black Bar						0			Disabled	
								1			Enabled. 0x11h, Bit 2 must also be enabled.	
		RGB Matrix					0				Disable Programmable RGB Matrix	
							1				Enable Programmable RGB Matrix	
		SYNC on RGB				0					No SYNC	
						1					SYNC on all RGB Outputs	
		RGB/YUV Output			0						RGB Component Outputs	
					1						YUV Component Outputs	
		SD SYNC		0							No SYNC Output	
				1							Output SD SYNCs on $\overline{S\_HSYNC}$ and $\overline{S\_VSYNC}$	
		HD SYNC	0								No SYNC Output	
			1								Output HD SYNCs on $\overline{S\_HSYNC}$ and $\overline{S\_VSYNC}$	
03h	RGB Matrix 0								X	X	LSB for GY	03h
04h	RGB Matrix 1								X	X	LSB for RV	F0h
							X	X			LSB for BU	
					X	X					LSB for GV	
			X	X							LSB for GU	
05h	RGB Matrix 2		X	X	X	X	X	X	X	X	Bits 9–2 for GY	4Eh
06h	RGB Matrix 3		X	X	X	X	X	X	X	X	Bits 9–2 for GU	0Eh
07h	RGB Matrix 4		X	X	X	X	X	X	X	X	Bits 9–2 for GV	24h
08h	RGB Matrix 5		X	X	X	X	X	X	X	X	Bits 9–2 for BU	92h
09h	RGB Matrix 6		X	X	X	X	X	X	X	X	Bits 9–2 for RV	7Ch
0Ah		Reserved										00h
0Bh		Reserved										00h
0Ch		Reserved										00h
0Dh		Reserved										00h
0Eh		Reserved										00h
0Fh		Reserved										00h

Table IV. HD Mode Register

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
10h	HD Mode Register 1	HD Output Standard							0	0	EIA770.2 Output	00h
									0	1	EIA770.1 Output	
									1	0	Ouptut Levels for Full Input Range	
									1	1	Reserved	
		HD Input Control Signals					0	0			HSYNC, VSYNC, BLANK	
							0	1			EAV/SAV Codes [1]	
							1	0			Async Timing Mode	
							1	1			Reserved	
		HD 625 p				0					525 p	
						1					625 p	
		HD 720 p			0						1080 i	
					1						720 p	
		HD BLANK Polarity		0							BLANK Active High	
				1							BLANK Active Low	
		HD Macrovision for 525 p/625 p	0								Macrovision Off	
			1								Macrovision On	
11h	HD Mode Register 2	HD Pixel Data Valid								0	Pixel Data Valid Off	00h
										1	Pixel Data Valid On	
									0		Reserved	
		HD Test Pattern Enable						0			HD Test Pattern Off	
								1			HD Test Pattern On	
		HD Test Pattern Hatch/Field					0				Hatch	
							1				Field/Frame	
		HD VBI Open				0					Disabled	
						1					Enabled	
		HD Undershoot Limiter		0	0						Disabled	
				0	1						–11 IRE	
				1	0						–6 IRE	
				1	1						–1.5 IRE	
		HD Sharpness Filter	0								Disabled	
			1								Enabled	
12h	HD Mode Register 3	HDY Delay wrt Falling Edge of HSYNC						0	0	0	0 Clock Cycle	
								0	0	1	1 Clock Cycle	
								0	1	0	2 Clock Cycle	
								0	1	1	3 Clock Cycle	
								1	0	0	4 Clock Cycle	
		HD Color Delay wrt Falling Edge of HSYNC			0	0	0				0 Clock Cycle	
					0	0	1				1 Clock Cycle	
					0	1	0				2 Clock Cycle	
					0	1	1				3 Clock Cycle	
					1	0	0				4 Clock Cycle	
		HD CGMS		0							Disabled	
				1							Enabled	
		HD CGMS CRC	0								Disabled	
			1								Enabled	

Table IV. HD Mode Register (continued)

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
13h	HD Mode Register 4	HD Cr/Cb Sequence[2]								0	Cb after Falling Edge of $\overline{\text{HSYNC}}$	4Ch
										1	Cr after Falling Edge of $\overline{\text{HSYNC}}$	
									0		Reserved	
		HD Input Format						0			8-Bit Input	
								1			10-Bit Input	
		Sync Filter on DAC D, E, F					0				Disabled	
							1				Enabled	
						0					Reserved	
		HD Chroma SSAF[2]			0						Disabled	
					1						Enabled	
		HD Chroma Input		0							4:4:4	
				1							4:2:2	
		HD Double Buffering	0								Disabled	
			1								Enabled	
14h	HD Mode Register 5		0	0	0	0	0	0	0	X	A low-high-low transition resets the internal HD timing counters.	00h
15h	HD Mode Register 6	Reserved								0	Zero must be written to this bit.	00h
		HD RGB Input							0		Disabled	
									1		Enabled	
		HD Sync on PrPb						0			Disabled	
								1			Enabled	
		HD Color DAC Swap [3]					0				DAC E = Pr, DAC F = Pb	
							1				DAC F = Pr, DAC E = Pb	
		HD Gamma Curve A/B				0					Gamma Curve A	
						1					Gamma Curve B	
		HD Gamma Curve Enable			0						Disabled	
					1						Enabled	
		HD Adaptive Filter Mode		0							Mode A	
				1							Mode B	
		HD Adaptive Filter Enable	0								Disabled	
			1								Enabled	

NOTES
[1]EAV/SAV codes are not supported for PS 1 × 10-Bit Interleaved Mode at 54 MHz.
[2]4:2:2 Input Format Only
[3]4:4:4 Input Format Only

Table V. Register Settings

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
16h	HD Y Color		X	X	X	X	X	X	X	X	Y Color Value	A0h
17h	HD Cr Color		X	X	X	X	X	X	X	X	Cr Color Value	80h
18h	HD Cb Color		X	X	X	X	X	X	X	X	Cb Color Value	80h
19h		Reserved										00h
1Ah		Reserved										00h
1Bh		Reserved										00h
1Ch		Reserved										00h
1Dh		Reserved										00h
1Eh		Reserved										00h
1Fh		Reserved										00h
20h	HD Sharpness Filter Gain	HD Sharpness Filter Gain Value A					0	0	0	0	Gain A = 0	00h
							0	0	0	1	Gain A = +1	
							…	…	…	…	…	
							0	1	1	1	Gain A = +7	
							1	0	0	0	Gain A = –8	
							…	…	…	…	…	
							1	1	1	1	Gain A = –1	
		HD Sharpness Filter Gain Value B	0	0	0	0					Gain B = 0	
			0	0	0	1					Gain B = +1	
			…	…	…	…					…	
			0	1	1	1					Gain B = +7	
			1	0	0	0					Gain B = –8	
			…	…	…	…					…	
			1	1	1	1					Gain B = –1	
21h	HD CGMS Data 0	HD CGMS Data Bits	0	0	0	0	C19	C18	C17	C16	CGMS 19–16	00h
22h	HD CGMS Data 1	HD CGMS Data Bits	C15	C14	C13	C12	C11	C10	C9	C8	CGMS 15–8	00h
23h	HD CGMS Data 2	HD CGMS Data Bits	C7	C6	C5	C4	C3	C2	C1	C0	CGMS 7–0	00h
24h	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A0	00h
25h	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A1	00h
26h	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A2	00h
27h	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A3	00h
28h	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A4	00h
29h	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A5	00h
2Ah	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A6	00h
2Bh	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A7	00h
2Ch	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A8	00h
2Dh	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A9	00h
2Eh	HD Gamma B	HD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B0	00h
2Fh	HD Gamma B	HD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B1	00h
30h	HD Gamma B	HD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B2	00h
31h	HD Gamma B	HD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B3	00h
32h	HD Gamma B	HD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B4	00h
33h	HD Gamma B	HD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B5	00h
34h	HD Gamma B	HD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B6	00h

Table VI. HD Adaptive Filters

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
38h	HD Adaptive Filter Gain 1	HD Adaptive Filter Gain 1 Value A					0	0	0	0	Gain A = 0	00hex
							0	0	0	1	Gain A = +1	
							0	1	1	1	Gain A = +7	
							1	0	0	0	Gain A = –8	
							1	1	1	1	Gain A = –1	
		HD Adaptive Filter Gain 1 Value B	0	0	0	0					Gain B = 0	
			0	0	0	1					Gain B = +1	
			0	1	1	1					Gain B = +7	
			1	0	0	0					Gain B = –8	
			1	1	1	1					Gain B = –1	
39h	HD Adaptive Filter Gain 2	HD Adaptive Filter Gain 2 Value A					0	0	0	0	Gain A = 0	00hex
							0	0	0	1	Gain A = +1	
							0	1	1	1	Gain A = +7	
							1	0	0	0	Gain A = –8	
							1	1	1	1	Gain A = –1	
		HD Adaptive Filter Gain 2 Value B	0	0	0	0					Gain B = 0	
			0	0	0	1					Gain B = +1	
			0	1	1	1					Gain B = +7	
			1	0	0	0					Gain B = –8	
			1	1	1	1					Gain B = –1	
3Ah	HD Adaptive Filter Gain 3	HD Adaptive Filter Gain 3 Value A					0	0	0	0	Gain A = 0	00hex
							0	0	0	1	Gain A = +1	
							0	1	1	1	Gain A = +7	
							1	0	0	0	Gain A = –8	
							1	1	1	1	Gain A = –1	
		HD Adaptive Filter Gain 3 Value B	0	0	0	0					Gain B = 0	
			0	0	0	1					Gain B = +1	
			0	1	1	1					Gain B = +7	
			1	0	0	0					Gain B = –8	
			1	1	1	1					Gain B = –1	
3Bh	HD Adaptive Filter Threshold A	HD Adaptive Filter Threshold A Value	X	X	X	X	X	X	X	X	Threshold A	00hex
3Ch	HD Adaptive Filter Threshold B	HD Adaptive Filter Threshold B Value	X	X	X	X	X	X	X	X	Threshold B	00hex
3Dh	HD Adaptive Filter Threshold C	HD Adaptive Filter Threshold C Value	X	X	X	X	X	X	X	X	Threshold C	00hex

Table VII. SD Mode Registers

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
3Eh		Reserved										00h
3Fh		Reserved										00h
40h	SD Mode Register 0	SD Standard							0	0	NTSC	00h
									0	1	PAL B, D, G, H, I	
									1	0	PAL M	
									1	1	PAL N	
		SD Luma Filter				0	0	0			LPF NTSC	
						0	0	1			LPF PAL	
						0	1	0			Notch NTSC	
						0	1	1			Notch PAL	
						1	0	0			SSAF Luma	
						1	0	1			Luma CIF	
						1	1	0			Luma QCIF	
						1	1	1			Reserved	
		SD Chroma Filter	0	0	0						1.3 MHz	
			0	0	1						0.65 MHz	
			0	1	0						1.0 MHz	
			0	1	1						2.0 MHz	
			1	0	0						Reserved	
			1	0	0						Chroma CIF	
			1	1	0						Chroma QCIF	
			1	1	1						3.0 MHz	
41h		Reserved										00h
42h	SD Mode Register 1	SD UV SSAF								0	Disabled	08h
										1	Enabled	
		SD DAC Output 1*							0		DAC A, B, C: CVBS, L, C; DAC D, E, F: GBR or YUV	
									1		DAC A, B, C: GBR or YUV; DAC D, E, F: CVBS, L, C	
		SD DAC Output 2						0			Swap DAC A and DAC D Outputs	
								1				
		SD Pedestal					0				Disabled	
							1				Enabled	
		SD Square Pixel				0					Disabled	
						1					Enabled	
		SD VCR FF/RW Sync			0						Disabled	
					1						Enabled	
		SD Pixel Data Valid		0							Disabled	
				1							Enabled	
		SD Active Video Edge	0								Disabled	
			1								Enabled	

Table VII. SD Mode Registers (continued)

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
43h	SD Mode Register 2	SD Pedestal YUV Output								0	No Pedestal on YUV	00h
										1	7.5 IRE Pedestal on YUV	
		SD Output Levels Y							0		Y = 700 mV/300 mV	
									1		Y = 714 mV/286 mV	
		SD Output Levels UV					0	0			700 mV p-p [PAL]; 1000 mV p-p [NTSC]	
							0	1			700 mV p-p	
							1	0			1000 mV p-p	
							1	1			648 mV p-p	
		SD VBI Open				0					Disabled	
						1					Enabled	
		SD CC Field Control		0	0						CC Disabled	
				0	1						CC on Odd Field Only	
				1	0						CC on Even Field Only	
				1	1						CC on Both Fields	
			1								Reserved	
44h	SD Mode Register 3	SD VSYNC-3H								0	Disabled	00h
										1	VSYNC = 2.5 lines [PAL]; VSYNC = 3 lines [NTSC]	
		SD RTC/TR/SCR						0	0		Genlock Disabled	
								0	1		Subcarrier Reset	
								1	0		Timing Reset	
								1	1		RTC Enabled	
		SD Active Video Length					0				720 Pixels	
							1				710 (NTSC); 702(PAL)	
		SD Chroma				0					Chroma Enabled	
						1					Chroma Disabled	
		SD Burst			0						Enabled	
					1						Disabled	
		SD Color Bars		0							Disabled	
				1							Enabled	
		Reserved	0								Zero must be written to this bit.	
45h	Reserved											00h
46h	Reserved											00h
47h	SD Mode Register 4	SD UV Scale								0	Disabled	00h
										1	Enabled	
		SD Y Scale							0		Disabled	
									1		Enabled	
		SD Hue Adjust						0			Disabled	
								1			Enabled	
		SD Brightness					0				Disabled	
							1				Enabled	
		SD Luma SSAF Gain				0					Disabled	
						1					Enabled	
		Reserved			0						Zero must be written to this bit.	
		Reserved		0							Zero must be written to this bit.	
		Reserved	0								Zero must be written to this bit.	

Table VII. SD Mode Registers (continued)

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
48h	SD Mode Register 5	Reserved								0	Zero must be written to this bit.	
		Reserved							0		Zero must be written to this bit.	00h
		SD Double Buffering						0			Disabled	
								1			Enabled	
		SD Input Format				0	0				8-Bit Input	
						0	1				16-Bit Input	
						1	0				10-Bit Input	
						1	1				20-Bit Input	
		SD Digital Noise Reduction			0						Disabled	
					1						Enabled	
		SD Gamma Control		0							Disabled	
				1							Enabled	
		SD Gamma Curve	0								Gamma Curve A	
			1								Gamma Curve B	
49h	SD Mode Register 6	SD Undershoot Limiter							0	0	Disabled	00h
									0	1	–11 IRE	
									1	0	–6 IRE	
									1	1	–1.5 IRE	
		SD Black Burst Output on DAC Y						0			Disabled	
								1			Enabled	
		SD Black Burst Output on DAC Luma					0				Disabled	
							1				Enabled	
		SD Chroma Delay			0	0					Disabled	
					0	1					4 Clock Cycles	
					1	0					8 Clock Cycles	
					1	1					Reserved	
		Reserved		0							Zero must be written to this bit.	
		Reserved	0								Zero must be written to this bit.	

*For more detail, see Input and Output Configuration section.

Table VIII. SD Registers

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
4Ah	SD Timing Register 0	SD Slave/Master Mode								0	Slave Mode	08h
										1	Master Mode	
		SD Timing Mode						0	0		Mode 0	
								0	1		Mode 1	
								1	0		Mode 2	
								1	1		Mode 3	
		SD BLANK Input					0				Enabled	
							1				Disabled	
		SD Luma Delay			0	0					No Delay	
					0	1					2 Clock Cycles	
					1	0					4 Clock Cycles	
					1	1					6 Clock Cycles	
		SD Min. Luma Value		0							–40 IRE	
				1							–7.5 IRE	
		SD Timing Reset	X	0	0	0	0	0	0	0	A low-high-low transistion will reset the internal SD timing counters.	
4Bh	SD Timing Register 1	SD $\overline{\text{HSYNC}}$ Width							0	0	Ta = 1 Clock Cycle	00h
									0	1	Ta = 4 Clock Cycles	
									1	0	Ta = 16 Clock Cycles	
									1	1	Ta = 128 Clock Cycles	
		SD $\overline{\text{HSYNC}}$ to $\overline{\text{VSYNC}}$ Delay					0	0			Tb = 0 Clock Cycle	
							0	1			Tb = 4 Clock Cycles	
							1	0			Tb = 8 Clock Cycles	
							1	1			Tb = 18 Clock Cycles	
		SD $\overline{\text{HSYNC}}$ to $\overline{\text{VSYNC}}$ Rising Edge Delay (Mode 1 Only); VSYNC Width (Mode 2 Only)			X	0					Tc = Tb	
					X	1					Tc = Tb + 32 µs	
					0	0					1 Clock Cycle	
					0	1					4 Clock Cycles	
					1	0					16 Clock Cycles	
					1	1					128 Clock Cycles	
		$\overline{\text{HSYNC}}$ to Pixel Data Adjust	0	0							0 Clock Cycle	
			0	1							1 Clock Cycle	
			1	0							2 Clock Cycles	
			1	1							3 Clock Cycles	
4Ch	SD F_{SC} Register 0		X	X	X	X	X	X	X	X	Subcarrier Frequency Bits 7–0	16h
4Dh	SD F_{SC} Register 1		X	X	X	X	X	X	X	X	Subcarrier Frequency Bits 15–8	7Ch
4Eh	SD F_{SC} Register 2		X	X	X	X	X	X	X	X	Subcarrier Frequency Bits 23–16	F0h
4Fh	SD F_{SC} Register 3		X	X	X	X	X	X	X	X	Subcarrier Frequency Bits 31–24	21h
50h	SD F_{SC} Phase		X	X	X	X	X	X	X	X	Subcarrier Phase Bits 9–2	00h
51h	SD Closed Captioning	Extended Data on Even Fields	X	X	X	X	X	X	X	X	Extended Data Bits 7–0	00h
52h	SD Closed Captioning	Extended Data on Even Fields	X	X	X	X	X	X	X	X	Extended Data Bits 15–8	00h
53h	SD Closed Captioning	Data on Odd Fields	X	X	X	X	X	X	X	X	Data Bits 7–0	00h
54h	SD Closed Captioning	Data on Odd Fields	X	X	X	X	X	X	X	X	Data Bits 15–8	00h
55h	SD Pedestal Register 0	Pedestal on Odd Fields	17	16	15	14	13	12	11	10	Setting any of these bits to 1 will disable pedestal on the line number indicated by the bit settings.	00h
56h	SD Pedestal Register 1	Pedestal on Odd Fields	25	24	23	22	21	20	19	18		00h
57h	SD Pedestal Register 2	Pedestal on Even Fields	17	16	15	14	13	12	11	10		00h
58h	SD Pedestal Register 3	Pedestal on Even Fields	25	24	23	22	21	20	19	18		00h

Table VIII. SD Registers (continued)

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
59h	SD CGMS/WSS 0	SD CGMS Data					19	18	17	16	CGMS Data Bits C19–C16	00h
		SD CGMS CRC				0					Disabled	
						1					Enabled	
		SD CGMS on Odd Fields			0						Disabled	
					1						Enabled	
		SD CGMS on Even Fields		0							Disabled	
				1							Enabled	
		SD WSS	0								Disabled	
			1								Enabled	
5Ah	SD CGMS/WSS 1	SD CGMS/WSS Data			13	12	11	10	9	8	CGMS Data Bits C13–C8 or WSS Data Bits C13–C8	00h
			15	14							CGMS Data Bits C15–C14	
5Bh	SD CGMS/WSS 2	SD CGMS/WSS Data	7	6	5	4	3	2	1	0	CGMS/WSS Data Bits C7–C0	00h
5Ch	SD LSB Register	SD LSB for Y Scale Value							X	X	SD Y Scale Bits 1–0	
		SD LSB for U Scale Value					X	X			SD U Scale Bits 1–0	
		SD LSB for V Scale Value			X	X					SD V Scale Bits 1–0	
		SD LSB for F_{SC} Phase	X	X							Subcarrier Phase Bits 1–0	
5Dh	SD Y Scale Register	SD Y Scale Value	X	X	X	X	X	X	X	X	SD Y Scale Bits 7–2	00h
5Eh	SD V Scale Register	SD V Scale Value	X	X	X	X	X	X	X	X	SD V Scale Bits 7–2	00h
5Fh	SD U Scale Register	SD U Scale Value	X	X	X	X	X	X	X	X	SD U Scale Bits 7–2	00h
60h	SD Hue Register	SD Hue Adjust Value	X	X	X	X	X	X	X	X	SD Hue Adjust Bits 7–0	00h
61h	SD Brightness/WSS	SD Brightness Value		X	X	X	X	X	X	X	SD Brightness Bits 6–0	00h
		SD Blank WSS Data*	0								Disabled	
			1								Enabled	
62h	SD Luma SSAF	SD Luma SSAF Gain/Attenuation	0	0	0	0	0	0	0	0	–4 dB	00h
			0	0	0	0	0	1	1	0	0 dB	
			0	0	0	0	1	1	0	0	+4 dB	
63h	SD DNR 0	Coring Gain Border					0	0	0	0	No Gain	00h
							0	0	0	1	+1/16 (–1/8 in DNR Mode)	
							0	0	1	0	+2/16 (–2/8 in DNR Mode)	
							0	0	1	1	+3/16 (–3/8 in DNR Mode)	
							0	1	0	0	+4/16 (–4/8 in DNR Mode)	
							0	1	0	1	+5/16 (–5/8 in DNR Mode)	
							0	1	1	0	+6/16 (–6/8 in DNR Mode)	
							0	1	1	1	+7/16 (–7/8 in DNR Mode)	
							1	0	0	0	+8/16 (–1 in DNR Mode)	
		Coring Gain Data	0	0	0	0					No Gain	
			0	0	0	1					+1/16 (–1/8 in DNR Mode)	
			0	0	1	0					+2/16 (–2/8 in DNR Mode)	
			0	0	1	1					+3/16 (–3/8 in DNR Mode)	
			0	1	0	0					+4/16 (–4/8 in DNR Mode)	
			0	1	0	1					+5/16 (–5/8 in DNR Mode)	
			0	1	1	0					+6/16 (–6/8 in DNR Mode)	
			0	1	1	1					+7/16 (–7/8 in DNR Mode)	
			1	0	0	0					+8/16 (–1 in DNR Mode)	

Table VIII. SD Registers (continued)

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
64h	SD DNR 1	DNR Threshold			0	0	0	0	0	0	0	00h
					0	0	0	0	0	1	1	
					1	1	1	1	1	0	62	
					1	1	1	1	1	1	63	
		Border Area		0							2 Pixels	
				1							4 Pixels	
		Block Size Control	0								8 Pixels	
			1								16 Pixels	
65h	SD DNR 2	DNR Input Select						0	0	1	Filter A	00h
								0	1	0	Filter B	
								0	1	1	Filter C	
								1	0	0	Filter D	
		DNR Mode				0					DNR Mode	
						1					DNR Sharpness Mode	
		DNR Block Offset	0	0	0	0					0 Pixel Offset	
			0	0	0	1					1 Pixel Offset	
			1	1	1	0					14 Pixel Offset	
			1	1	1	1					15 Pixel Offset	
66h	SD Gamma A	SD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A0	00h
67h	SD Gamma A	SD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A1	00h
68h	SD Gamma A	SD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A2	00h
69h	SD Gamma A	SD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A3	00h
6Ah	SD Gamma A	SD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A4	00h
6Bh	SD Gamma A	SD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A5	00h
6Ch	SD Gamma A	SD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A6	00h
6Dh	SD Gamma A	SD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A7	00h
6Eh	SD Gamma A	SD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A8	00h
6Fh	SD Gamma A	SD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A9	00h
70h	SD Gamma B	SD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B0	00h
71h	SD Gamma B	SD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B1	00h
72h	SD Gamma B	SD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B2	00h
73h	SD Gamma B	SD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B3	00h
74h	SD Gamma B	SD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B4	00h
75h	SD Gamma B	SD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B5	00h
76h	SD Gamma B	SD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B6	00h
77h	SD Gamma B	SD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B7	00h
78h	SD Gamma B	SD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B8	00h
79h	SD Gamma B	SD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B9	00h
7Ah	SD Brightness Detect	SD Brightness Value	X	X	X	X	X	X	X	X	Read-Only	
7Bh	Field Count Register	Field Count						X	X	X	Read-Only	
		Reserved					0				Zero must be written to this bit.	
		Reserved				0					Zero must be written to this bit.	
		Reserved			0						Zero must be written to this bit.	
		Reserved Code	X	X							Read-Only	

Table VIII. SD Registers (continued)

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
7Ch	Reset Register	Timing Reset								0	No reset of Timing Generator in Subcarrier Reset Mode. 0x44h, Bits 1 and 2 must be set to Subcarrier Reset.	00h
										1	Reset Timing Generator in Subcarrier Reset Mode	
		Reserved							0		Zero must be written to this bit.	
		Reserved						0			Zero must be written to this bit.	
		Reserved					0				Zero must be written to this bit.	
		Reserved				0					Zero must be written to this bit.	
		Reserved			0						Zero must be written to this bit.	
		Reserved		0							Zero must be written to this bit.	
		Reserved	0								Zero must be written to this bit.	

*Line 23

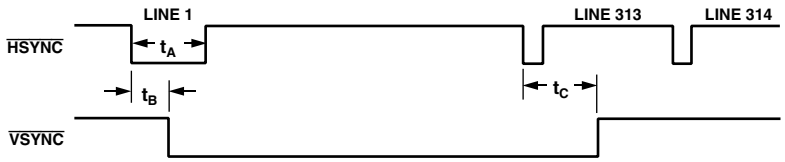


Figure 19. Timing Register 1 in PAL Mode

Table IX. Macrovision Registers*

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
7Dh	Reserved											
7Eh	Reserved											
7Fh	Reserved											
80h	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 3a [7:0]	00h
81h	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 3b [15:8]	00h
82h	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 3c [23:16]	00h
83h	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 3d [31:24]	00h
84h	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 3e [39:32]	00h
85h	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 3f [47:40]	00h
86h	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 40 [55:48]	00h
87h	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 41 [63:56]	00h
88h	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 42 [71:64]	00h
89h	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 43 [79:72]	00h
8Ah	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 44 [87:80]	00h
8Bh	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 45 [95:88]	00h
8Ch	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 46 [103:96]	00h
8Dh	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 47 [111:104]	00h
8Eh	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 48 [119:112]	00h
8Fh	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 49 [127:120]	00h
90h	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 4A [135:128]	00h
91h	Macrovision	MV Control Bit								X	MV 4B [136]	00h
			0	0	0	0	0	0	0		Zero must be written to these bits.	

*Macrovision Registers are only available on the ADV7300A.

INPUT AND OUTPUT CONFIGURATION
STANDARD DEFINITION ONLY

The 8- or 10-bit multiplexed input data is input on Pins S9–S0, with S0 being the LSB in 10-Bit Input Mode. For 8-bit Input Mode, the data is input on Pins S9–S2. ITU-R.BT601/ITU-R.BT656 input standards are supported. In 16-Bit Input Mode, the Y pixel data is input on Pins S9–S2 and CrCb data on Pins Y9–Y2. In 20-Bit Input Mode, the Y pixel data is input on S9–S0 and CrCb pixel data on Pins Y9–Y0. The 27 MHz clock input must be input on Pin CLKIN_A. Input sync signals are optional and are input on the S_VSYNC, S_HSYNC, and S_BLANK pins.

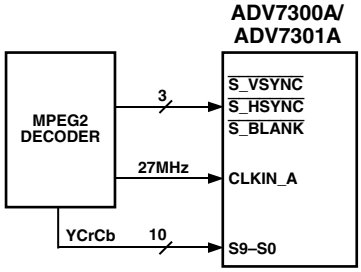


Figure 20. Standard Definition Only Input Mode

PROGRESSIVE SCAN ONLY OR HDTV ONLY

YCrCb Progressive Scan, HDTV, or any other HD YCrCb data can be input in 4:2:2 or 4:4:4 format. In 4:2:2 Input Mode, the Y data is input on Pins Y9–Y0 and the CrCb data on Pins C9–C0. In 4:4:4 Input Mode, Y data is input on Pins Y9–Y0, Cb data on Pins C9–C0, and Cr data on Pins S9–S0. If the YCrCb data does not conform to SMPTE293M (525 p), ITU-R.BT1358M (625 p), SMPTE274M (1080 i), SMPTE296M (720 p), or BTA-T1004, the Async Timing Mode must be used. RGB data can only be input in 4:4:4 format in PS Input Mode only, or HDTV Input Mode only, when HD RGB input is enabled. G data is input on Pins Y9–Y0, R data on S9–S0, and B data on Pins C9–C0. The clock signal must be input on Pin CLKIN_A. Synchronization signals are optional and are input on Pins P_VSYNC, P_HSYNC, and P_BLANK.

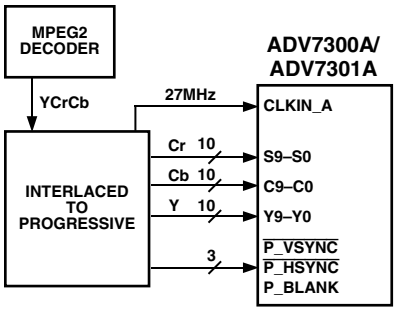


Figure 21. Progressive Scan Only Input Mode

SIMULTANEOUS STANDARD DEFINITION AND PROGRESSIVE SCAN OR HDTV

YCrCb PS, HDTV, or any other HD data must be input in 4:2:2 format. In 4:2:2 Input Mode, the Y data is input on Pins Y9–Y0 and the CrCb data on C9–C0. If PS 4:2:2 data is interleaved onto a single 10-bit bus, Pins Y9–Y0 are used for the Input Port. The interleaved data is to be input at 27 MHz in setting the Input Mode Register at Address 01h accordingly. If the YCrCb data does not conform to SMPTE293M (525 p), ITU-R.BT1358M (625 p), SMPTE274M (1080 i), SMPTE296M (720 p), or BTA-T1004, the Async Timing Mode must be used.

The 8- or 10-bit standard definition data must be compliant to ITU-R.BT601/ITU-R.BT656 in 4:2:2 format. Standard definition data is input on Pins S9–S0, with S0 being the LSB. Using 8-bit input format, the data is input on Pins S9–S2. The clock input for SD must be input on CLKIN_A, and the clock input for HD must be input on CLKIN_B. Synchronization signals are optional. SD syncs are input on Pins S_VSYNC, S_HSYNC, and S_BLANK; the HD syncs on Pins P_VSYNC, P_HSYNC, and P_BLANK.

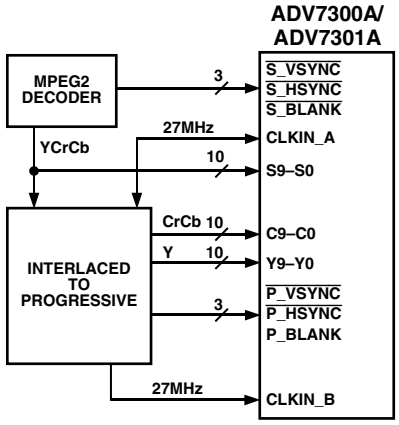


Figure 22. Simultaneous Progressive Scan and SD Input

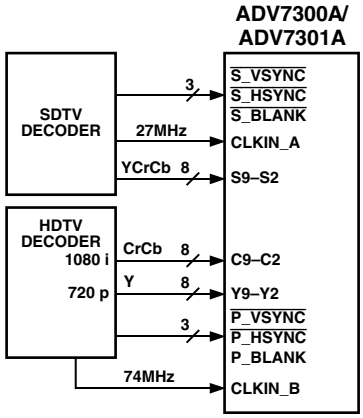


Figure 23. Simultaneous HDTV and SD Input

If in Simultaneous Input Mode the two clock phases differ by less than 9.25 ns or more than 27.75 ns, the Clock Align Bit must be set accordingly. This also applies if the Pixel Align Bit is set. If the application uses the same clock source for both SD and PS, the Clock Align Bit must be set since the phase difference between both inputs is less than 9.25 ns.

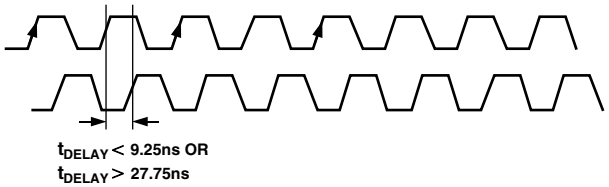


Figure 24. Clock Phase with Two Input Clocks

PROGRESSIVE SCAN AT 27 MHz OR 54 MHz

YCrCb progressive scan data can be input at 27 MHz or 54 MHz. The input data is interleaved onto a single 10-bit bus and is input on Pins Y9–Y0. For PS Input Only Mode, the input clock must be input on CLKIN_A. In Simultaneous SD/HD Mode, the input clock is input on CLKIN_B.

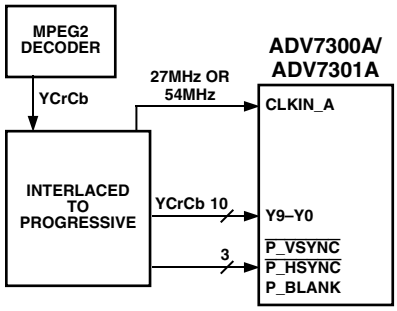


Figure 25. 1 × 10-Bit PS @ 27 MHz or 54 MHz

When the input sequence of the PS data, i.e., 10-bit interleaved at 27 MHz, starts with Y0 data, as shown in Figure 26, PIXEL ALIGN [Subaddress 01h] must be set to "0." In this case, the timing information embedded in the data stream is recognized and the video data is transferred to the according Y channel and CrCb channel processing blocks.

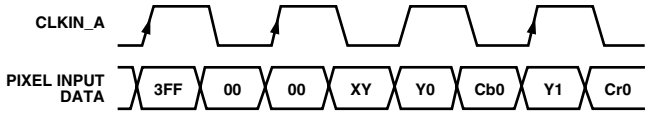


Figure 26. Input Sequence in PS 10-Bit Interleaved Mode, EAV/SAV Followed by Y0 Data

If the input sequence starts with Cb0 data as shown in Figure 27, initially PIXEL ALIGN [Subaddress 01h] must be set to "0." This ensures that the ADV7300A/ADV7301A locks to the input sequence in decoding the embedded timing information correctly. For correct color decoding, the Pixel Align Bit [Subaddress 01h] must then be set to "l" after a delay of one field. The ADV7300A/ADV7301A is now in free run mode; any changes in the timing information are ignored.

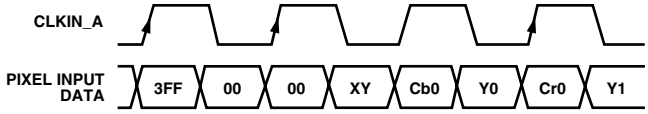


Figure 27. Input Sequence in PS 10-Bit Interleaved Mode, EAV/SAV Followed by Cb0 Data

PS 10-bit interleaved at 54 MHz must be input with separate timing signals. EAV/SAV codes cannot be used in this mode.

Table X. Overview of All Possible Input Configurations

Input Format	Total Bits		Input Video	Input Pins	Subaddress	Register Setting
ITU-R.BT656	8	4:2:2	YCrCb	S9–S2 [MSB = S9]	01h, 48h	00h, 00h
	10	4:2:2	YCrCb	S9–S0 [MSB = S9]	01h, 48h	00h, 10h
	16	4:2:2	Y	S9–S2 [MSB = S9]	01h, 48h	00h, 08h
			CrCb	Y9–Y2 [MSB = Y9]		
	20	4:2:2	Y	S9–S0 [MSB = S9]	01h, 48h	00h, 18h
			CrCb	Y9–Y0 [MSB = Y9]		
PS Only	8 (27 MHz Clock)	4:2:2	YCrCb	Y9–Y2 [MSB = Y9]	01h, 13h	10h, 40h
	10 (27 MHz Clock)	4:2:2	YCrCb	Y9–Y0 [MSB = Y9]	01h, 13h	10h, 44h
	8 (54 MHz Clock)	4:2:2	YCrCb	Y9–Y2 [MSB = Y9]	01h, 13h	70h, 40h
	10 (54 MHz Clock)	4:2:2	YCrCb	Y9–Y0 [MSB = Y9]	01h, 13h	10h, 44h
	16	4:2:2	Y	Y9–Y2 [MSB = Y9]	01h, 13h	10h, 40h
			CrCb	C9–C2 [MSB = C9]		
	20	4:2:2	Y	Y9–Y0 [MSB = Y9]	01h, 13h	10h, 44h
			CrCb	C9–C0 [MSB = C9]		
	24	4:4:4	Y	Y9–Y2 [MSB = Y9]	01h, 13h	10h, 00h
			Cb	C9–C2 [MSB = C9]		
			Cr	S9–S2 [MSB = S9]		
	30	4:4:4	Y	Y9–Y0 [MSB = Y9]	01h, 13h	10h, 04h
			Cb	C9–C0 [MSB= C9]		
			Cr	S9–S0 [MSB = S9]		
HDTV Only	8	4:2:2	YCrCb	Y9–Y2 [MSB = Y9]	01h, 13h	20h, 40h
	10	4:2:2	YCrCb	Y9–Y0 [MSB = Y9]	01h, 13h	20h, 44h
	16	4:2:2	Y	Y9–Y2 [MSB = Y9]	01h, 13h	20h, 40h
			CrCb	C9–Y2 [MSB = C9]		
	20	4:2:2	Y	Y9–Y0 [MSB = Y9]	01h, 13h	20h, 44h
			CrCb	C9–C0 [MSB = C9]		
	24	4:4:4	Y	Y9–Y2 [MSB = Y9]	01h, 13h	20h, 00h
			Cb	C9–Y2 [MSB = C9]		
			Cr	S9–S2 [MSB = S9]		
	30	4:4:4	Y	Y9–Y0 [MSB = Y9]	01h, 13h	20h, 04h
			Cb	C9–C0 [MSB = C9]		
			Cr	S9–S0 [MSB = S9]		
HD RGB	24	4:4:4	G	Y9–Y2 [MSB = Y9]	01h, 13h, 15h	10h or 20h, 00h, 02h
			B	C9–C2 [MSB = C9]		
			R	S9–S2 [MSB = S9]		
	30	4:4:4	G	Y9–Y0 [MSB = Y9]	01h, 13h, 15h	10h or 20h, 04h, 02h
			B	C9–C0 [MSB = C9]		
			R	S9–S0 [MSB = S9]		
ITU-R.BT656 and PS	8	4:2:2	YCrCb	S9–S2 [MSB = S9]	01h	40h
		4:2:2	YCrCb	Y9–Y2 [MSB = Y9]	13h, 48h	40h, 00h
	10	4:2:2	YCrCb	S9–S0 [MSB = S9]	01h	40h
		4:2:2	YCrCb	Y9–Y0 [MSB = Y9]	13h, 48h	44h, 10h
ITU-R.BT656 and PS or HDTV	8	4:2:2	YCrCb	S9–S2 [MSB = S9]	01h	30h, 50h, or 60h
	10	4:2:2	YCrCb	S9–S0 [MSB = S9]	01h	30h, 50h, or 60h
	16	4:2:2	Y	Y9–Y2 [MSB = Y9]	13h, 48h	40h, 00h
			CrCb	C9–C2 [MSB = C9]		
	20	4:2:2	Y	Y9–Y0 [MSB = Y9]	13h, 48h	44h, 10h
			CrCb	C9–C0 [MSB = C9]		

OUTPUT CONFIGURATION

Tables XI–XIII demonstrate what output signals are assigned to the DACs when corresponding control bits are set.

Table XI. Output Configuration in SD Only Mode

RGB/YUV O/P Addr 0x02h, Bit 5	SD DAC O/P 1 Addr 0x42h, Bit 2	SD DAC O/P 2 Addr 0x42h, Bit 1	DAC A	DAC B	DAC C	DAC D	DAC E	DAC F
0	0	0	CVBS	Luma	Chroma	G	B	R
0	0	1	G	B	R	CVBS	Luma	Chroma
0	1	0	G	Luma	Chroma	CVBS	B	R
0	1	1	CVBS	B	R	G	Luma	Chroma
1	0	0	CVBS	Luma	Chroma	Y	U	V
1	0	1	Y	U	V	CVBS	Luma	Chroma
1	1	0	Y	Luma	Chroma	CVBS	U	V
1	1	1	CVBS	U	V	Y	Luma	Chroma

Table XII. Output Configuration in HD Only Mode

HD I/P Format	HD RGB I/P Addr 0x15h, Bit 1	RGB/YUV O/P Addr 0x02h, Bit 5	HD Color Swap Addr 0x15h, Bit 3	DAC A	DAC B	DAC C	DAC D	DAC E	DAC F
YCrCb 4:2:2	N/A	0	0	N/A	N/A	N/A	G	B	R
YCrCb 4:2:2	N/A	0	1	N/A	N/A	N/A	G	R	B
YCrCb 4:2:2	N/A	1	0	N/A	N/A	N/A	Y	Pb	Pr
YCrCb 4:2:2	N/A	1	1	N/A	N/A	N/A	Y	Pr	Pb
YCrCb 4:4:4	N/A	0	0	N/A	N/A	N/A	G	B	R
YCrCb 4:4:4	N/A	0	1	N/A	N/A	N/A	G	R	B
YCrCb 4:4:4	N/A	1	0	N/A	N/A	N/A	Y	Pb	Pr
YCrCb 4:4:4	N/A	1	1	N/A	N/A	N/A	Y	Pr	Pb
RGB 4:4:4	1	0	0	N/A	N/A	N/A	G	B	R
RGB 4:4:4	1	0	1	N/A	N/A	N/A	G	R	B
RGB 4:4:4	1	1	0	N/A	N/A	N/A	G	B	R
RGB 4:4:4	1	1	1	N/A	N/A	N/A	G	R	B

Table XIII. Output Configuration in Simultaneous SD/HD Mode

Input Formats	RGB/YUV O/P Addr 0x02h, Bit 5	HD Color Swap Addr 0x15h, Bit 3	DAC A	DAC B	DAC C	DAC D	DAC E	DAC F
SD YCrCb in 4:2:2 and HD YCrCb in 4:2:2	0	0	CVBS	Luma	Chroma	G	B	R
SD YCrCb in 4:2:2 and HD YCrCb in 4:2:2	0	1	CVBS	Luma	Chroma	G	R	B
SD YCrCb in 4:2:2 and HD YCrCb in 4:2:2	1	0	CVBS	Luma	Chroma	Y	Pb	Pr
SD YCrCb in 4:2:2 and HD YCrCb in 4:2:2	1	1	CVBS	Luma	Chroma	Y	Pr	Pb

TIMING MODES

HD Async Timing Mode

[Subaddress 10h, Bits 3–2]

For any input data that does not conform to SMPTE293M, SMPTE274M, SMPTE296M, or ITU-R.BT1358 standards, an Asynchronous Timing Mode can be used to interface to the ADV7300A/ADV7301A. Timing control signals for HSYNC, VSYNC, and BLANK have to be programmed by the user. Macrovision is not available in Async Timing Mode.

Figure 28 shows an example of how to program the ADV7300A/ADV7301A to accept a different high definition standard, other than SMPTE293M, SMPTE274M, SMPTE296M, or ITU-R.BT1358 standards.

Table XIV must be followed when programming the control signals in Async Timing Mode.

HD Timing Reset

A timing reset is achieved in setting the HD Timing Reset Control Bit at Address 14h from "0" to "1." In this state, the horizontal and vertical counters will remain reset. On setting this bit back to "0," the internal counters will again commence counting. The minimum time the pin has to be held high is one clock cycle; otherwise, this reset signal might not be recognized. This timing reset applies to the HD timing counters only.

SD Timing

Realtime Control, Subcarrier Reset, Timing Reset

[Subaddress 44h, Bits 2–1]

Together with the RTC_SCR_TR pin and SD Mode Register 3 [Address 44h, Bits 1–2], the ADV7300A/ADV7301A can be used in Timing Reset Mode, Subcarrier Phase Reset Mode, or RTC Mode.

a. A timing reset is achieved in a low-to-high transition on the RTC_SCR_TR pin (Pin 31). In this state, the horizontal and vertical counters will remain reset. On releasing this pin (set to low), the internal counters will again commence counting. The minimum time the pin has to be held high is one clock cycle; otherwise, this reset signal might not be recognized. This timing reset applies to the SD timing counters only.

b. Subcarrier phase reset, a low-to-high transition on the RTC_SCR_TR pin (Pin 31), will reset the subcarrier phase to zero when the SD RTC/TR/SCR control bits at Address 44h are set to "01." This reset signal will have to be held high for a minimum of one clock cycle. Since the Field Counter is not reset, it is recommended to apply the reset in Field 7 (PAL). The reset of the phase will then occur on the next field by being correctly lined up with the internal counters. The Field Count Register at Address 7Bh can be used to identify the number of the active field.

c. In RTC Mode, the ADV7300A/ADV7301A can be used to lock to an external video source. The Realtime Control Mode allows the ADV7300A/ADV7301A to automatically alter the subcarrier frequency to compensate for line length variations. When the part is connected to a device that outputs a digital data stream in the RTC format (such as a ADV7185 video decoder; see Figure 29), the part will automatically change to the compensated subcarrier frequency on a line-by-line basis. This digital data stream is 67 bits wide and the subcarrier is contained in Bits 0 to 21. Each bit is two clock cycles long. 00h should be written into all four Subcarrier Frequency Registers when using this mode.

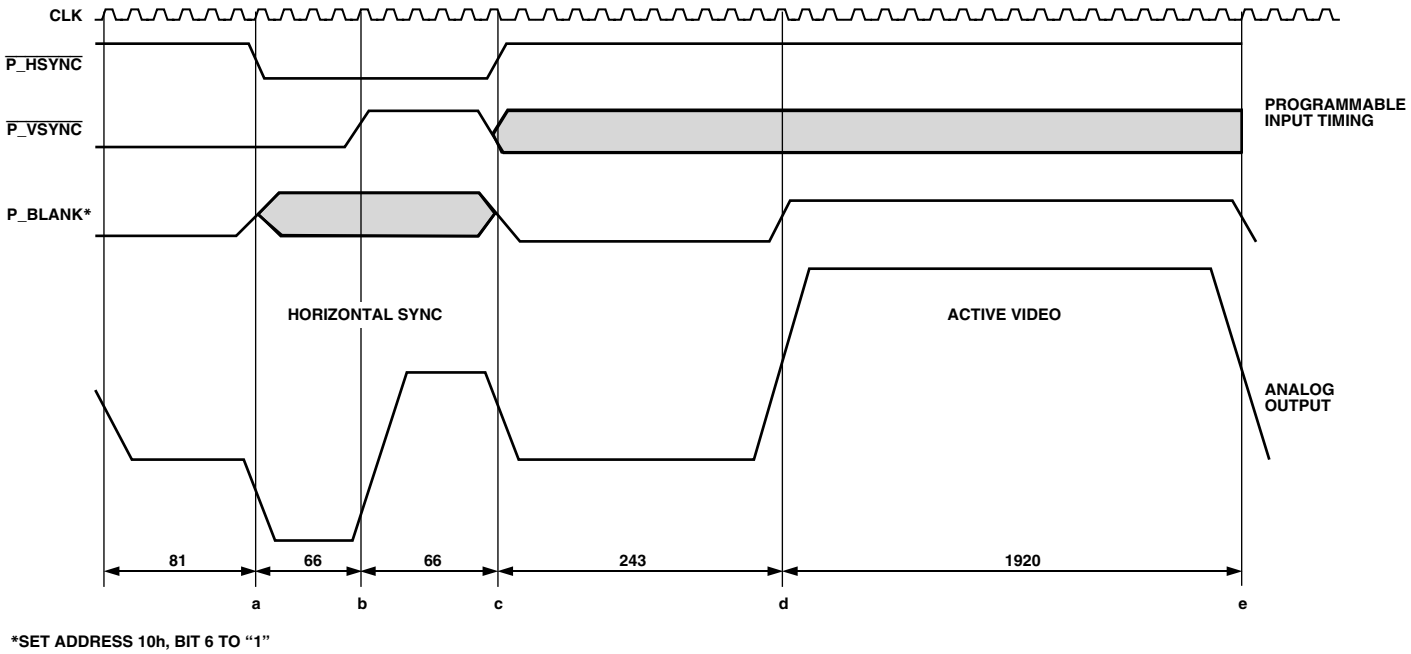
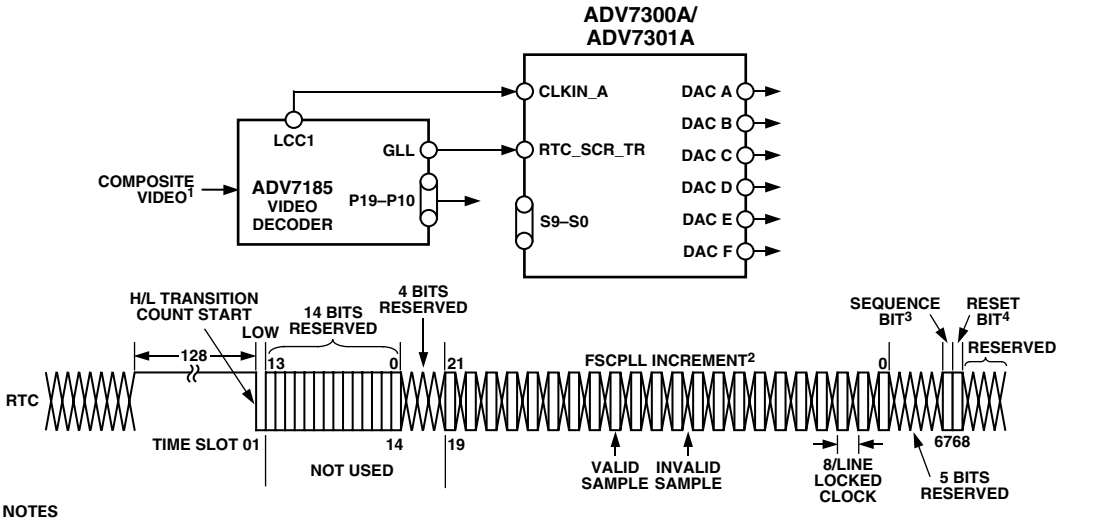


Figure 28. Async Timing Mode, Programming Input Control Signals for SMPTE295M Compatibility

Table XIV. Truth Table

$\overline{\text{P\_HSYNC}}$	$\overline{\text{P\_VSYNC}}$[1]	P_BLANK[1]		Reference[2]
1 → 0	0	0 or 1	50% point of falling edge of tri-level horizontal sync signal	a
0	0 → 1	0 or 1	25% point of rising edge of tri-level horizontal sync signal	b
0 → 1	0 or 1	0	50% point of falling edge of tri-level horizontal sync signal	c
1	0 or 1	0 → 1	50% start of active video	d
1	0 or 1	1 → 0	50% end of active video	e

NOTES
For standards that do not require a tri-sync level, P_BLANK must be tied low at all times.
[1]When Async Timing Mode is enabled, P_BLANK, Pin 25 becomes an active high input. P_BLANK is set to active low at Address 10h, Bit 6.
[2]See Figure 28.



NOTES
[1]i.e., VCR OR CABLE
[2]F_{SC} PLL INCREMENT IS 22 BITS LONG. VALUE LOADED INTO ADV7300A/ADV7301A F_{SC} DDS REGISTER IS F_{SC} PLL INCREMENTS BITS 21:0 PLUS BITS 0:9 OF SUBCARRIER FREQUENCY REGISTERS. ALL ZEROS SHOULD BE WRITTEN TO THE SUBCARRIER FREQUENCY REGISTERS OF THE ADV7300A/ADV7301A.
[3]PAL: 0 = LINE NORMAL, 1 = LINE INVERTED; NTSC: 0 = NO CHANGE
[4]RESET ADV7300A/ADV7301A DDS

Figure 29. RTC Timing and Connections

SD VCR FF/RW Sync
[Subaddress 42h, Bit 5]
In DVD record applications where the encoder is used with a decoder, the VCR FF/RW Sync Control Bit can be used for nonstandard input video, i.e., in Fast Forward or Rewind Modes. In Fast Forward Mode, the sync information for the start of a new field in the incoming video usually occurs before the total number of lines/fields are reached; in Rewind Mode, this sync signal occurs usually after the total number of lines/fields are reached. Conventionally, this means that the output video will have an erroneous start of new field signals, one generated by the incoming video and one when the internal lines/field counters reach the end of a field. When VCR FF/RW sync control is enabled [Subaddress 42h, Bit 5], the lines/field counters are updated according to the incoming VSYNC signal, and the analog output matches the incoming VSYNC signal.

This control is available in all slave timing modes except Slave Mode 0.

RESET SEQUENCE
A reset is activated with a high-to-low transition on the $\overline{\text{RESET}}$ pin (Pin 33) according to the timing specifications. The ADV7300A/ADV7301A will revert to the default output configuration. Figure 30 illustrates the $\overline{\text{RESET}}$ sequence timing.

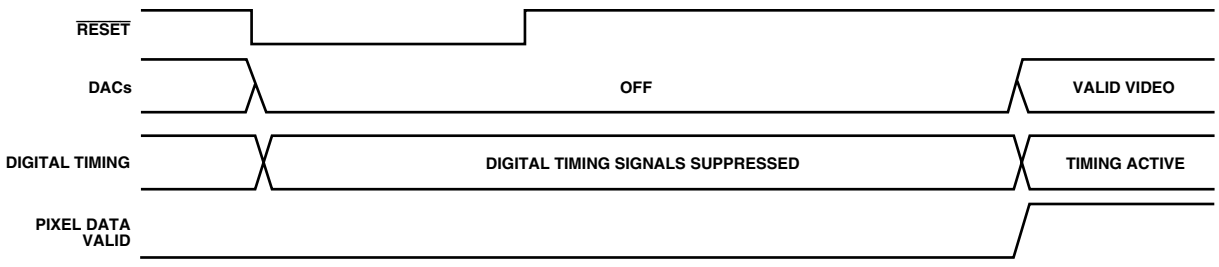


Figure 30. $\overline{\text{RESET}}$ Timing Sequence

VERTICAL BLANKING INTERVAL

The ADV7300A/ADV7301A accepts input data that contains VBI data [CGMS, WSS, VITS, etc.] in SD and HD Modes.

For SMPTE293M (525 p) standards, VBI data can be inserted on Lines 13 to 42 of each frame, or Lines 6 to 43 for ITU-R.BT1358 (625 p) standard.

For SD NTSC, this data can be present on Lines 10 to 20, in PAL on Lines 7 to 22.

If VBI is disabled [Address 11h, Bit 4 for HD; Address 43h, Bit 4 for SD], VBI data is not present at the output and the entire VBI is blanked. These control bits are valid in all master and slave modes.

In Slave Mode 0, if VBI is enabled, the Blanking Bit in the EAV/SAV code is overwritten and it is possible to use VBI in this timing mode as well.

In Slave Mode 1 or 2, the $\overline{\text{BLANK}}$ Control Bit must be set to enabled [Address 4Ah, Bit 3] to allow VBI data to pass through the ADV7300A/ADV7301A. Otherwise, the ADV7300A/ADV7301A automatically blanks the VBI to standard.

If CGMS is enabled and VBI disabled, the CGMS data will nevertheless be available at the output.

SD SUBCARRIER FREQUENCY REGISTERS

[Subaddress 4Ch–4Fh]

Four 8-bit wide registers are used to set up the subcarrier frequency. The value of these registers is calculated in using the equation:

$$\textit{Subcarrier Frequency Register} = \frac{\#\ of\ \ Subcarrier\ \ Frequency\ \ Cycles\ in\ \ One\ Video\ \ Line}{\#\ of\ \ 27\ \ MHz\ \ Clock\ \ Cycles\ in\ \ One\ Video\ \ Line} \times 2^{32}$$

Example:
NTSC Mode

$$\textit{Subcarrier Frequency} = \frac{227.5}{1716} \times 2^{32} = 569408542\,*$$

Subcarrier Register Value = 21F07C1Eh

SD F_{SC} Register 0: 1E
SD F_{SC} Register 1: 7Ch
SD F_{SC} Register 2: F0h
SD F_{SC} Register 3: 21h

Refer to the MPU Port Description section for more detail on how to access the subcarrier frequency registers.

SUBCARRIER PHASE REGISTER

[Subaddress 50h, 5Ch, Bits 7, 6]

Ten bits are used to set up the subcarrier phase. Each bit represents 0.352°. For normal operation, this register is set to 00h.

*Rounded to the nearest integer

FILTERS

Table XV shows an overview of the programmable filters available on the ADV7300A/ADV7301A.

Table XV. Selectable Filters

Filter	Subaddress
SD Luma LPF NTSC	40h
SD Luma LPF PAL	40h
SD Luma Notch NTSC	40h
SD Luma Notch PAL	40h
SD Luma SSAF	40h
SD Luma CIF	40h
SD Luma QCIF	40h
SD Chroma 0.65 MHz	40h
SD Chroma 1.0 MHz	40h
SD Chroma 1.3 MHz	40h
SD Chroma 2.0 MHz	40h
SD Chroma 3.0 MHz	40h
SD Chroma CIF	40h
SD Chroma QCIF	40h
SD UV SSAF	42h
HD Chroma Input	13h
HD Sync Filter	13h
HD Chroma SSAF	13h

HD Sync Filter

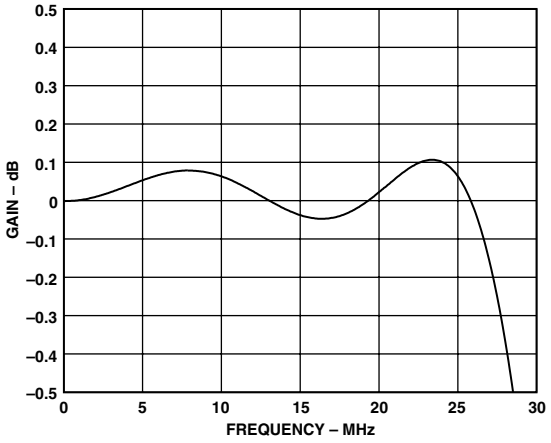


Figure 31. HD Sync Filter Enabled

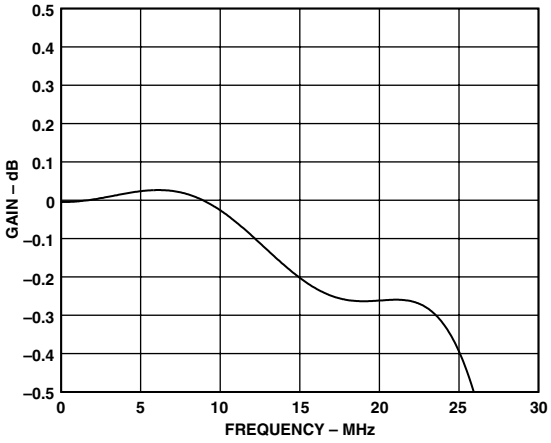


Figure 32. HD Sync Filter Disabled

HD 4:2:2 to 4:4:4 Interpolation Filters and Chroma SSAF
It is recommended to input data in 4:2:2 Input Mode to make use of the HD chroma SSAFs on the ADV7300A/ADV7301A. This filter has a 0 dB pass-band response and prevents signal components being folded back into the frequency band. In 4:4:4 Input Mode, the video data is already interpolated by the external input device and the chroma SSAFs of the ADV7300A/ADV7301A are bypassed.

The chroma SSAF is controlled with Address 13h, Bit 5. When the HD input format is 4:2:2, the HD Chroma Input Bit [Address 13h, Bit 6] must be set to "1."

2×/4×/8× Oversampling Filters
The oversampling filters are enabled in setting the PLL ON control [Subaddress 00h, Bit 1] to "1." If enabled, PS and ITU-R.BT656 data is output at a rate of 108 MHz, HDTV at a rate of 148 MHz.

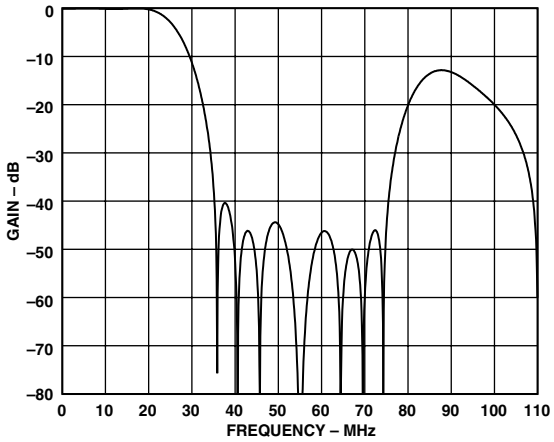


Figure 33. Y – PS 4× Oversampling Filter

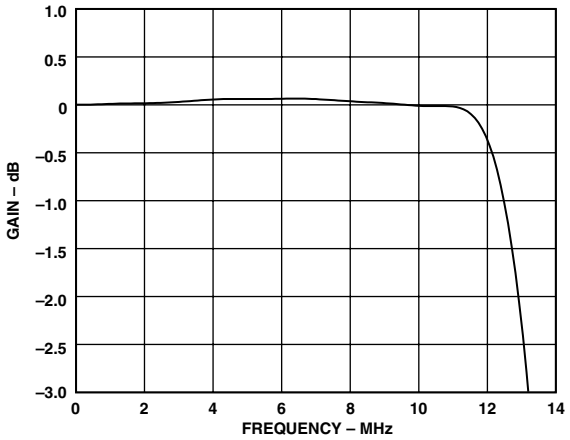


Figure 34. Y – PS 4× Oversampling Filter in the Pass Band

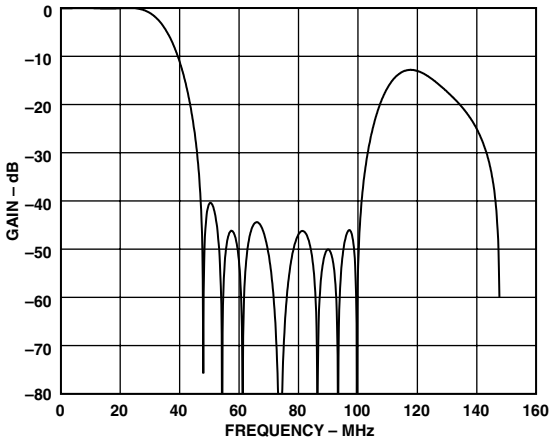


Figure 35. Y – HDTV 2× Oversampling Filter

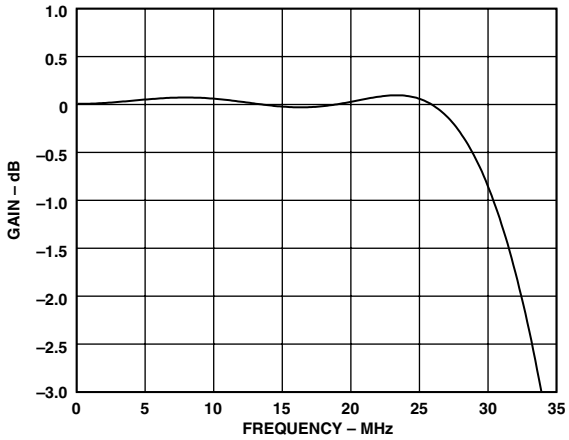


Figure 36. Y – HDTV 2× Oversampling Filter in the Pass Band

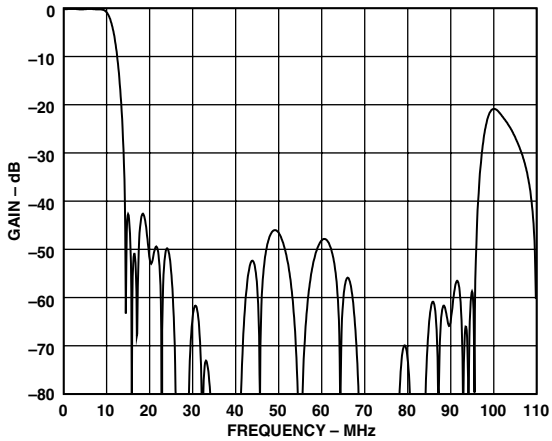


Figure 37. UV – HDTV 2× Oversampling Filter

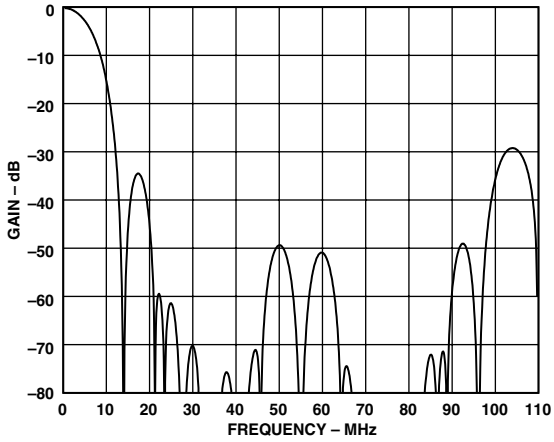


Figure 38. UV – PS 4× Oversampling Filter, Linear

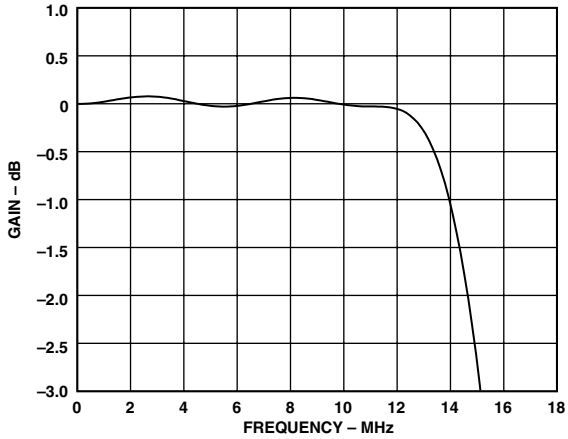


Figure 39. UV – HDTV 2× Oversampling Filter, Pass Band

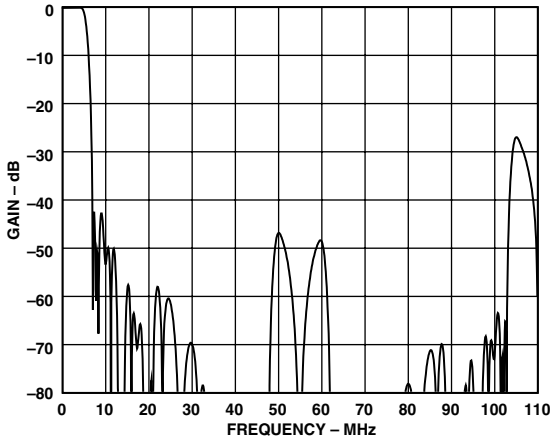


Figure 40. UV – PS 4× Oversampling Filter, SSAF

ADV7300A/ADV7301A

SD Internal Filter Response
[Subaddress 42h, Bit 0]

The Y filter supports several different frequency responses including two low-pass responses, two notch responses, an extended (SSAF) response with or without gain boost/attenuation, a CIF response, and a QCIF response. The UV filter supports several different frequency responses, including six low-pass responses, a CIF response, and a QCIF response, as can be seen in Figures 41–59.

If SD SSAF gain is enabled, there is the option of 12 responses in the range from –4 dB to +4 dB. The desired response can be chosen by the user by programming the correct value via the I^2C. The variation of frequency responses can be seen in Figures 41–59.

Inaddition to the chroma filters listed above, the ADV7300A/ADV7301A contains an SSAF filter specifically designed for and applicable to the color difference component outputs U and V. This filter has a cutoff frequency of approximately 2.7 MHz and –40 dB at 3.8 MHz, as shown in Figure 41. This filter can be controlled via Address 42h, Bit 0. If this filter is disabled, the selectable chroma filters shown in Table XVI can be used for the CVBS or chroma signal.

Table XVI. Internal Filter Specifications

Filter	Pass-Band Ripple[1] (dB)	3 dB Bandwidth[2] (MHz)
Luma LPF NTSC	0.16	4.24
Luma LPF PAL	0.1	4.81
Luma Notch NTSC	0.09	2.3/4.9/6.6
Luma Notch PAL	0.1	3.1/5.6/6.4
Luma SSAF	0.04	6.45
Luma CIF	0.127	3.02
Luma QCIF	Monotonic	1.5
Chroma 0.65 MHz	Monotonic	0.65
Chroma 1.0 MHz	Monotonic	1
Chroma 1.3 MHz	0.09	1.395
Chroma 2.0 MHz	0.048	2.2
Chroma 3.0 MHz	Monotonic	3.2
Chroma CIF	Monotonic	0.65
Chroma QCIF	Monotonic	0.5

NOTES
[1]Pass-band ripple is the maximum fluctuation from the 0 dB response in the pass band, measured in dB. The pass band is defined to have 0 Hz to fc (Hz) frequency limits for a low-pass filter, 0 Hz to f1 (Hz) and f2 (Hz) to infinity for a notch filter, where fc, f1, f2 are the –3 dB points.
[2]+3 dB bandwidth refers to the –3 dB cutoff frequency.

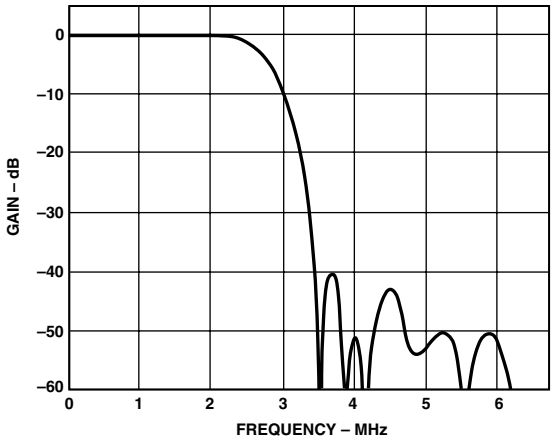


Figure 41. UV SSAF Filter

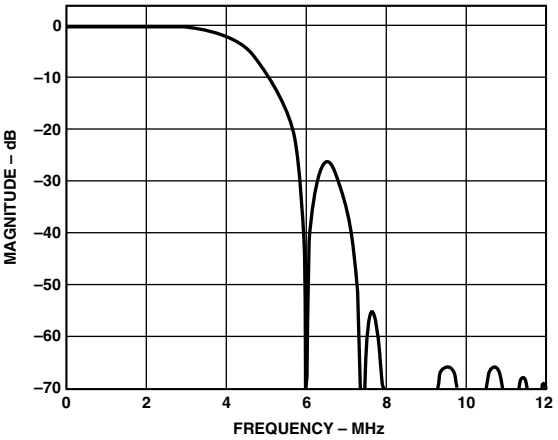


Figure 42. Luma NTSC Low-Pass Filter

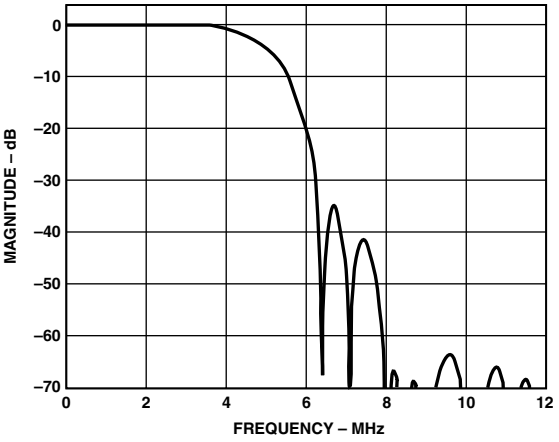


Figure 43. Luma PAL Low-Pass Filter

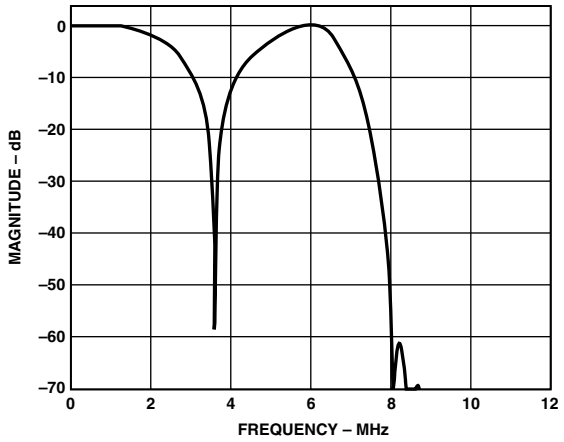


Figure 44. Luma NTSC Notch Filter

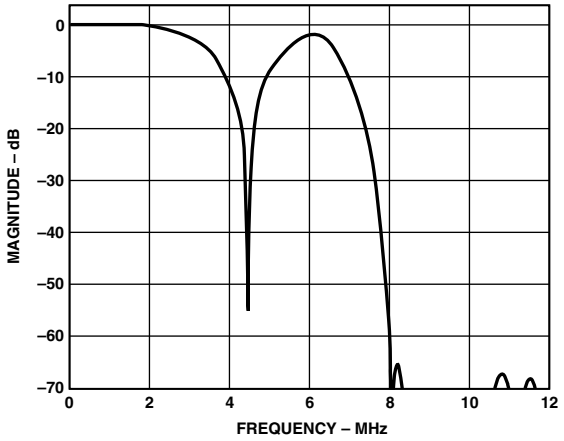


Figure 45. Luma PAL Notch Filter

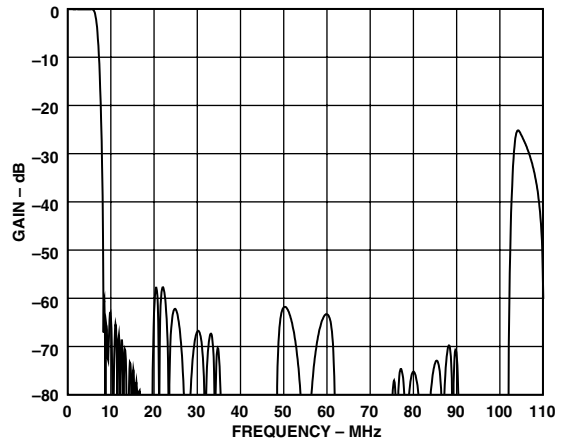


Figure 46. Luma SSAF Filter up to 108 MHz

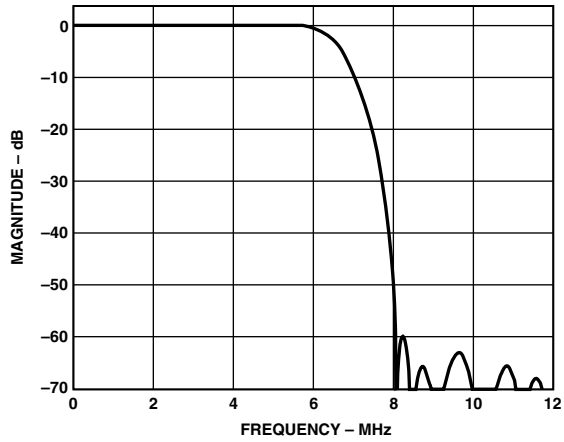


Figure 47. Luma SSAF Filter up to 12 MHz

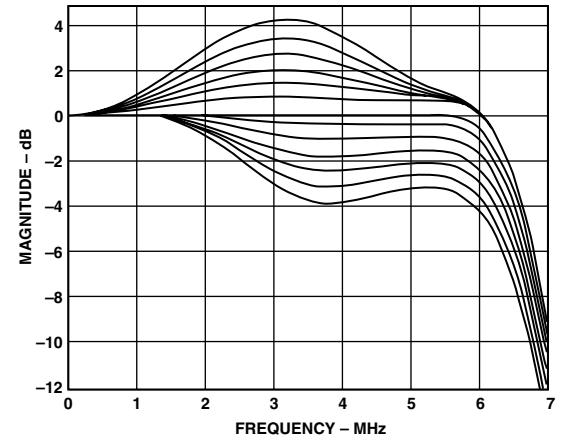


Figure 48. Luma SSAF Filter, Programmable Responses

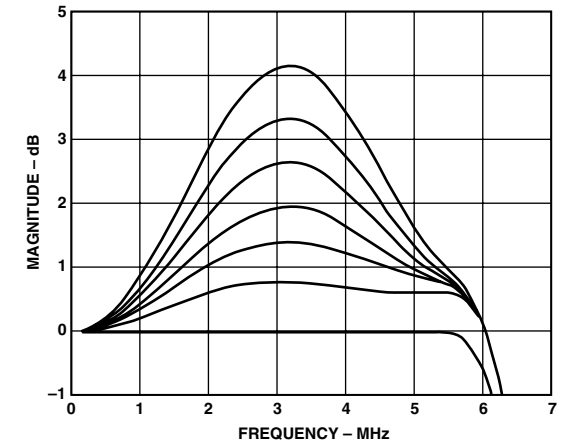


Figure 49. Luma SSAF Filter, Programmable Gain

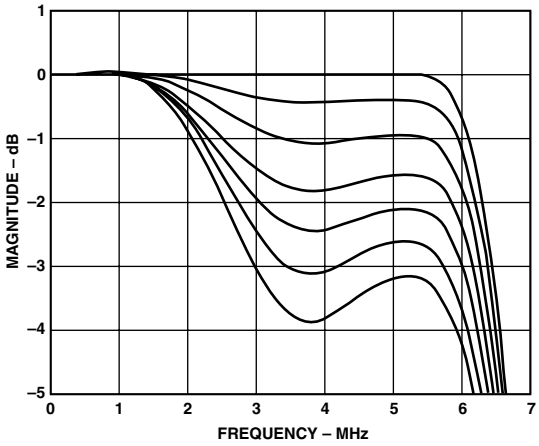


Figure 50. Luma SSAF Filter, Programmable Attenuation

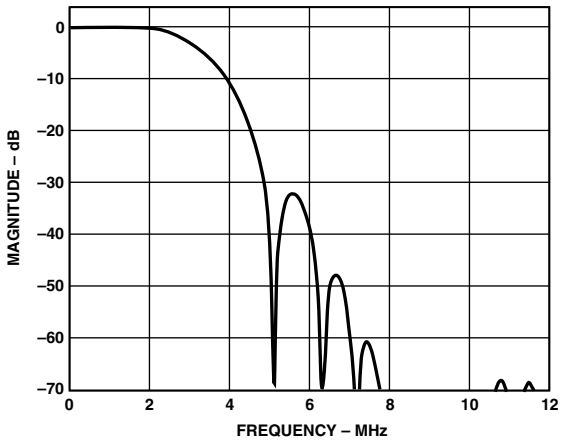


Figure 51. Luma CIF LP Filter

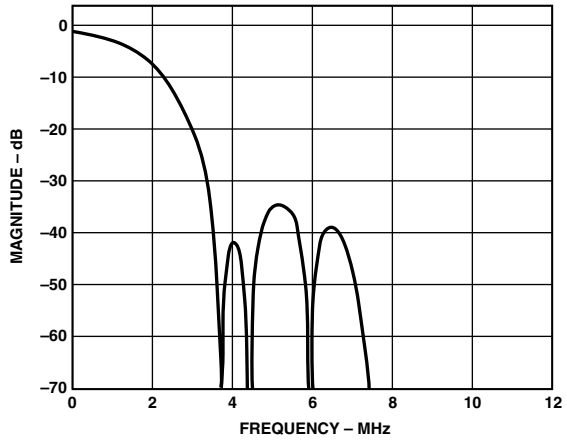


Figure 52. Luma QCIF LP Filter

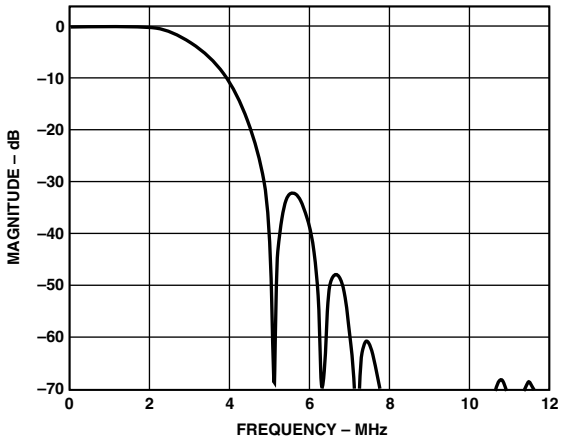


Figure 53. Chroma 3.0 MHz LP Filter

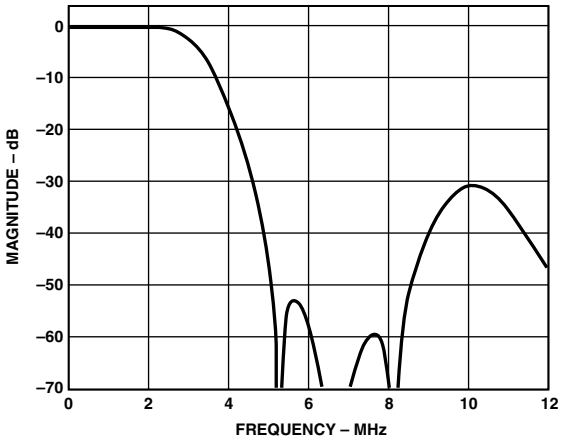


Figure 54. Chroma 2.0 MHz LP Filter

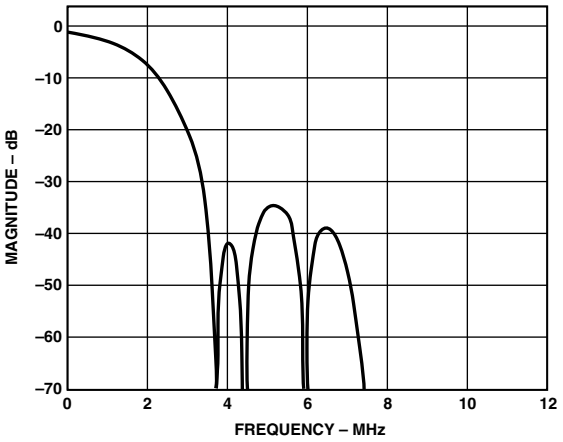


Figure 55. Chroma 1.3 MHz LP Filter

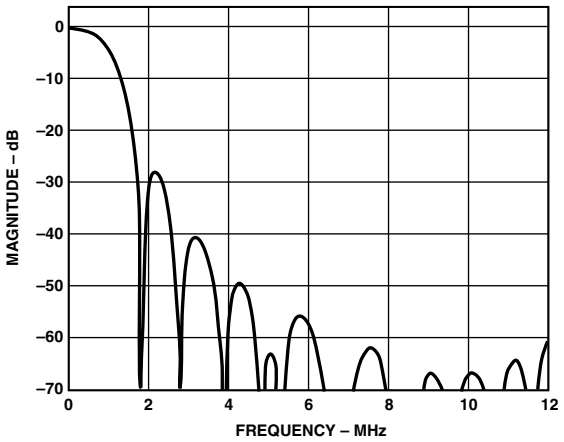


Figure 56. Chroma 1.0 MHz LP Filter

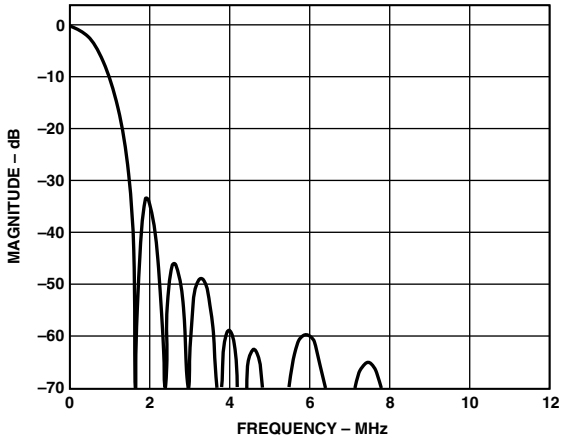


Figure 57. Chroma 0.65 MHz LP Filter

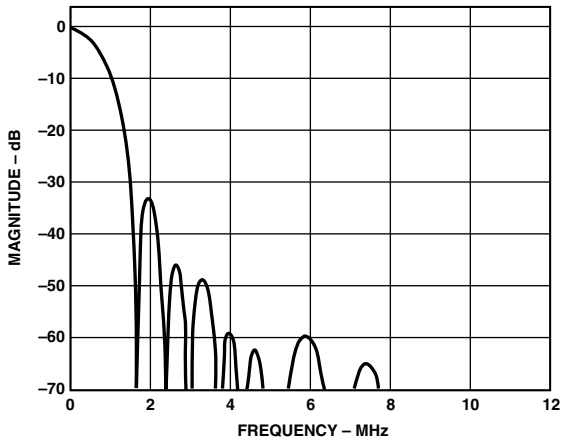


Figure 58. Chroma CIF LP Filter

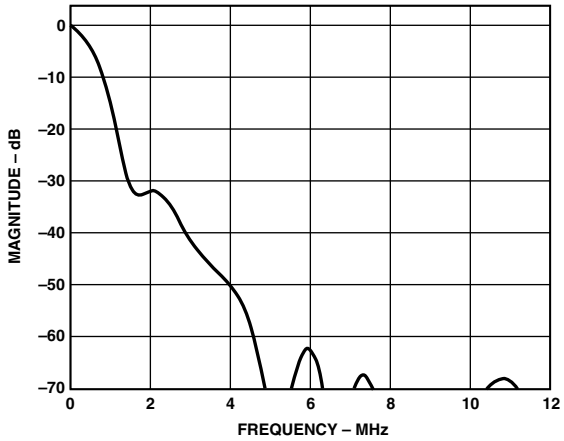


Figure 59. Chroma QCIF LP Filter

COLOR CONTROLS AND RGB MATRIX

HD Y Color, HD Cr Color, HD Cb Color [Subaddresses 16h–18h]

Three 8-bit wide registers at Addresses 16h, 17h, and 18h are used to program the output color of the internal HD test pattern generator, be it the lines of the crosshatch pattern or the uniform field test pattern. They are not functional as color controls on external pixel data input. For this purpose, the RGB matrix is used.

The standard used for the values for Y and the color difference signals to obtain white, black, and the saturated primary and complementary colors conforms to the ITU-R.BT601–ITU-R.BT604 standards. Table XVII shows sample color values to be programmed into the color registers when Output Standard Selection is set to EIA 770.2.

Table XVII. Sample Color Values for EIA 770.2 Output Standard Selection

Sample Color	Color Y Value	Color Cr Value	Color Cb Value
White	235 (EB)	128 (80)	128 (80)
Black	16 (10)	128 (80)	128 (80)
Red	81 (51)	240 (F0)	90 (5A)
Green	145 (91)	34 (22)	54 (36)
Blue	41 (29)	110 (6E)	240 (F0)
Yellow	210 (D2)	146 (92)	16 (10)
Cyan	170 (AA)	16 (10)	166 (A6)
Magenta	106 (6A)	222 (DE)	202 (CA)

HD RGB Matrix [Subaddresses 03h–09h]

When the programmable RGB matrix is disabled [Address 02h, Bit 3], the internal RGB matrix takes care of all YCrCb to YUV or RGB scaling according to the input standard programmed into the device.

When the programmable RGB matrix is enabled, the color components are converted according to the SMPTE274M standard (1080 i):

$$Y' = (0.2126 \times R') + (0.7152 \times G') + (0.0722 \times B')$$

$$Cb' = \frac{0.5}{1 - 0.0722} \times (B' - Y')$$

$$Cr' = \frac{0.5}{1 - 0.2126} \times (R' - Y')$$

This is reflected in the preprogrammed values for GY = 13Bh, RV = 1F0h, BU = 248h, GV = 93h, and GU = 3Bh.

If another input standard is used, the scale values for GY, GU, GV, BU, and RV have to be adjusted according to this input standard. It must be considered by the user that the color component conversion might use different scale values. For example, SMPTE293M uses the following conversion:

$$Y' = (0.299 \times R') + (0.587 \times G') + (0.114 \times B')$$

$$Cb' = \frac{0.5}{1 - 0.114} \times (B' - Y')$$

$$Cr' = \frac{0.5}{1 - 0.299} \times (R' - Y')$$

The programmable RGB matrix can be used to control the HD output levels in cases where the video output does not conform to standards due to altering the DAC output stages, such as termination resistors, for example. The programmable RGB matrix is used for external HD data and is not functional when the HD test pattern is enabled.

To make use of the programmable RGB matrix, the YCrCb data should contain the HSYNC signal on the Y channel only. The RGB matrix should be enabled [Address 02h, Bit 3], the output should be set to RGB [Address 02h, Bit 3], Sync on PrPb should be disabled [Address 15h, Bit 2], and Sync on RGB is optional [Address 02h, Bit 4].

GY at Addresses 03h and 05h control the output levels on the green signal, BU at 04h and 08h the blue signal output levels, and RV at 04h and 09h the red output levels. To control YPrPb output levels, YUV output should be enabled [Address 02h, Bit 5]. In this case, GY [Address 05h; Address 03, Bits 0–1] is used for the Y output, RV [Address 09; Address 04, Bits 0–1] is used for the Pr output, and BU [Address 08h; Address 04h, Bits 2–3] is used for the Pb output.

If RGB output is selected, the RGB matrix scaler uses the following equations:

$$R = GY \times Y + RV \times Cr$$

$$G = GY \times Y - GU \times Cb - GV \times Cr$$

$$B = GY \times Y + BU \times Cb$$

If YUV output is selected, the following equations are used:

$$R = RV \times Cr$$

$$G = GY \times Y$$

$$B = BU \times Cb$$

On power-up, the RGB matrix is programmed with default values:

Address 0x03h: 03h
Address 0x04h: F0h
Address 0x05h: 4Eh
Address 0x06h: 0Eh
Address 0x07h: 24h
Address 0x08h: 92h
Address 0x09h: 7Ch

When the programmable RGB matrix is not functional, the ADV7300A/ADV7301A automatically scales YCrCb inputs to all standards supported. For SMPTE293M, the register values are as follows:

Address 0x03h: 03h
Address 0x04h: 1Eh
Address 0x05h: 4Eh
Address 0x06h: 1Bh
Address 0x07h: 38h
Address 0x08h: 8Bh
Address 0x09h: 6Eh

Address 15h, Bit 3 must be set to "1" in this mode.

SD Color Control [Subaddresses 5Ch, 5Dh, 5Eh, and 5Fh]

SD Y SCALE, SD Cr SCALE, and SD Cb SCALE are three 10-bit wide control registers to scale the Y, U, and V output levels.

Each of these registers represents the value required to scale the U or V level from 0 to 2.0 and the Y level from 0 to 1.5 of its initial level. The value of these 10 bits is calculated using the equation:

$$Y, U, or V Scalar Value = Scale Factor \times 512$$

Example:
Scale Factor = 1.18

$$Y, U, or V Scale Value = 1.18 \times 512 = 665.6$$
$$Y, U, or V Scale Value = 665 \text{ (rounded to nearest integer)}$$
$$Y, U, or V Scale Value = 1010011001_b$$

Address 5Ch, SD LSB Register = 15h
Address 5Dh, SD Y Scale Register = A6h
Address 5Eh, SD V Scale Register = A6h
Address 5Fh, SD U Scale Register = A6h

SD Hue Adjust Value
[Subaddress 60h]
The hue adjust value is used to adjust the hue on the composite and chroma outputs.

These 8 bits represent the value required to vary the hue of the video data, i.e., the variance in phase of the subcarrier during active video with respect to the phase of the subcarrier during the color burst. The ADV7300A/ADV7301A provide a range of ±22.5° increments of 0.17578125°. For normal operation (zero adjustment), this register is set to 80h. FFh and 00h represent the upper and lower limit (respectively) of adjustment attainable.

For a positive hue adjust value:

$$0.17578125° \times (HCR - 128)$$

Example:
To adjust the hue by +4°, write 97h to the Hue Adjust Value Register:

$$\frac{+4}{0.17578125} + 128 = 151 = 97h$$

where 151 is rounded to the nearest integer. To adjust the hue by –4°, write 69h to the Hue Adjust Value Register:

$$\frac{-4}{0.17578125} + 128 = 105 = 69h$$

where 105 is rounded to the nearest integer.

SD Brightness Control
[Subaddress 61h]
The brightness is controlled by adding a programmable setup level onto the scaled Y data. This brightness level may be added onto the scaled Y data. For NTSC with pedestal, the setup can vary from 0 IRE to 22.5 IRE. For NTSC without pedestal and PAL, the setup can vary from –7.5 IRE to +15 IRE.

The Brightness Control Register is an 8-bit wide register. Seven bits are used to control the brightness level. This brightness level can be a positive or negative value.

Example:
Standard: NTSC with pedestal. To add +20 IRE brightness level, write 28h to Address 61h, SD Brightness:

$$SD Brightness Value \text{ (hex)} = (IRE Value \times 2.015631)$$
$$28h = (20 \times 2.015631) = 40.31262$$

Standard: PAL. To add –7 IRE brightness level, write 72h to Address 61h, SD Brightness:

$$SD Brightness Value \text{ (hex)} = (IRE Value \times 2.015631)$$
$$0001110_b = (7 \times 2.015631) = 14.109417$$

0001110 into two's complement equals 1110010, or 72h.

SD Brightness Detect
[Subaddress 7Ah]
The ADV7300A/ADV7301A allows monitoring of the brightness level of the incoming video data. The Brightness Detect Register is a read-only register.

Double Buffering
[Subaddress 13h, Bit 7; Subaddress 48h, Bit 2]
Double buffered registers are updated once per field on the falling edge of the VSYNC signal. Double buffering improves the overall performance since modifications to register settings will not be made during active video but take effect on the start of the active video.

Double buffering can be activated on the following HD registers: HD Gamma A and Gamma B curves and HD CGMS Registers. Double buffering can be activated on the following SD Registers: SD Gamma A and Gamma B Curves, SD Y Scale, SD U Scale, SD V Scale, SD Brightness, SD Closed Captioning, and SD Macrovision Bits 5–0.

Table XVIII. Brightness Control Values

Setup Level— NTSC w/ Pedestal (IRE)	Setup Level— NTSC w/o Pedestal (IRE)	Setup Level— PAL (IRE)	SD Brightness Value
22.5	+15	+15	1Eh
15	+7.5	+7.5	0Fh
7.5	0	0	00h
0	–7.5	–7.5	71h

Values in the range from 3Fh to 44h might result in an invalid output signal.

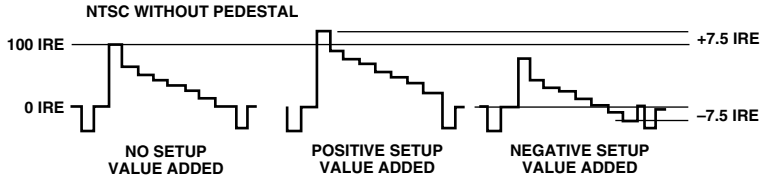


Figure 60. Examples for Brightness Control Values

Gamma Correction
[Subaddresses 21h–37h for HD;
Subaddresses 66h–79h for SD]

Gamma correction is available for SD and HD video. For each standard there are twenty 8-bit wide registers. They are used to program the Gamma Correction Curves A and B. HD Gamma Curve A is programmed at Addresses 0x24h–0x2Dh and HD Gamma Curve B at 0x2Eh–0x37h. SD Gamma Curve A is programmed at Addresses 0x66h–0x6Fh, and SD Gamma Curve B at Addresses 0x70h–0x79h.

Generally, gamma correction is applied to compensate for the nonlinear relationship between signal input and brightness level output (as perceived on the CRT). It can also be applied wherever nonlinear processing is used.

Gamma correction uses the function:

$$Signal_{OUT} = \left(Signal_{IN}\right)^{\gamma}$$

where γ equals the gamma power factor.

Gamma correction is performed on the luma data only. The user has the choice to use two different curves, Curve A or Curve B. At any one time only one of these curves can be used. The response of the curve is programmed at 10 predefined locations. In changing the values at these locations, the gamma curve can be modified. Between these points, linear interpolation is used to generate intermediate values. Considering the curve to have a total length of 256 points, the 10 locations are at: 24, 32, 48, 64, 80, 96, 128, 160, 192, and 224. Locations 0, 16, 240, and 255 are fixed and cannot be changed.

For the length of 16 to 240, the gamma correction curve must be calculated as:

$$y = x^{\gamma}$$

where y = gamma corrected output, x = linear input signal, and γ = the gamma power factor.

To program the gamma correction registers, the values for y must be calculated using the formula:

$$y_n = \left(\frac{x_{(n-16)}}{240-16}\right)^{\gamma} \times \left(240-16\right) + 16$$

where $x_{(n-16)}$ = the value for x along the x-axis at points n = 24, 32, 48, 64, 80, 96, 128, 160, 192, or 224, y_n = the value for y along the y-axis, which has to be written into the Gamma Correction Register.

Example:

$$y_{24} = \left(\left(\frac{8}{224}\right)^{0.5} \times 224\right) + 16 = 58\,*$$

$$y_{32} = \left(\left(\frac{16}{224}\right)^{0.5} \times 224\right) + 16 = 76\,*$$

$$y_{48} = \left(\left(\frac{32}{224}\right)^{0.5} \times 224\right) + 16 = 101\,*$$

$$y_{64} = \left(\left(\frac{48}{224}\right)^{0.5} \times 224\right) + 16 = 120\,*$$

$$y_{80} = \left(\left(\frac{64}{224}\right)^{0.5} \times 224\right) + 16 = 136\,*$$

$$y_{96} = \left(\left(\frac{80}{224}\right)^{0.5} \times 224\right) + 16 = 150\,*$$

$$y_{128} = \left(\left(\frac{112}{224}\right)^{0.5} \times 224\right) + 16 = 174\,*$$

$$y_{160} = \left(\left(\frac{144}{224}\right)^{0.5} \times 224\right) + 16 = 195\,*$$

$$y_{192} = \left(\left(\frac{176}{224}\right)^{0.5} \times 224\right) + 16 = 214\,*$$

$$y_{224} = \left(\left(\frac{208}{224}\right)^{0.5} \times 224\right) + 16 = 232\,*$$

The gamma curves shown in Figures 61 and 62 are examples. Any user-defined curve is acceptable in the range of 16–240.

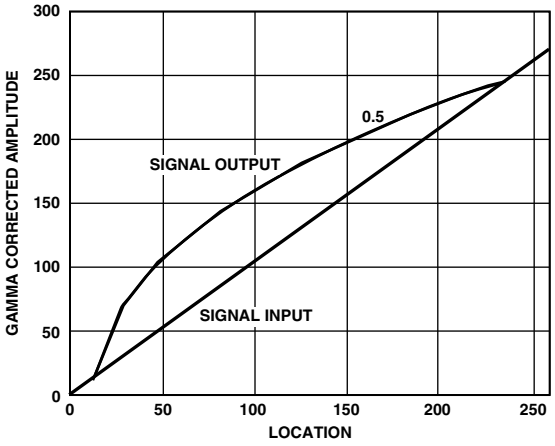


Figure 61. Signal Input (Ramp) and Signal Output for Gamma 0.5

*Rounded to the nearest integer

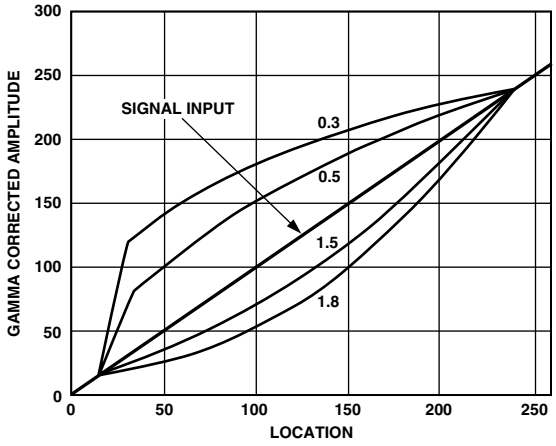


Figure 62. Signal Input (Ramp) and Selectable Gamma Output

HD SHARPNESS FILTER CONTROL AND ADAPTIVE FILTER CONTROL

[Subaddresses 20h and 38h-3Dh]

There are three filter modes available on the ADV7300A/ADV7301A: Sharpness Filter Mode and two adaptive filter modes.

HD Sharpness Filter Mode

To enhance or attenuate the Y signal in the frequency ranges shown in Figure 63, the following register settings must be used: HD Sharpness Filter must be enabled and HD Adaptive Filter Enable must be set to disabled.

To select one of the 256 individual responses, the corresponding gain values for each filter, which range from –8 to +7, must be programmed into the HD Sharpness Filter Gain Register at Address 0x20h.

HD Adaptive Filter Mode

The HD Adaptive Filter Threshold A, B, C Registers, the HD Adaptive Filter Gain 1, 2, and 3 Registers, and the HD Sharpness Filter Gain Register are used in Adaptive Filter Mode. To activate the adaptive filter control, the HD Sharpness Filter and HD Adaptive Filter Enable must be enabled.

The derivative of the incoming signal is compared to the three programmable threshold values: HD Adaptive Filter Threshold A, B, C. The recommended threshold range is from 16–235, although any value in the range of 0–255 can be used.

The edges can then be attenuated with the settings in HD Adaptive Filter Gain 1, 2, 3 Registers and HD Sharpness Filter Gain Register.

According to the settings of the HD Adaptive Filter Mode control, there are two adaptive filter modes available:

1. Mode A is used when Adaptive Filter Mode is set to "0." In this case, Filter B (LPF) will be used in the adaptive filter block. Also, only the programmed values for Gain B in the HD Sharpness Filter Gain, HD Adaptive Filter Gain 1, 2, 3 are applied when needed. The Gain A values are fixed and cannot be changed.
2. Mode B is used when Adaptive Filter Mode is set to "1." In this mode, a cascade of Filter A and Filter B is used. Both settings for Gain A and Gain B in the HD Sharpness Filter Gain, HD Adaptive Filter Gain 1, 2, 3 become active when needed.

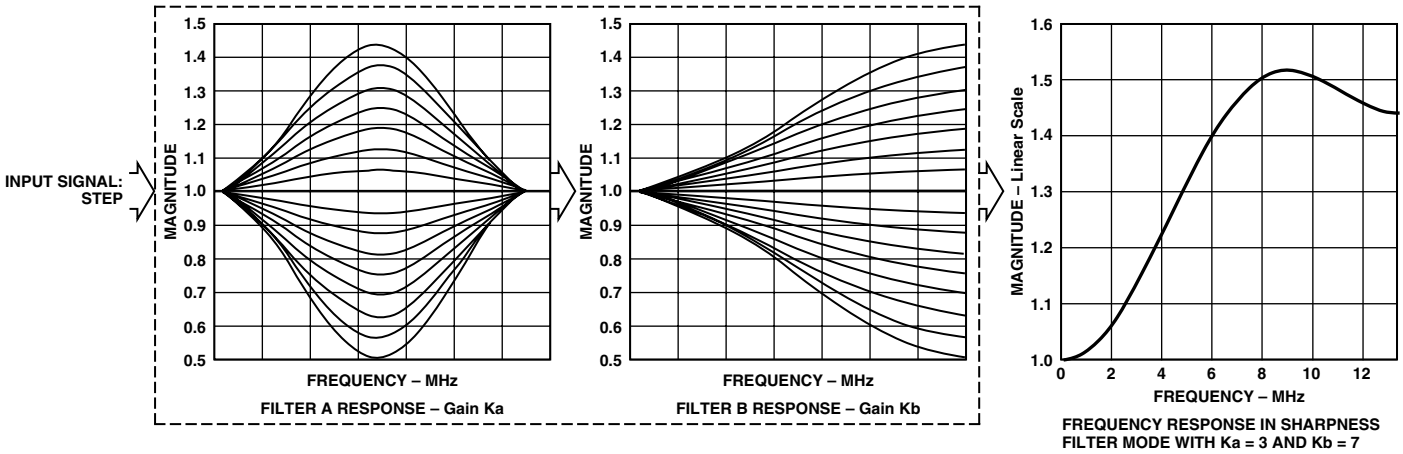


Figure 63. Sharpness and Adaptive Filter Control Block

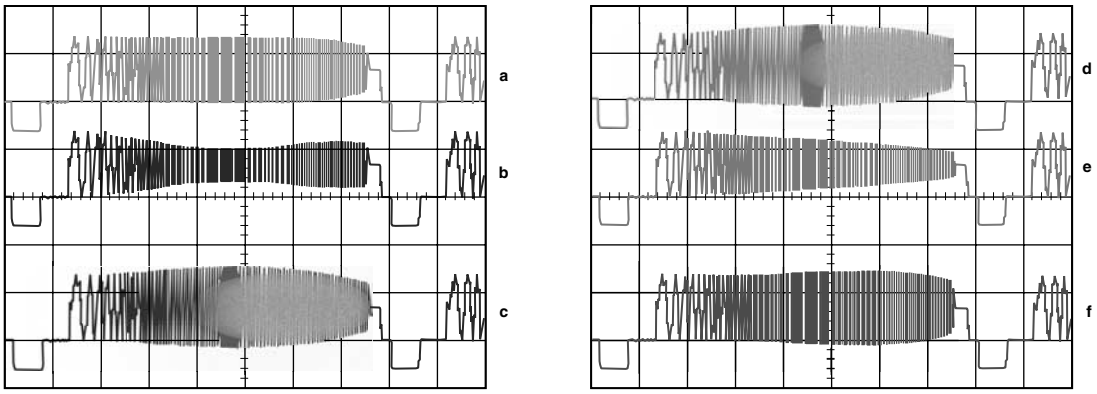


Figure 64. HD Sharpness Filter Control with Different Gain Settings for HD Sharpness Filter Gain Value

HD Sharpness Filter and Adaptive Filter Application Examples

HD Sharpness Filter Application

The HD sharpness filter can be used to enhance or attenuate the Y video output signal.

The register settings in Tables XIX and XX are used to achieve the results shown in Figure 64. Input data was generated by an external signal source.

Table XIX. Sharpness Filter on Frequency Sweep

Address	Register Setting	Reference*
00h	FCh	
01h	10h	
02h	20h	
10h	00h	
11h	81h	
20h	00h	a
20h	08h	b
20h	04h	c
20h	40h	d
20h	80h	e
20h	22h	f

*See Figure 64.

The effect of the sharpness filter can also be seen when using the internally generated crosshatch pattern.

Table XX. Sharpness Filter on Internal Test Pattern

Address	Register Setting
00h	FCh
01h	10h
02h	20h
10h	00h
11h	85h
20h	99h

In toggling the Sharpness Filter Enable Bit [Address 11h, Bit 8], it can be seen that the line contours of the crosshatch pattern change their sharpness.

Adaptive Filter Control Application

Figure 65 shows a typical signal to be processed by the adaptive filter control block.

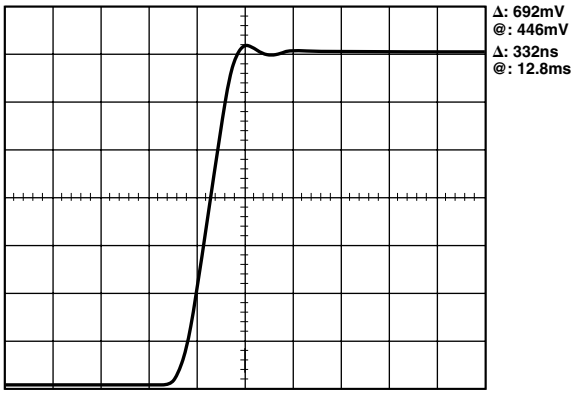


Figure 65. Input Signal to Adaptive Filter Control

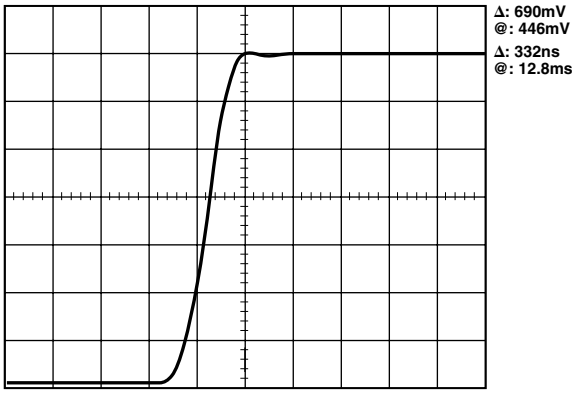


Figure 66. Output Signal After Adaptive Filter Control

The register settings in Table XXI are used to obtain the results shown in Figure 66, i.e., to remove the ringing on the Y signal. Input data was generated by an external signal source.

Table XXI. Adaptive Filter Control on Step Input Signal

Address	Register Setting
00h	FCh
01h	38h
02h	20h
10h	00h
11h	81h
15h	80h
20h	00h
38h	ACh
39h	9Ah
3Ah	88h
3Bh	28h
3Ch	3Fh
3Dh	64h

All other register settings are 00h.

When changing the Adaptive Filter Mode to Mode B [Address 15h, Bit 6], the output in Figure 67 can be obtained.

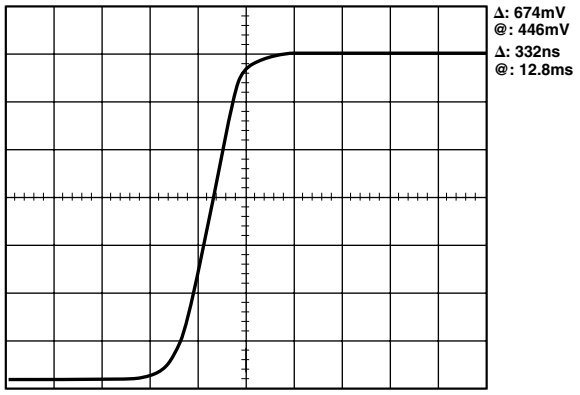


Figure 67. Output Signal from Adaptive Filter Control

The adaptive filter control can also be demonstrated using the internally generated crosshatch test pattern and toggling the Adaptive Filter Control Bit [Address 15h, Bit 7], shown in Table XXII.

Table XXII. Adaptive Filter Control on Internal Test Pattern

Address	Register Setting
00h	FCh
01h	38h
02h	20h
10h	00h
11h	85h
15h	80h
20h	00h
38h	ACh
39h	9Ah
3Ah	88h
3Bh	28h
3Ch	3Fh
3Dh	64h

SD DIGITAL NOISE REDUCTION
[Subaddresses 63h, 64h, and 65h]

DNR is applied to the Y data only. A filter block selects the high frequency, low amplitude components of the incoming signal (DNR input select). The absolute value of the filter output is compared to a programmable threshold value (DNR threshold control). There are two DNR modes available: DNR Mode and DNR Sharpness Mode.

In DNR Mode, if the absolute value of the filter output is smaller than the threshold, it is assumed to be noise. A programmable amount (coring gain border, coring gain data) of this noise signal will be subtracted from the original signal.

In DNR Sharpness Mode, if the absolute value of the filter output is less than the programmed threshold, it is assumed to be noise, as before. Otherwise, if the level exceeds the threshold, now being identified as a valid signal, a fraction of the signal (coring gain border, coring gain data) will be added to the original signal in order to boost high frequency components and to sharpen the video image.

In MPEG systems, it is common to process the video information in blocks of 8 × 8 pixels for MPEG2 systems or 16 × 16 pixels for MPEG1 systems (block size control). DNR can be applied to the resulting block transition areas that are known to contain noise. Generally, the block transition area contains two pixels. It is possible to define this area to contain four pixels (border area.)

It is also possible to compensate for variable block positioning or differences in YCrCb pixel timing with the use of the (DNR block offset.)

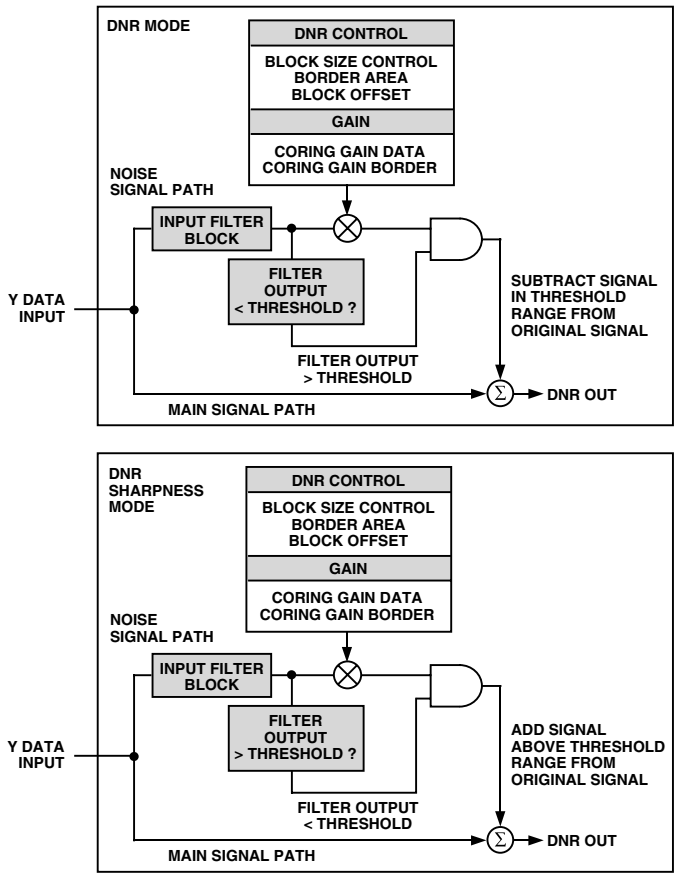


Figure 68. DNR Block Diagram

The Digital Noise Reduction Registers are three 8-bit-wide registers. They are used to control the DNR processing.

Coring Gain Border
[Address 63h, Bits 3–0]
These four bits are assigned to the gain factor applied to the border areas. In DNR Mode the range of gain values is 0–1, in increments of 0.125. This factor is applied to the DNR filter output that lies below the set threshold range. The result is then subtracted from the original signal.

In DNR Sharpness Mode, the range of gain values is 0 to 0.5, in increments of 0.0625. This factor is applied to the DNR filter output that lies above the threshold range. The result is added to the original signal.

Coring Gain Data
[Address 63h, Bits 7–4]
These four bits are assigned to the gain factor applied to the luma data inside the MPEG pixel block.

In DNR Mode, the range of gain values is 0–1, in increments of 0.125. This factor is applied to the DNR filter output that lies below the set threshold range. The result is then subtracted from the original signal.

In DNR Sharpness Mode, the range of gain values is 0–0.5, in increments of 0.0625. This factor is applied to the DNR filter output that lies above the threshold range. The result is added to the original signal.

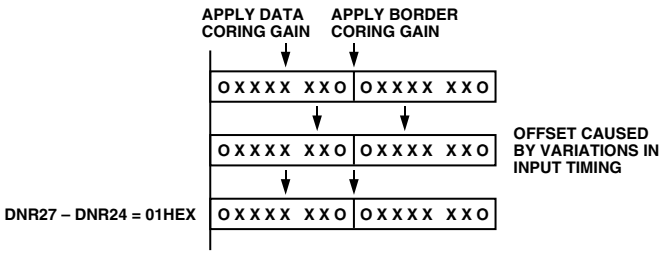


Figure 69. DNR Block Offset Control

DNR Threshold
[Address 64h, Bits 5–0]
These six bits are used to define the threshold value in the range of 0 to 63. The range is an absolute value.

Border Area
[Address 64h, Bit 6]
In setting this bit to a Logic "1," the block transition area can be defined to consist of four pixels. If this bit is set to a Logic "0," the border transition area consists of two pixels, where one pixel refers to two clock cycles at 27 MHz.

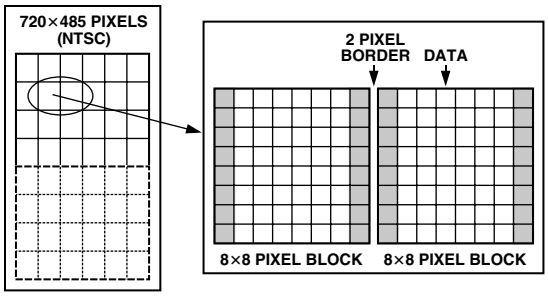


Figure 70. DNR Border Area

Block Size Control
[Address 64h, Bit 7]
This bit is used to select the size of the data blocks to be processed. Setting the block size control function to a Logic "1" defines a 16 × 16 pixel data block; a Logic "0" defines an 8 × 8 pixel data block, where one pixel refers to two clock cycles at 27 MHz.

DNR Input Select Control
[Address 65h, Bits 2–0]
Three bits are assigned to select the filter that is applied to the incoming Y data. The signal that lies in the pass band of the selected filter is the signal that will be DNR processed. The figure below shows the filter responses selectable with this control.

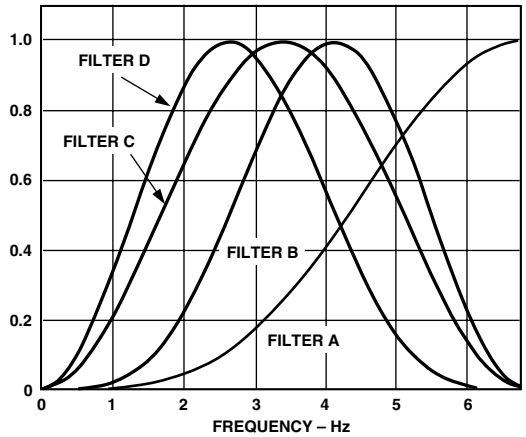


Figure 71. DNR Input Select

DNR Mode Control
[Address 65h, Bit 4]
This bit controls the DNR Mode selected. A Logic "0" selects DNR Mode, and a Logic "1" selects DNR Sharpness Mode. DNR works on the principle of defining low amplitude, high frequency signals as probable noise and subtracting this noise from the original signal.

In DNR Mode, it is possible to subtract a fraction of the signal that lies below the set threshold, assumed to be noise, from the original signal. The threshold is set in DNR Register 1.

When DNR Sharpness Mode is enabled, it is possible to add a fraction of the signal that lies above the set threshold to the original signal, since this data is assumed to be valid data and not noise. The overall effect is that the signal will be boosted (similar to using extended SSAF filter).

Block Offset Control
[Address 65h, Bits 7–4]
Four bits are assigned to this control that allow a shift of the data block of 15 pixels maximum. Consider the coring gain positions fixed. The block offset shifts the data in steps of one pixel such that the border coring gain factors can be applied at the same position regardless of variations in input timing of the data.

SD ACTIVE VIDEO EDGE

[Subaddress 42h, Bit 7]

When the active video edge is enabled, the first three pixels and the last three pixels of the active video, on the Luma Channel are scaled in such a way that maximum transitions on these pixels are not possible. The scaling factors are 1/8×, 1/2×, and 7/8×. All other active video passes through unprocessed.

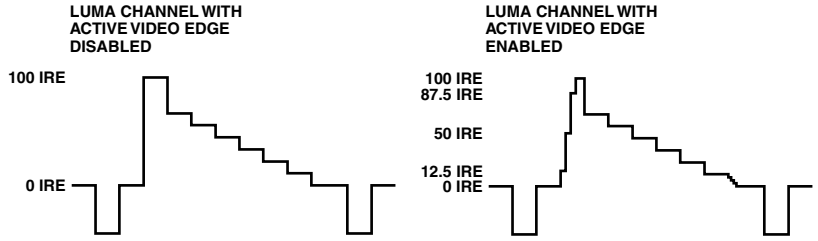


Figure 72. Active Video Edge Functionality Example

BOARD DESIGN AND LAYOUT CONSIDERATIONS

DAC Termination and Layout Considerations

The ADV7300A/ADV7301A contain an on-board voltage reference. The V_{REF} pin is normally terminated to V_{AA} through a 0.1 µF capacitor when the internal V_{REF} is used. Alternatively, the ADV7300A/ADV7301A can be used with an external V_{REF} (i.e., AD1580). The RSET resistors are connected between the R_{SET} pins and AGND and are used to control the full-scale output current and, therefore, the DAC voltage output levels. For full-scale output, R_{SET} must have a value of 760 Ω. The R_{SET} values should not be changed. R_{LOAD} has a value of 150 Ω for full-scale output.

Video Output Buffer and Optional Output Filter

Output buffering on all six DACs is necessary in order to drive output devices, such as SD or HD monitors. Analog Devices produces a range of suitable op amps for this application, for example the AD8061. More information on line driver buffering circuits is given in the relevant op amp data sheets.

An optional analog reconstruction LPF might be required as an antialias filter if the ADV7300A/ADV7301A is connected to a device that requires this filtering. The filter specifications vary with the application, see Table XXIII.

Table XXIII. External Filter Requirements

Input Mode	External Filter Oversampling	Cutoff Frequency	Attenuation
SD	2×	>6.5 MHz	–50 dB @ 20.5 MHz
SD	8×	>6.5 MHz	–50 dB @ 101.5 MHz
PS	1×	>12.5 MHz	–50 dB @ 14.5 MHz
PS	4×	>12.5 MHz	–50 dB @ 95.5 MHz
HDTV	1×	>30 MHz	–50 dB @ 44.25 MHz
HDTV	2×	>30 MHz	–50 dB @ 118.5 MHz

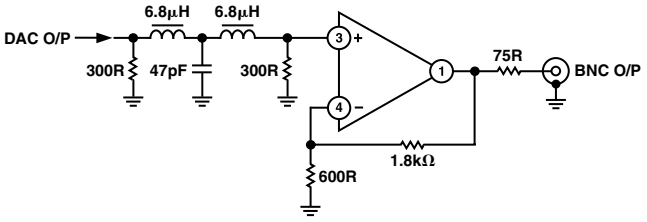


Figure 73. Example for Output Filter for SD, 8× Oversampling

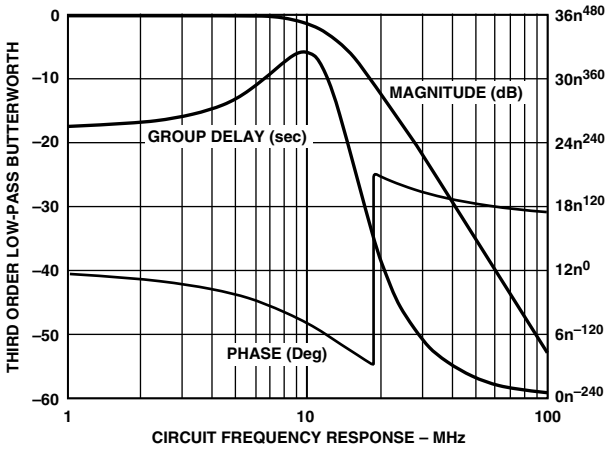


Figure 74. Filter Plot for Output Filter for SD, 8× Oversampling

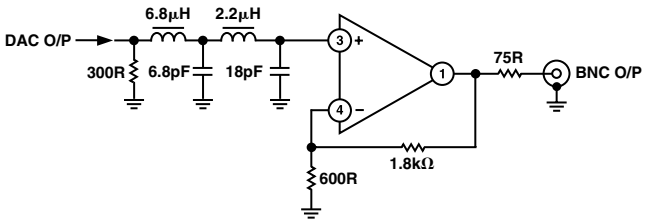


Figure 75. Example of Output for Output Filter for PS, 4× Oversampling

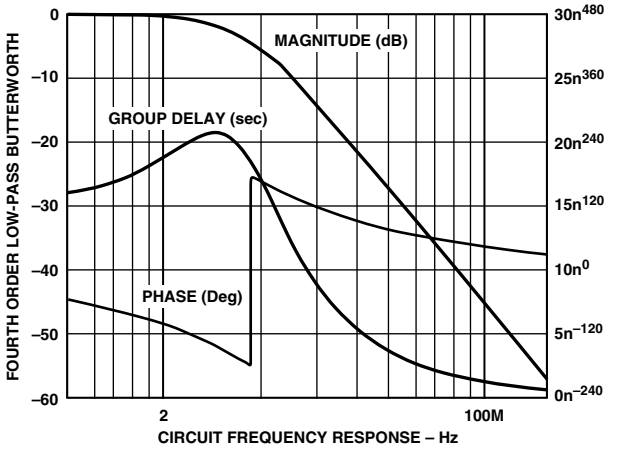


Figure 76. Filter Plot for Output Filter for PS, 4× Oversampling

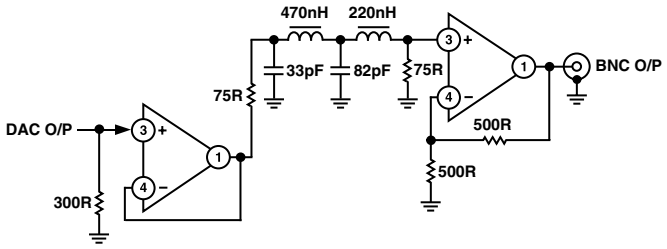


Figure 77. Example for Output Filter HDTV, 2× Oversampling

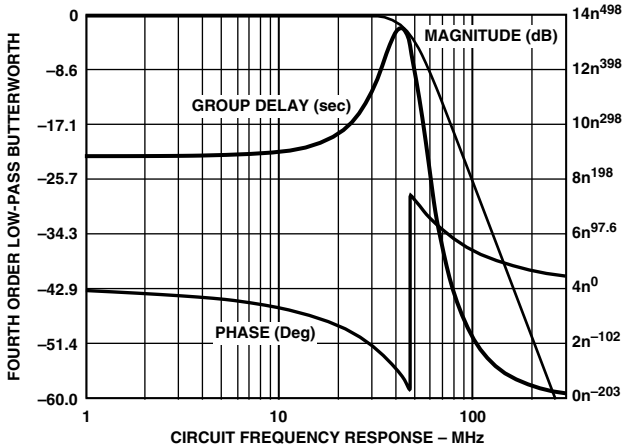


Figure 78. Filter Plot for Output Filter for HDTV, 2× Oversampling

Table XXIV. Possible Output Rates

Input Mode Addr 01h, Bits 6–4	PLL Addr 00h, Bit 1	Output Rate
SD	Off	27 MHz (2×)
	On	108 MHz (8×)
PS	Off	27 MHz (1×)
	On	108 MHz (4×)
HDTV	Off	74.25 MHz (1×)
	On	148.5 MHz (2×)
SD and	Off	27 MHz (2×)
	On	108 MHz (8×)
PS	Off	27 MHz (1×)
	On	108 MHz (4×)
SD* and	Off	27 MHz (2×)
	On	108 MHz (8×)
HDTV	Off	74.25 MHz (1×)
	On	74.25 MHz (1×)
SD and	Off	27 MHz (2×)
	On	27 MHz (2×)
HDTV*	Off	74.25 MHz (1×)
	On	148.5 MHz (2×)

*Oversampled

PCB Board Layout Considerations

The ADV7300A/ADV7301A is optimally designed for lowest noise performance, both radiated and conducted noise. To complement the excellent noise performance of the ADV7300A/ADV7301A, it is imperative that great care be given to the PC board layout. The layout should be optimized for the lowest noise on the ADV7300A/ADV7301A power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and AGND, V_{DD} and DGND, and V_{DD_IO} and GND_IO pins should be kept as short as possible to minimize inductive ringing.

It is recommended that a four-layer printed circuit board be used with power and ground planes separating the layer of the signal carrying traces of the components and solder side layer. Placement of components should take into account noisy circuits, such as crystal clocks, high speed logic circuitry, and analog circuitry.

There should be a separate analog ground plane and a separate digital ground plane.

Power planes should encompass a digital and an analog power plane. The analog power plane should contain the DACs and all associated circuitry, V_{REF} circuitry. The digital power plane should contain all logic circuitry. The analog and digital power planes should be individually connected to the common power plane at one single point through a suitable filtering device, such as a ferrite bead.

DAC output traces on a PCB should be treated as transmission lines. It is recommended that the DACs be placed as close as possible to the output connector, with the analog output traces being as short as possible (less than three inches). The DAC termination resistors should be placed as close as possible to the DAC outputs and should overlay the PCB's ground plane. As

well as minimizing reflections, short analog output traces will reduce noise pickup due to neighboring digital circuitry.

To avoid crosstalk between the DAC outputs, it is recommended to leave as much space as possible between the tracks of the individual DAC output pins.

Supply Decoupling

Noise on the analog power plane can be further reduced by the use of decoupling capacitors. Optimum performance is achieved by the use of 0.1 μF ceramic capacitors. Each of the group of V_{AA}, V_{DD}, or V_{DD_IO} pins should be individually decoupled to ground. This should be done by placing the capacitors as close as possible to the device with the capacitor leads as short as possible, thus minimizing lead inductance.

Digital Signal Interconnect

The digital signal lines should be isolated as much as possible from the analog outputs and other analog circuitry. Digital signal lines should not overlay the analog power plane. Due to the high clock rates used, long clock lines to the ADV7300A/ADV7301A should be avoided to minimize noise pickup. Any active pull-up termination resistors for the digital inputs should be connected to the digital power plane and not the analog power plane.

Analog Signal Interconnect

The ADV7300A/ADV7301A should be located as close as possible to the output connectors, thus minimizing noise pickup and reflections due to impedance mismatch. For optimum performance, the analog outputs should each be source and load terminated, as shown in Figure 79. The termination resistors should be as close as possible to the ADV7300A/ADV7301A to minimize reflections.

Any unused inputs should be tied to ground.

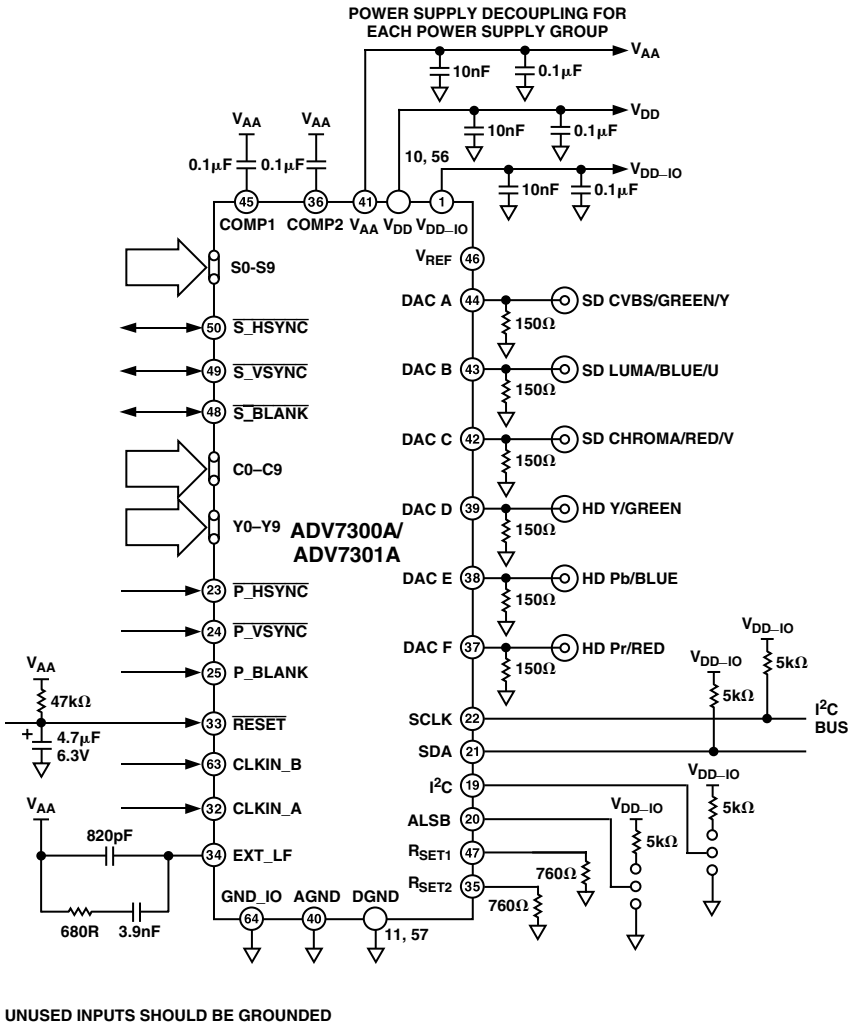


Figure 79. Circuit Layout

ADV7300A/ADV7301A

Appendix A

COPY GENERATION MANAGEMENT SYSTEM
HD CGMS DATA Registers 2–0
[Subaddress 12h]

HD CGMS is available in 525 p Mode only, conforming to "CGMS-A EIA-J CPR1204-1, Transfer Method of Video ID information using vertical blanking interval (525 p System), March 1998" and IEC61880, 1998, video systems (525/60)—video and accompanied data using the vertical blanking interval—analog interface.

When HD CGMS is enabled, CGMS data is inserted on Line 41. The HD CGMS Data Registers are to be found at Addresses 0x21h, 0x22h, and 0x23h.

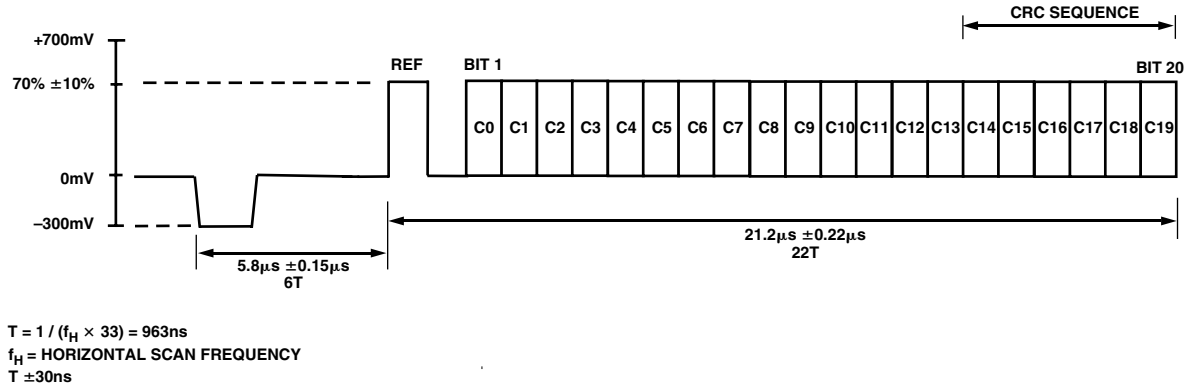


Figure 80. CGMS Waveform

SD CGMS Data Registers 2–0
{Subaddresses 59h, 5Ah, and 5Bh]

The ADV7300A/ADV7301A supports Copy Generation Management System (CGMS) conforming to the standard. CGMS data is transmitted on Line 20 of the odd fields and Line 283 of the even fields. Bits C/W05 and C/W06 control whether or not CGMS data is output on odd and even fields. CGMS data can only be transmitted when the ADV7300A/ADV7301A is configured in NTSC Mode. The CGMS data is 20 bits long; the function of each of these bits is as shown below. The CGMS data is preceded by a reference pulse of the same amplitude and duration as a CGMS bit, see Figure 81.

If SD CGMS CRC [Address 59h, Bit 4] is set to a Logic "1," the last six bits, C19–C14, that comprise the 6-bit CRC check sequence are calculated automatically on the ADV7300A/ADV7301A based on the lower 14 bits (C0–C13) of the data in the data registers and output with the remaining 14 bits to form the complete 20 bits of the CGMS data. The calculation of the CRC sequence is based on the polynomial:

$$x^6 + x + 1$$

with a preset value of 111111. If SD CGMS CRC [Address 59h, Bit 4] is set to a Logic "0," then all 20 bits (C0–C19) are output directly from the CGMS registers (no CRC calculated; must be calculated by the user).

Table XXV. Function of CGMS Bits

Word	Bit	Function	
0	B1	Aspect Ratio	0 = 4:3 1 = 16:9
	B2	Display Format	0 = Normal 1 = Letterbox
	B3	Undefined	
	B4–B6	Identification Information about Video and Other Signals (i.e., Audio)	
1	B7–B10	Identification Signal. Incidental to Word 0.	
2	B11–B14	Identification Signal and Information. Incidental to Word 0.	

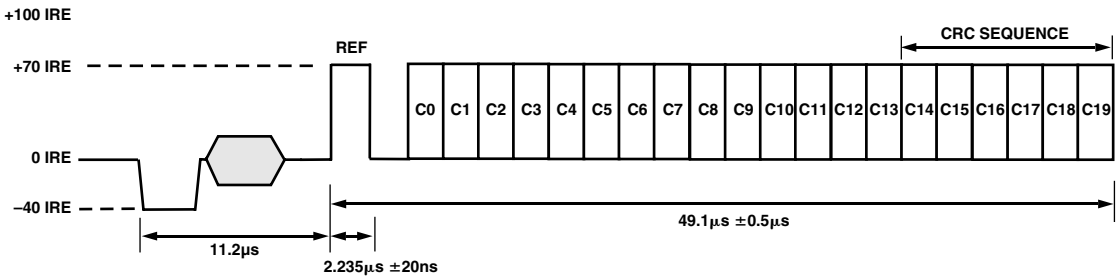


Figure 81. CGMS Waveform

Appendix B

SD WIDE SCREEN SIGNALLING
[Subaddresses 59h, 5Ah, and 5Bh]

The ADV7300A/ADV7301A supports Wide Screen Signalling (WSS) conforming to the standard. WSS data is transmitted on Line 23. WSS data can only be transmitted when the ADV7300A/ADV7301A is configured in PAL Mode. The WSS data is 14 bits long. The function of each of these bits is shown in Table XXVI. The WSS data is preceded by a run-in sequence and a start code (see Figure 82). If SD WSS [Address 59h, Bit 7] is set to a Logic "1," it enables the WSS data to be transmitted on Line 23. The latter portion of Line 23 (42.5 µs from the falling edge of HSYNC) is available for the insertion of video.

It is possible to blank the WSS portion of Line 23 with Subaddress 61h, Bit 7.

Table XXVI. Function of WSS Bits

Bit	Function
0	Aspect Ratio
1	Format
2	Position
3	Odd Parity Check of Bits 0–2
4	0 = Camera Mode 1 = Film Mode
5	0 = Standard Coding 1 = Motion Adaptive Color Plus
6	0 = No Helper 1 = Modulated Helper
7	Reserved
8	
9–10	00 = No Open Subtitles 10 = Subtitles Inside Active Image Area 01 = Subtitles Outside Active Image Area 11 = Reserved
11	0 = No Surround Sound Information 1 = Surround Sound Mode
12–13	Reserved

Table XXVII. Function of WSS Bits 0–3

B0	B1	B2	B3	Aspect Ratio	Format	Position
0	0	0	1	4:3	Full Format	N/A
1	0	0	0	14:9	Letterbox	Center
0	1	0	0	14:9	Letterbox	Top
1	1	0	1	16:9	Letterbox	Center
0	0	1	0	16:9	Letterbox	Top
1	0	1	1	>16:9	Letterbox	Center
0	1	1	1	14:9	Full Format	Center
1	1	1	0	16:9	N/A	N/A

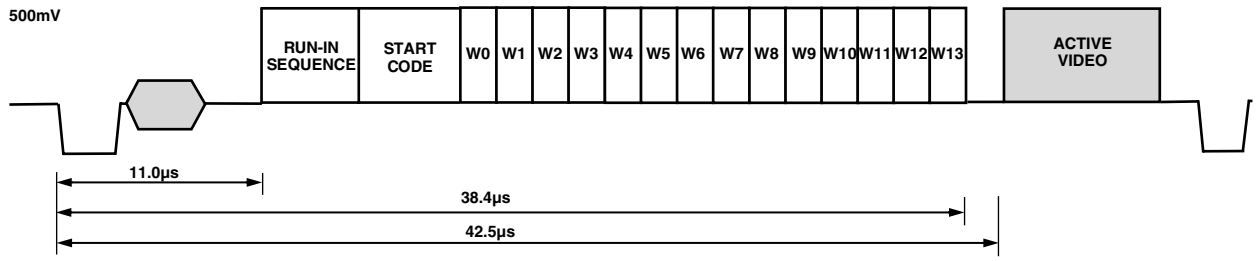


Figure 82. WSS Waveform

ADV7300A/ADV7301A

Appendix C

SD CLOSED CAPTIONING
[Subaddresses 51h–54h]

The ADV7300A/ADV7301A supports closed captioning conforming to the standard television synchronizing waveform for color transmission. Closed captioning is transmitted during the blanked active line time of Line 21 of the odd fields and Line 284 of the even fields.

Closed captioning consists of a seven cycle sinusoidal burst that is frequency and phase-locked to the caption data. After the clock run-in signal, the blanking level is held for 2 data bits and is followed by a Logic Level "1" start bit. Sixteen bits of data follow the start bit. These consist of two 8-bit bytes, 7 data bits, and 1 odd parity bit. The data for these bytes is stored in the SD Closed Captioning Registers [Addresses 53h–54h].

The ADV7300A/ADV7301A also supports the extended closed captioning operation that is active during even fields and is encoded on Line 284. The data for this operation is stored in the SD Closed Captioning Registers [Addresses 51h–52h].

All clock run-in signals and timing to support closed captioning on Lines 21 and 284 are generated automatically by the ADV7300A/ADV7301A. All pixels inputs are ignored during Lines 21 and 284 if closed captioning is enabled.

FCC Code of Federal Regulations (CFR) 47, Section 15.119 and EIA608 describe the closed captioning information for Lines 21 and 284.

The ADV7300A/ADV7301A uses a single buffering method. This means that the closed captioning buffer is only 1 byte deep; therefore, there will be no frame delay in outputting the closed captioning data unlike other 2 byte deep buffering systems. The data must be loaded one line before (Line 20 or Line 283) it is output on Line 21 and Line 284. A typical implementation of this method is to use $\overline{\text{VSYNC}}$ to interrupt a microprocessor that in turn will load the new data (2 bytes) every field. If no new data is required for transmission, "0" must be inserted in both data registers; this is called nulling. It is also important to load "control codes," all of which are double bytes on Line 21, or a TV will not recognize them. If there is a message like "Hello World" that has an odd number of characters, it is important to pad it out to even to get the "end of caption" 2-byte control code to land in the same field.

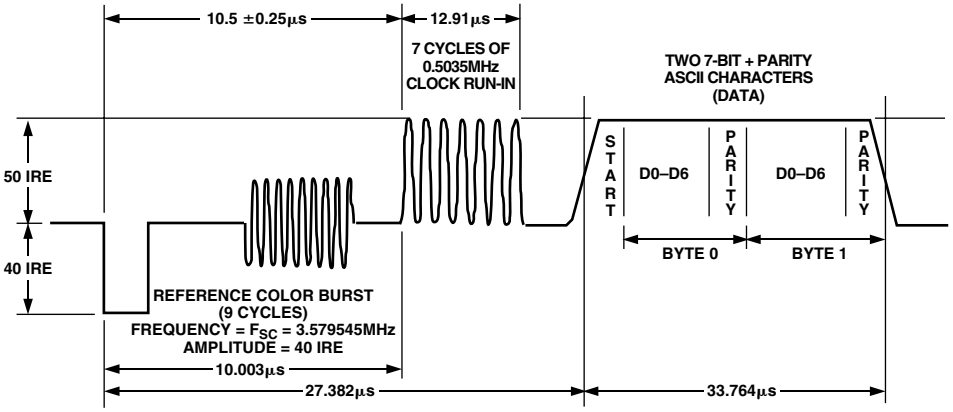


Figure 83. Closed Captioning Waveform, NTSC

Appendix D

TEST PATTERNS

The ADV7300A/ADV7301A can generate SD and HD test patterns.

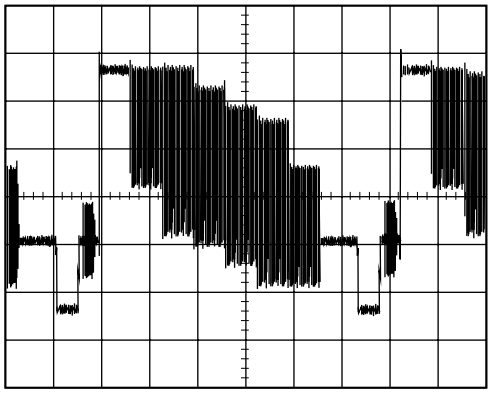


Figure 84. NTSC Color Bars

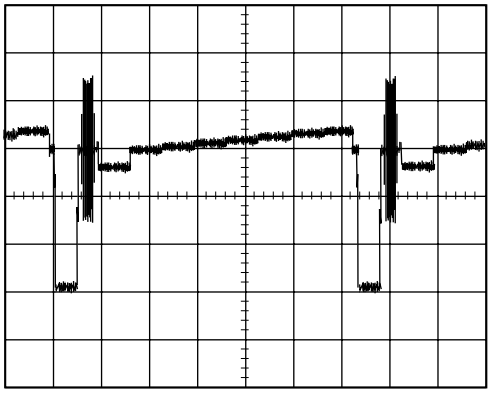


Figure 85. NTSC Black Bar (–21 mV, 0 mV, +3.5 mV, +7 mV, +10.5 mV, +14 mV, +18 mV, +23 mV)

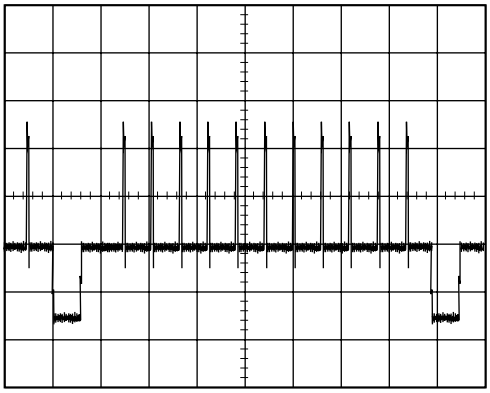


Figure 86. 525 p Hatch Pattern

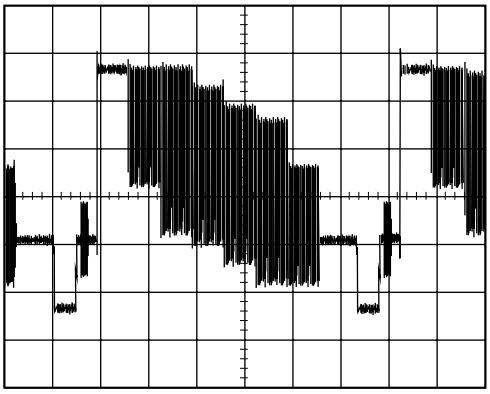


Figure 87. PAL Color Bars

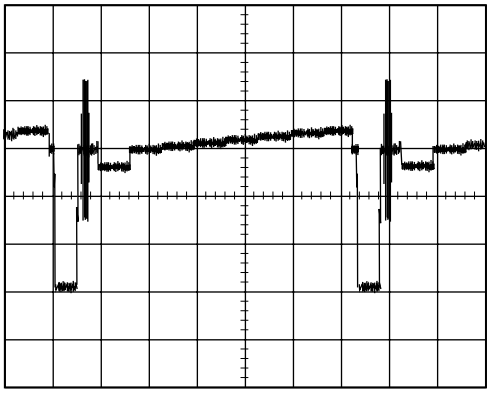


Figure 88. PAL Black Bar (–21 mV, 0 mV, +3.5 mV, +7 mV, +10.5 mV, +14 mV, +18 mV, +23 mV)

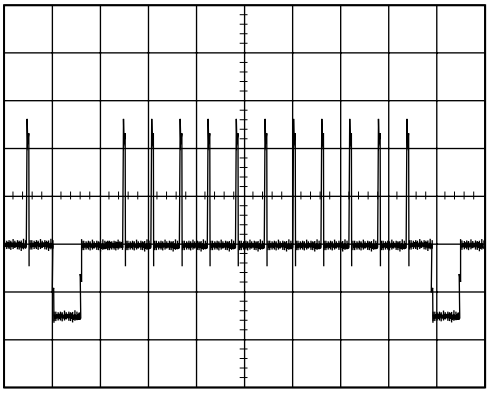


Figure 89. 625 p Hatch Pattern

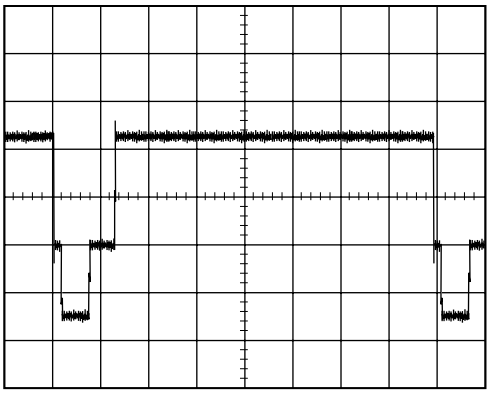


Figure 90. 525 p Field Pattern

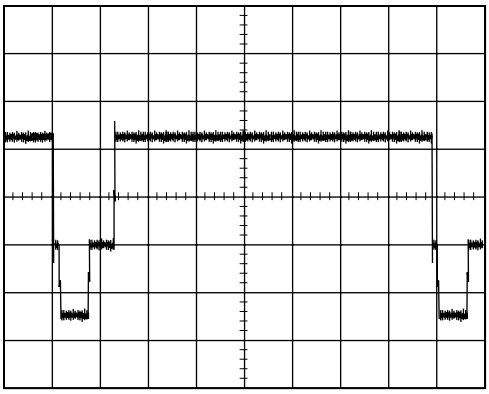


Figure 92. 625 p Field Pattern

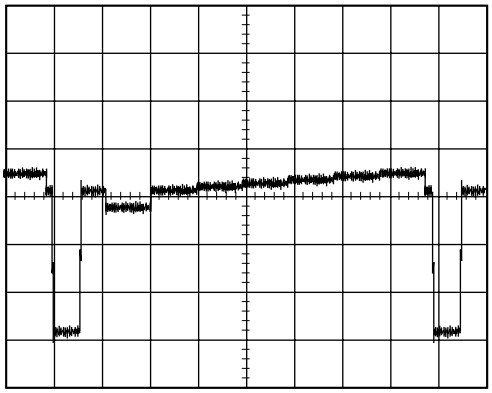


Figure 91. 525 p Black Bar (–35 mV, 0 mV, +7 mV, +14 mV, +21 mV, +28 mV, +35 mV)

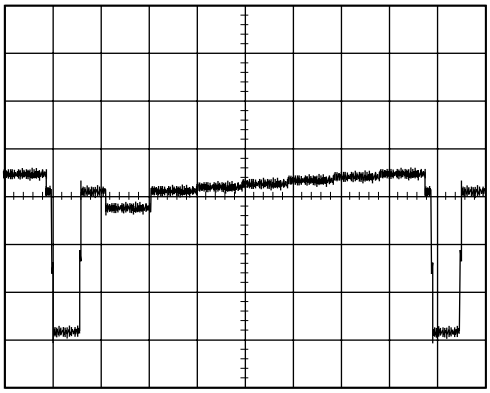


Figure 93. 625 p Black Bar (–35 mV, 0 mV, +7 mV, +14 mV, +21 mV, +28 mV, +35 mV)

Table XXVIII. NTSC CVBS Output on DAC A

Subaddress	Register Setting
00h	82h
11h	01h
40h	10h
42h	40h
44h	40h
4Ah	08h
4Ch	16h
4Dh	7Ch
4Eh	F0h
4Fh	21h

All other registers are set to 00h.

For PAL CVBS output on DAC A, the same settings in Table XXVIII are used except those listed in Table XXIX.

Table XXIX. PAL CVBS Output on DAC A

Subaddress	Register Setting
40h	11h
4Ch	CBh
4Dh	8Ah
4Eh	09h
4Fh	2Ah

Table XXX. NTSC Black Bar Pattern Output on DAC A

Subaddress	Register Setting
00h	82h
02h	04h
11h	01h
40h	10h
42h	40h
44h	40h
4Ah	08h
4Ch	16h
4Dh	7Ch
4Eh	F0h
4Fh	21h

All other registers are set to 00h. The Subcarrier Frequency Registers 4Ch–4Fh will be needed to generate the correct color burst signal.

For PAL Black Bar Pattern Output on DAC A, the same settings in Table XXX are used except those listed in Table XXXI.

Table XXXI. PAL Black Bar Pattern Output on DAC A

Subaddress	Register Setting
40h	11h
4Ch	CBh
4Dh	8Ah
4Eh	09h
4Fh	2Ah

Table XXXII. 525 p Hatch Pattern on DAC D

Subaddress	Register Setting
00h	12h
01h	10h
02h	20h
10h	40h
11h	05h
16h	A0h
17h	80h
18h	80h

All other registers are set to 00h.

For a 625 p Hatch Pattern on DAC D, the same settings in Table XXXII are used except for Subaddress 10h, which has a register setting of 50h.

Table XXXIII. 525 p Field Pattern*

Subaddress	Register Setting
00h	12h
01h	10h
02h	20h
10h	40h
11h	0Dh
16h	A0h
17h	80h
18h	80h

All other registers are set to 00h.
*See Figure 90.

For a 625 p Field Pattern on DAC D, the same settings in Table XXXIII are used except for Subaddress 10h, which has a register setting of 50h.

For a 525 p Black Bar Pattern Output on DAC D, the same settings in Table XXXIII are used except for Subaddresses 02h, which has a register setting of 24h.

For a 625 p Black Bar Pattern Output on DAC D, the same settings in Table XXXIII are used except for Subaddresses 02h and 10h, which have register settings of 24h and 50h, respectively.

ADV7300A/ADV7301A

Appendix E

SD TIMING MODES
[Subaddress 4Ah]
Mode 0 (CCIR-656): Slave Option
(Timing Register 0 TR0 = X X X X X 0 0 0)
The ADV7300A/ADV7301A is controlled by the start active video (SAV) and end active video (EAV) time codes in the pixel data. All timing information is transmitted using a 4-byte synchronization pattern. A synchronization pattern is sent immediately before and after each line during active picture and retrace. $\overline{\text{S\_VSYNC}}$, $\overline{\text{S\_HSYNC}}$, and $\overline{\text{S\_BLANK}}$ (if not used) pins should be tied high during this mode. Blank output is available.

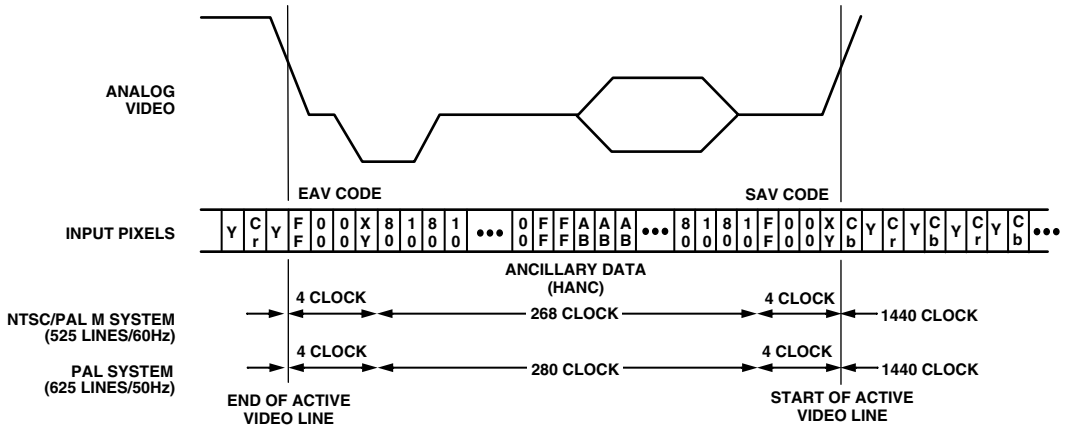


Figure 94. SD Slave Mode 0

Mode 0 (CCIR-656): Master Option
(Timing Register 0 TR0 = X X X X X 0 0 1)
The ADV7300A/ADV7301A generates H, V, and F signals required for the SAV and EAV time codes in the CCIR-656 standard. The H bit is output on the $\overline{\text{S\_HSYNC}}$ pin, the V bit is output on the $\overline{\text{S\_BLANK}}$ pin, and the F bit is output on the $\overline{\text{S\_VSYNC}}$ pin.

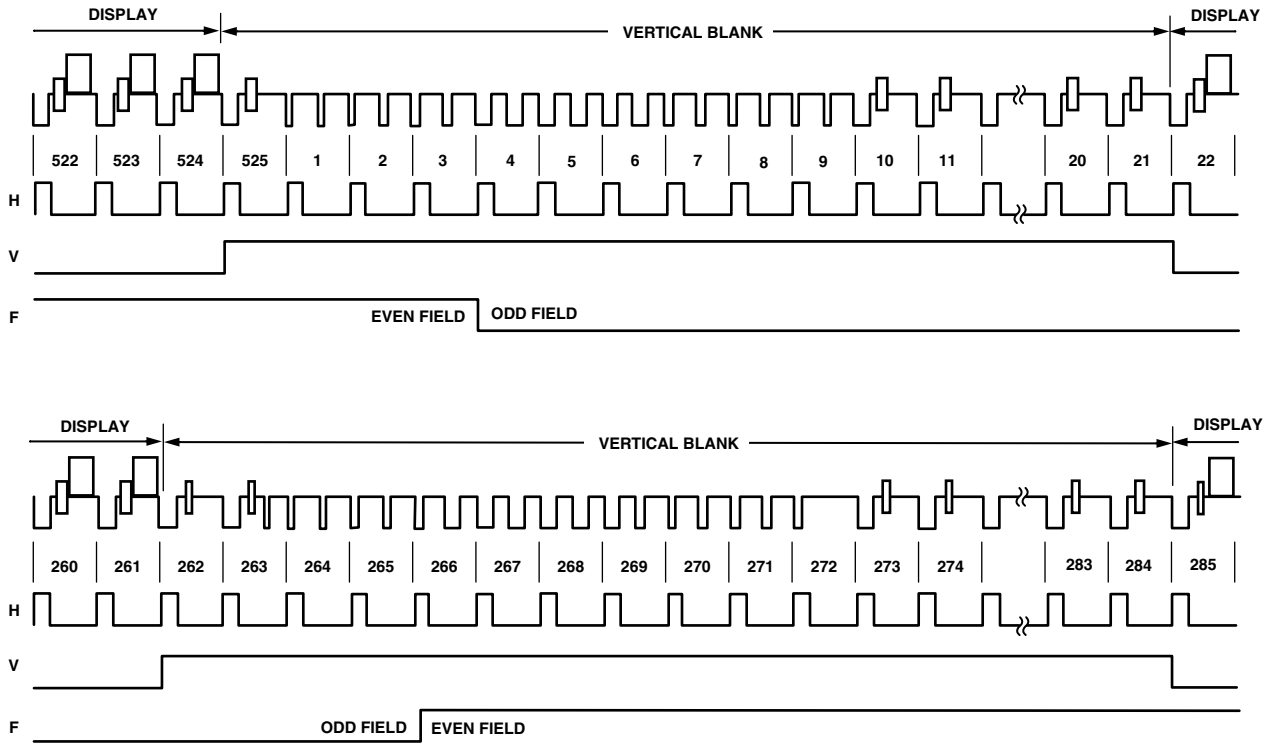


Figure 95. SD Master Mode 0, NTSC

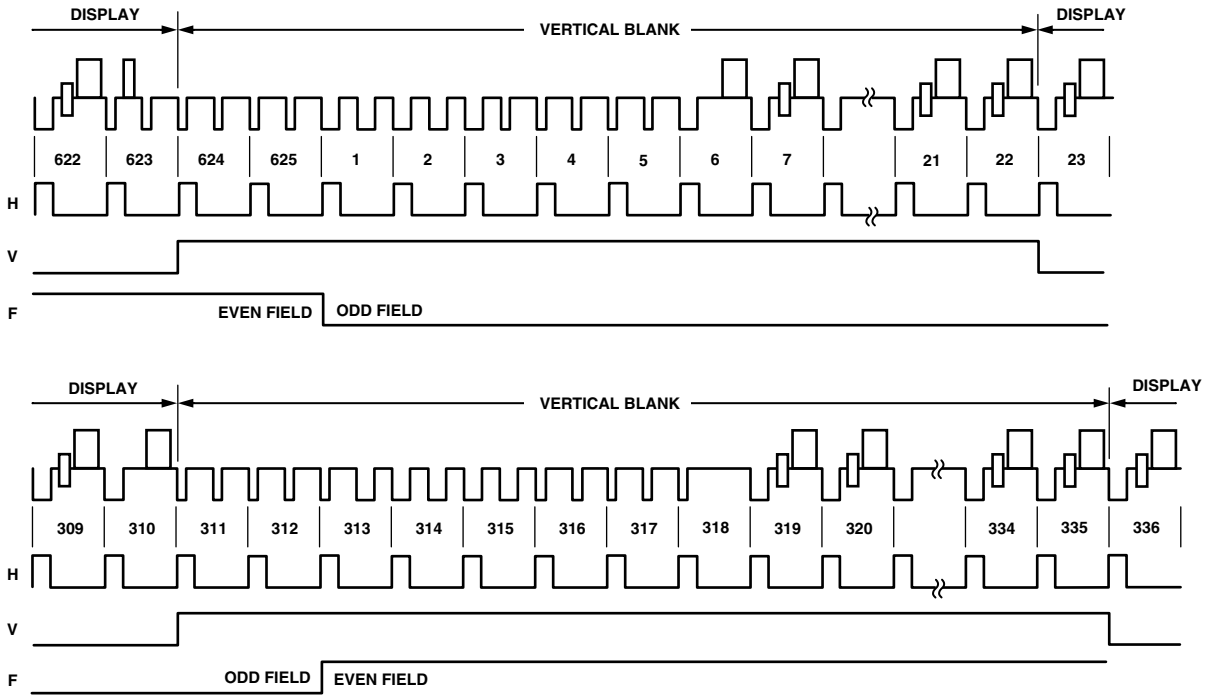


Figure 96. SD Master Mode 0, PAL

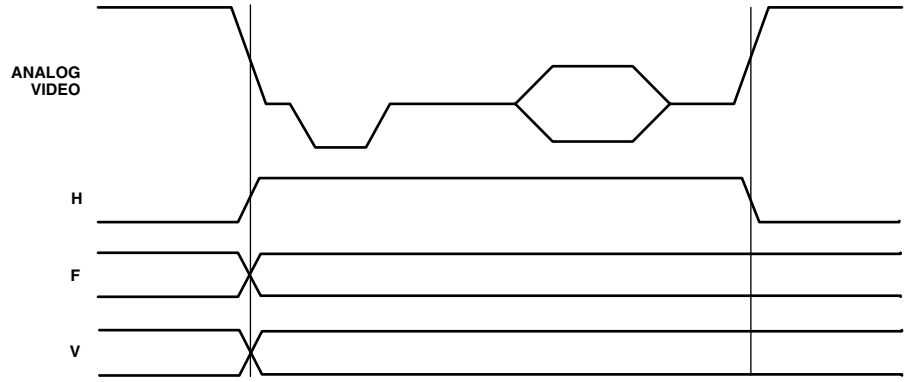


Figure 97. SD Master Mode 0 Data Transitions

Mode 1: Slave Option
HSYNC, BLANK, FIELD
(Timing Register 0 TR0 = X X X X X 0 1 0)
In this mode, the ADV7300A/ADV7301A accepts horizontal SYNC and odd/even FIELD signals. A transition of the FIELD input when HSYNC is low indicates a new frame, i.e., vertical retrace. The BLANK signal is optional. When the BLANK input is disabled, the ADV7300A/ADV7301A automatically blanks all normally blank lines as per CCIR-624. HSYNC is input on the S_HSYNC pin, BLANK on the S_BLANK pin, and FIELD on the S_VSYNC pin.

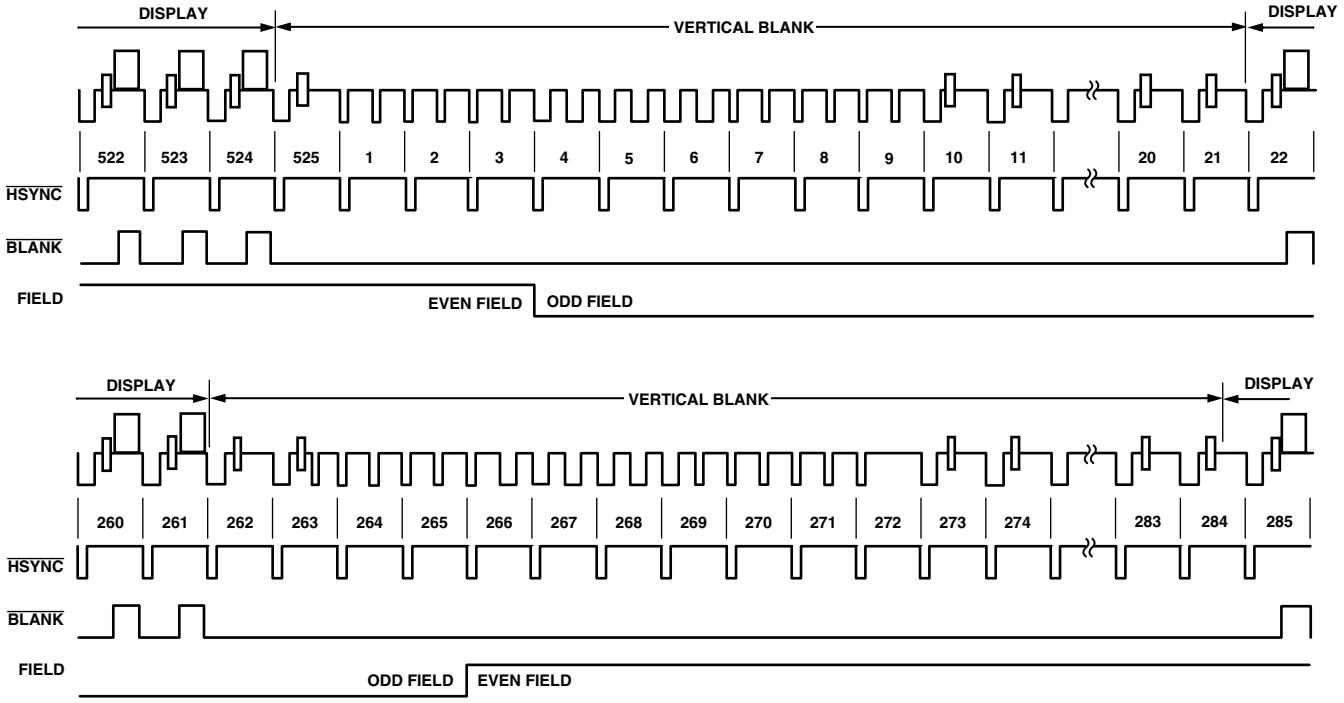


Figure 98. SD Slave Mode 1, NTSC

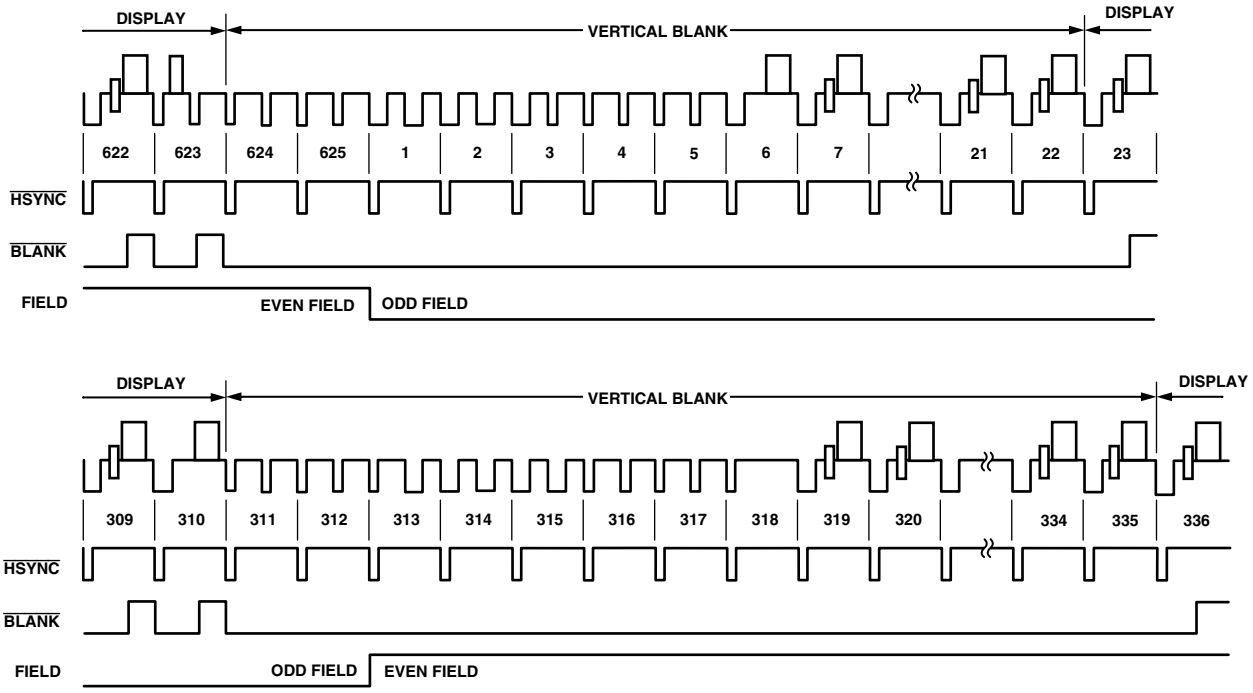


Figure 99. SD Slave Mode 1, PAL

Mode 1: Master Option
$\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, FIELD
(Timing Register 0 TR0 = X X X X X 0 1 1)
In this mode, the ADV7300A/ADV7301A can generate horizontal SYNC and odd/even FIELD signals. A transition of the FIELD input when $\overline{\text{HSYNC}}$ is low indicates a new frame, i.e., vertical retrace. The blank signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, the ADV7300A/ADV7301A automatically blanks all normally blank lines as per CCIR-624. Pixel data is latched on the rising clock edge following the timing signal transitions. $\overline{\text{HSYNC}}$ is output on the $\overline{\text{S\_HSYNC}}$ pin, $\overline{\text{BLANK}}$ on the $\overline{\text{S\_BLANK}}$ pin, and FIELD on the $\overline{\text{S\_VSYNC}}$ pin.

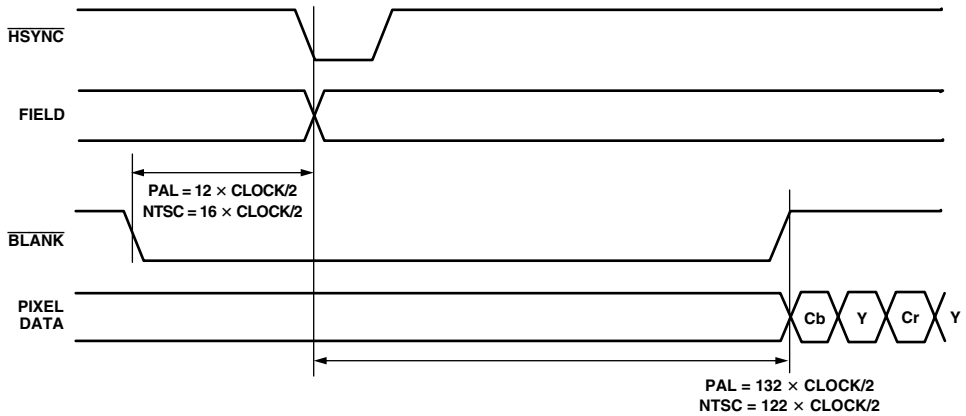


Figure 100. SD Timing Mode 1 Odd/Even Field Transitions, Master/Slave

Mode 2: Slave Option
HSYNC, VSYNC, BLANK
(Timing Register 0 TR0 = X X X X X 1 0 0)
In this mode, the ADV7300A/ADV7301A accepts horizontal and vertical SYNC signals. A coincident low transition of both HSYNC and VSYNC inputs indicates the start of an odd field. A VSYNC low transition when HSYNC is high indicates the start of an even field. The BLANK signal is optional. When the BLANK input is disabled, the ADV7300A/ADV7301A automatically blanks all normally blank lines as per CCIR-624. HSYNC is input on the S_HSYNC pin, BLANK on the S_BLANK pin, and FIELD on the S_VSYNC pin.

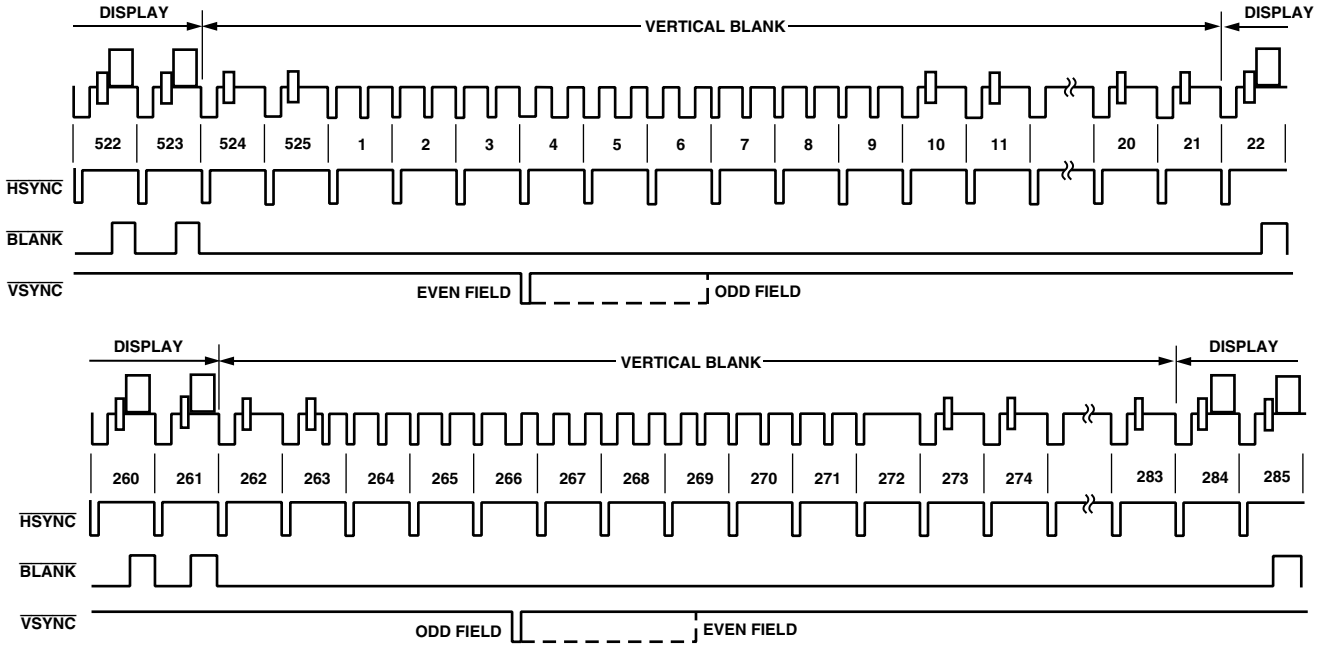


Figure 101. SD Slave Mode 2, NTSC

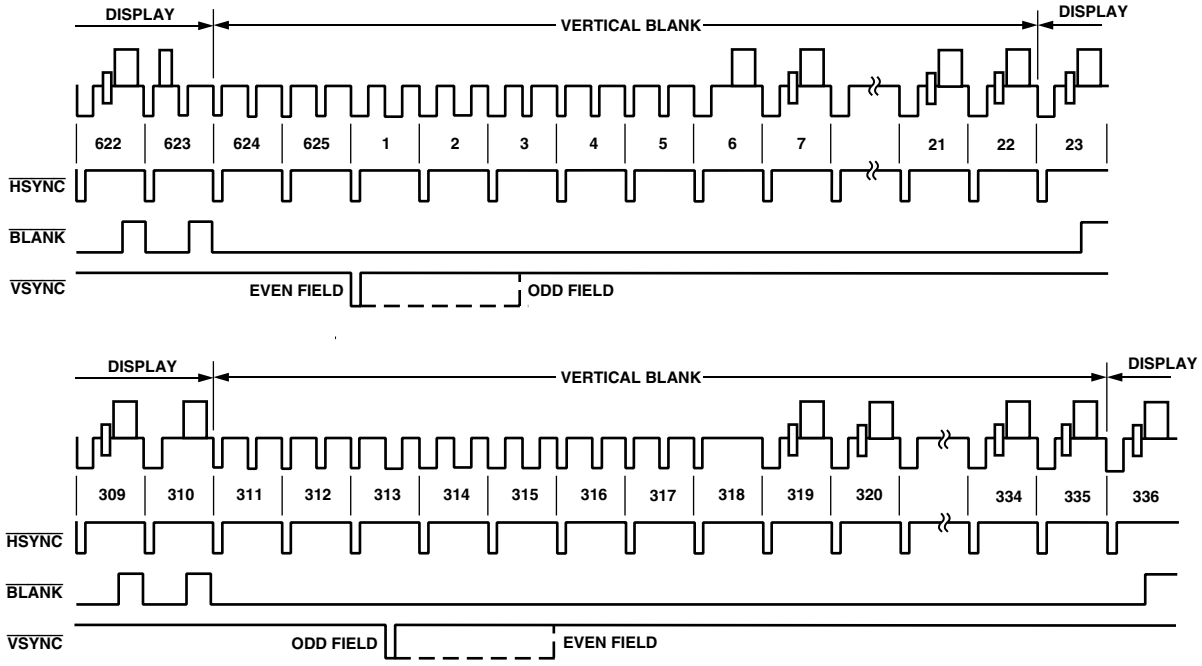


Figure 102. SD Slave Mode 2, PAL

Mode 2: Master Option
HSYNC, VSYNC, BLANK
(Timing Register 0 TR0 = X X X X X 1 0 1)
In this mode, the ADV7300A/ADV7301A can generate horizontal and vertical SYNC signals. A coincident low transition of both HSYNC and VSYNC inputs indicates the start of an odd field. A VSYNC low transition when HSYNC is high indicates the start of an even field. The BLANK signal is optional. When the BLANK input is disabled, the ADV7300A/ADV7301A automatically blanks all normally blank lines as per CCIR-624. HSYNC is output on the S_HSYNC pin, BLANK on the S_BLANK pin, and FIELD on the S_VSYNC pin.

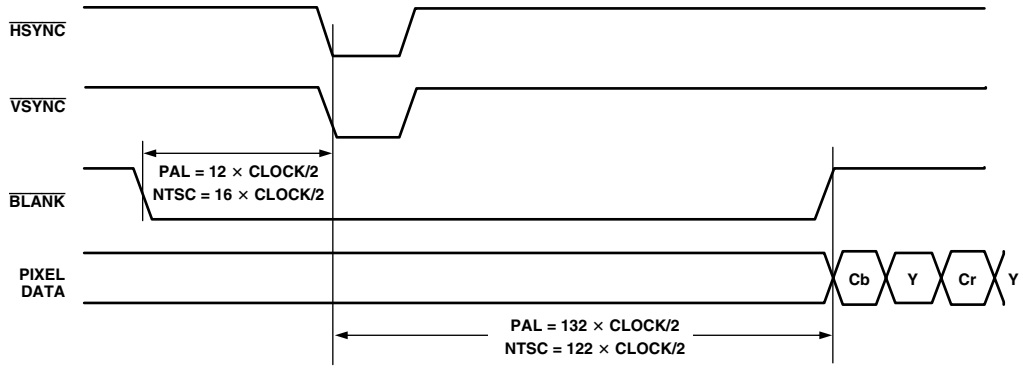


Figure 103. SD Timing Mode 2 Even to Odd Field Transition, Master/Slave

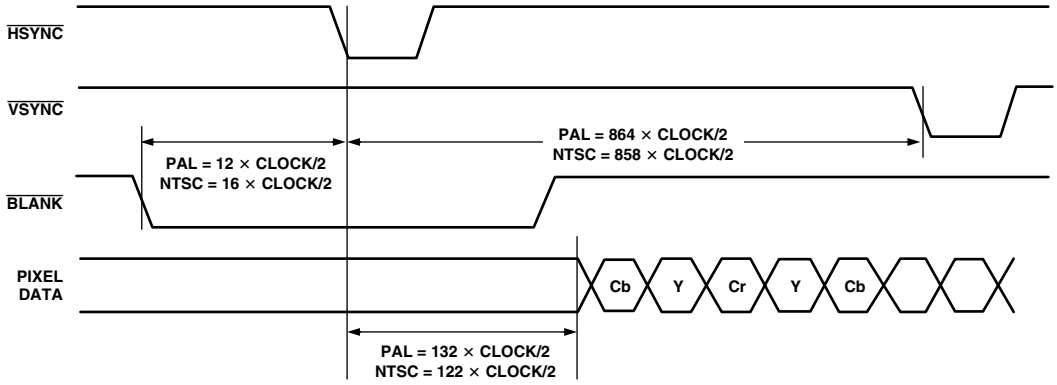


Figure 104. SD Timing Mode 2 Odd to Even Field Transition, Master/Slave

Mode 3: Master/Slave Option
HSYNC, BLANK, FIELD
(Timing Register 0 TR0 = X X X X X 1 1 0 or X X X X X 1 1 1)
In this mode, the ADV7300A/ADV7301A accepts or generates horizontal SYNC and odd/even FIELD signals. A transition of the FIELD input when HSYNC is high indicates a new frame, i.e., vertical retrace. The BLANK signal is optional. When the BLANK input is disabled, the ADV7300A/ADV7301A automatically blanks all normally blank lines as per CCIR-624. HSYNC is interfaced on the S_HSYNC pin, BLANK on the S_BLANK pin, and FIELD on the S_VSYNC pin.

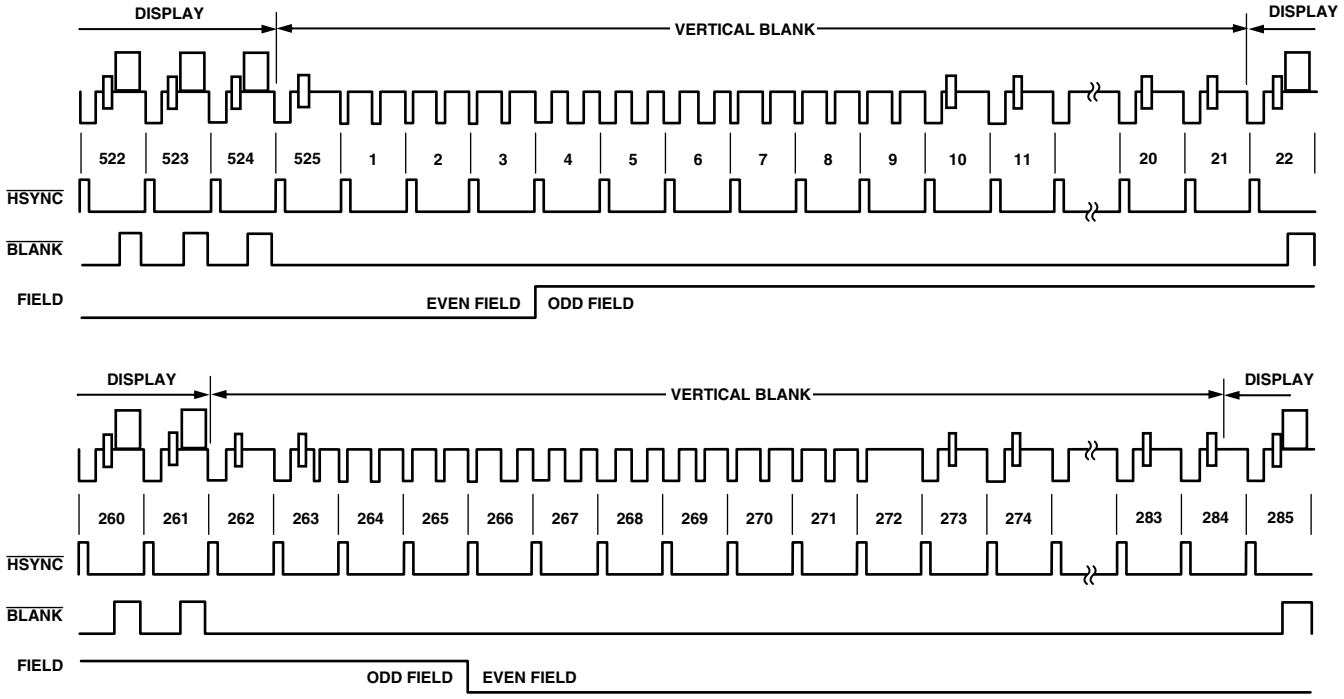


Figure 105. SD Timing Mode 3, NTSC

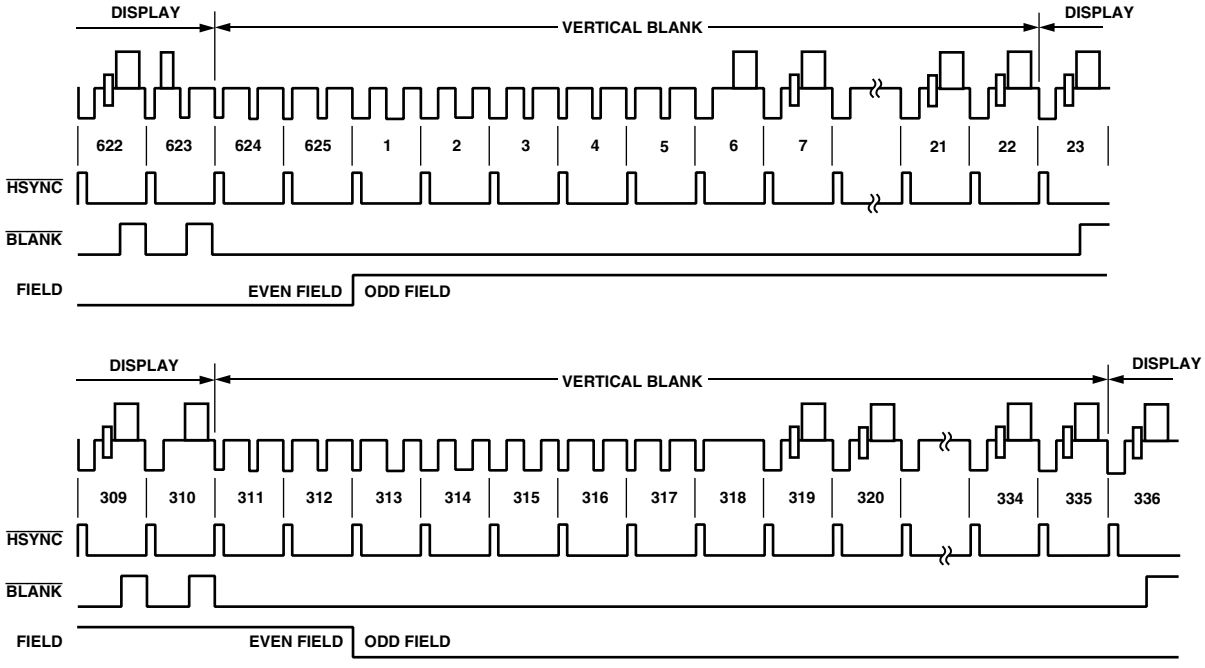


Figure 106. SD Timing Mode 3, PAL

Appendix F

VIDEO OUTPUT LEVELS

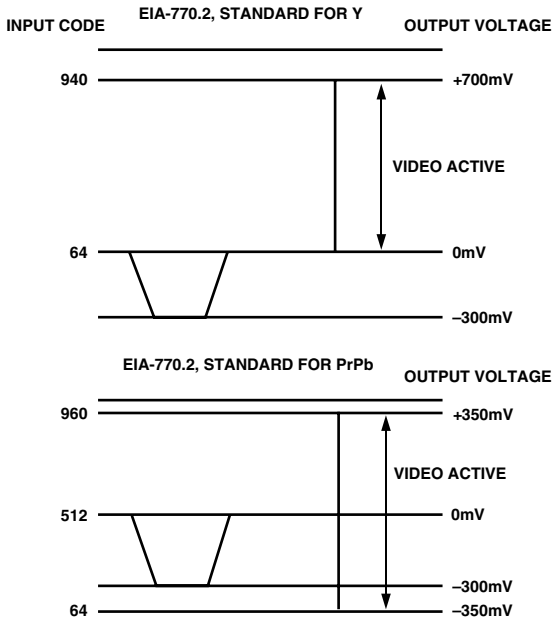


Figure 107. EIA-770.2 Standard Output Signals (525 p)

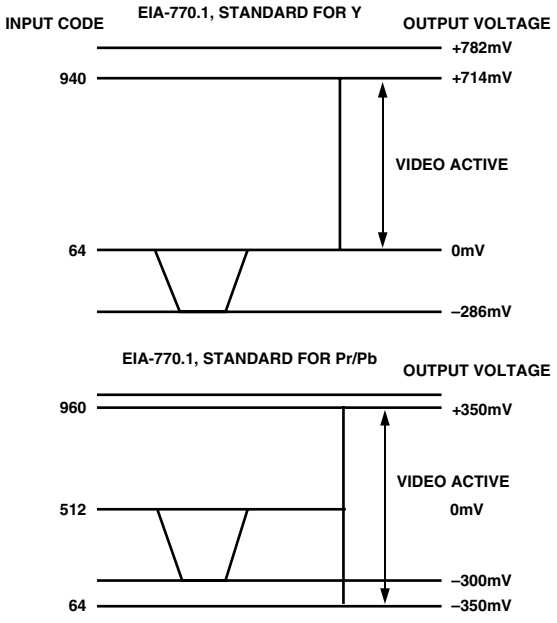


Figure 108. EIA-770.1 Standard Output Signals (525 p)

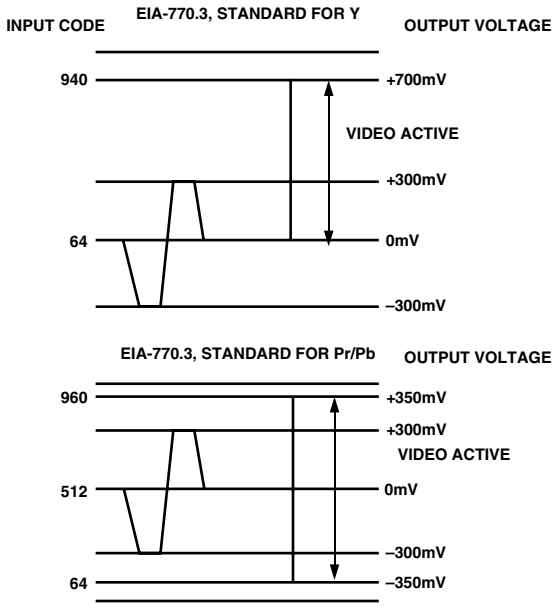


Figure 109. EIA-770.3 Standard Output Signals (1080 i, 720 p)

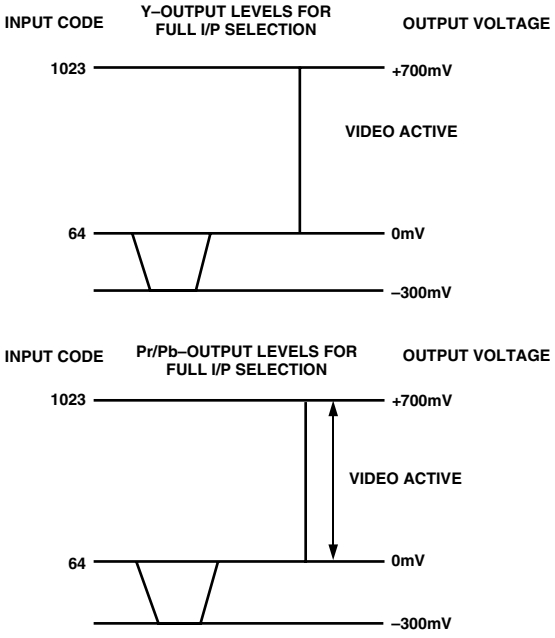
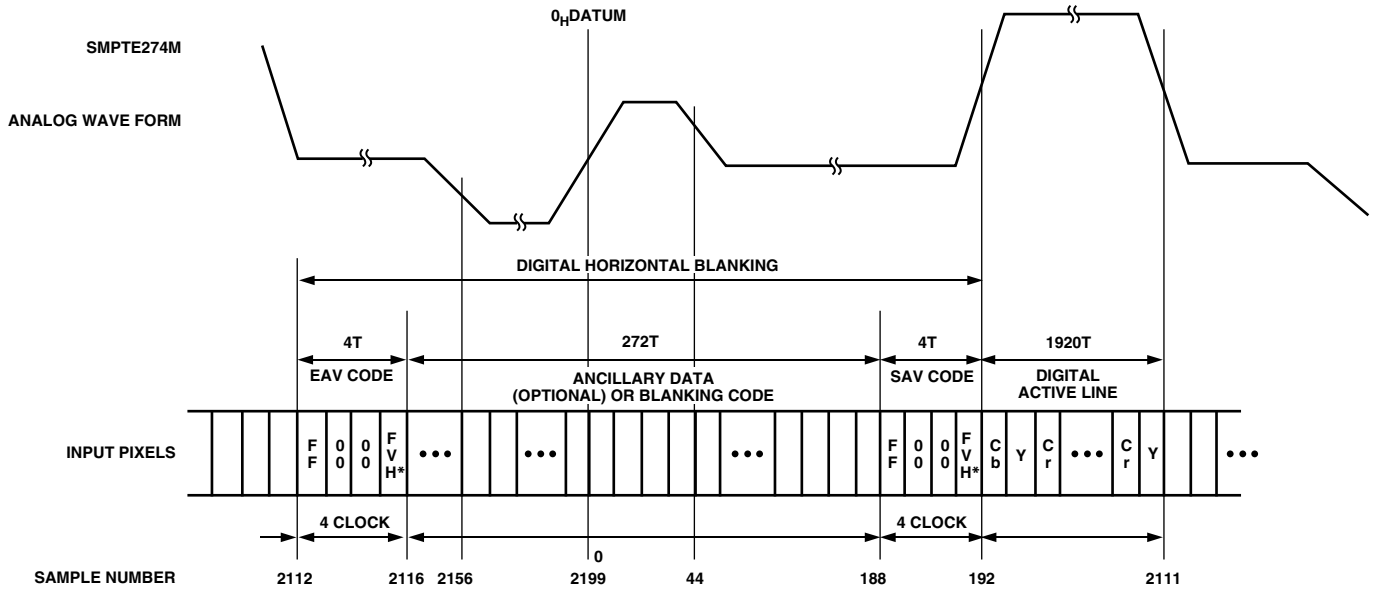


Figure 110. Output Levels for Full Input Selection

ADV7300A/ADV7301A

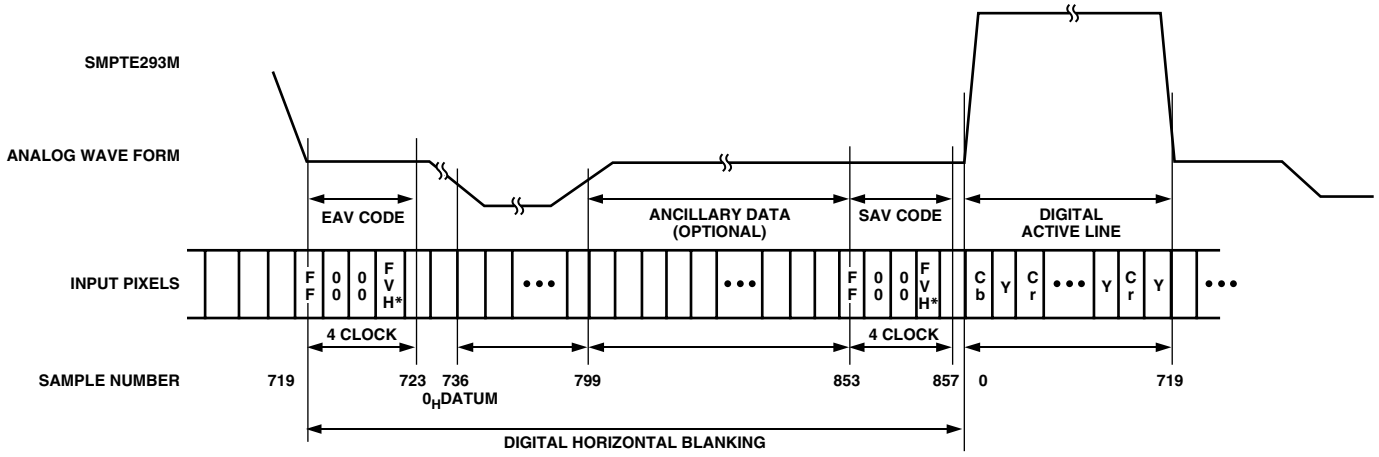
Appendix G

VIDEO STANDARDS



FVH* = FVH AND PARITY BITS
SAV/EAV: LINE 1-562: F = 0
SAV/EAV: LINE 563-1125: F = 1
SAV/EAV: LINE1-20; 561-583; 1124-1125: V = 1
SAV/EAV: LINE 21-560; 584-1123: V = 0

Figure 111. EAV/SAV Input Data Timing Diagram, SMPTE274M



FVH* = FVH AND PARITY BITS
SAV: LINE 43-525 = 200H
SAV: LINE 1-42 = 2AC
EAV: LINE43-525 = 274H
EAV: LINE 1-42 = 2D8

Figure 112. EAV/SAV Input Data Timing Diagram, SMPTE293M

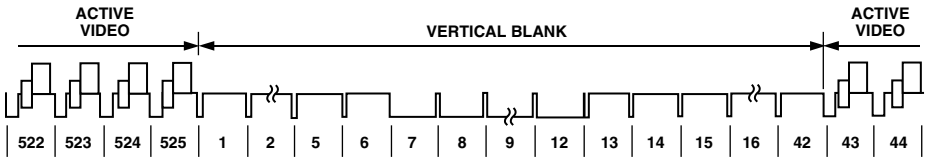


Figure 113. SMPTE293M

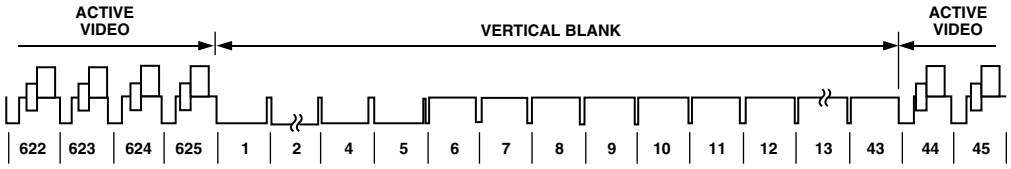


Figure 114. ITU-R.BT1358 (625 p)

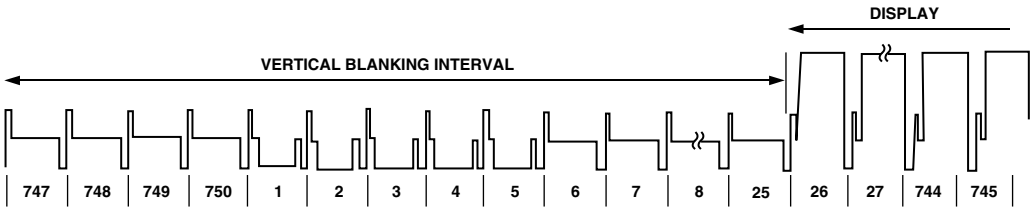


Figure 115. SMPTE296M (720 p)

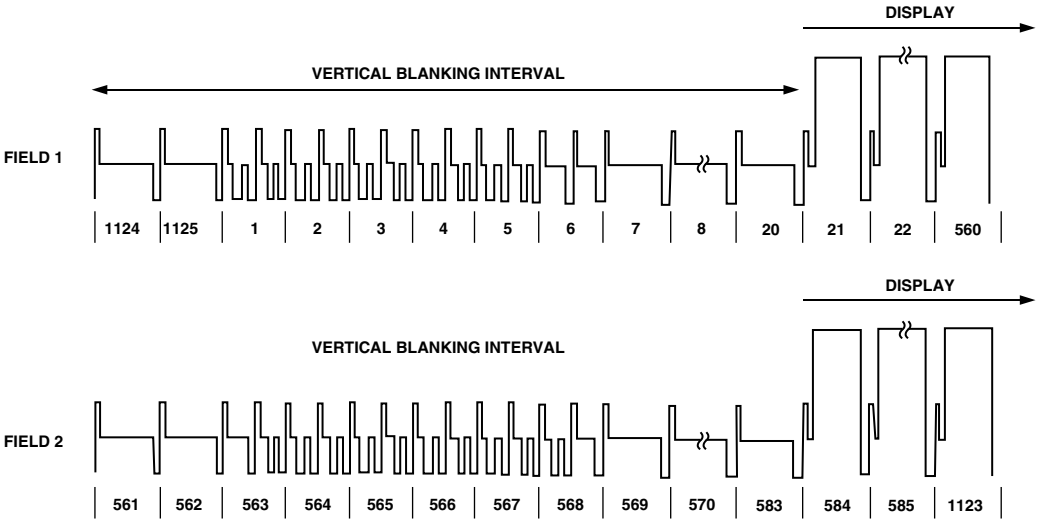
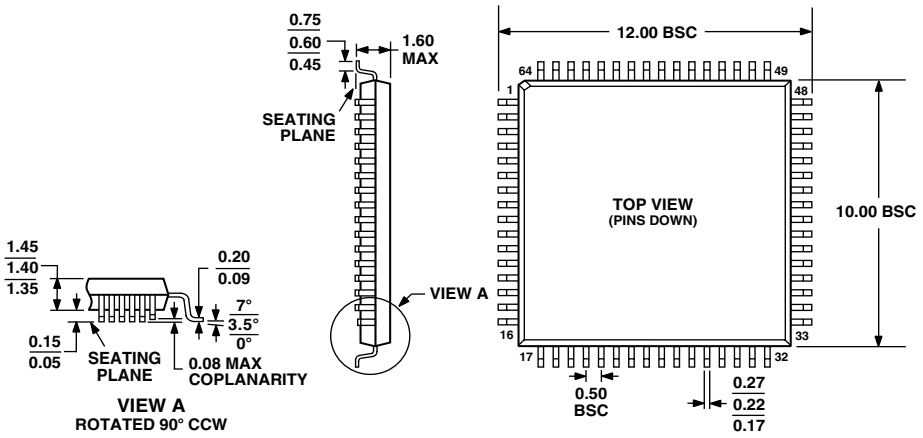


Figure 116. SMPTE274M (1080 i)

OUTLINE DIMENSIONS

Dimensions shown in millimeters

64-Lead Thin Plastic Quad Flatpack [LQFP]
(ST-64B)



COMPLIANT TO JEDEC STANDARDS MS-026BCD

C02861–0–9/02(A)

Revision History

Location	Page
9/02—Data Sheet changed from REV. 0 to REV. A.	
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Changes to TIMING SPECIFICATIONS	5
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Changes to Table IV	18
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Changes to Figure 79	51
Updated OUTLINE DIMENSIONS	68

PRINTED IN U.S.A.

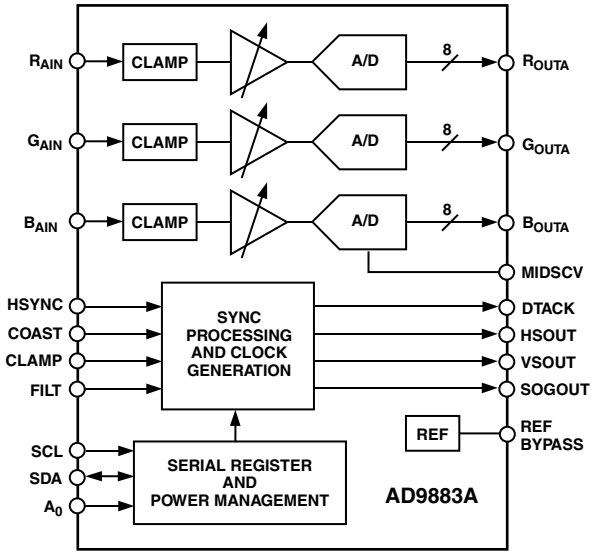
110 MSPS/140 MSPS Analog Interface for Flat Panel Displays

AD9883A

FEATURES
140 MSPS Maximum Conversion Rate
300 MHz Analog Bandwidth
0.5 V to 1.0 V Analog Input Range
500 ps p-p PLL Clock Jitter at 110 MSPS
3.3 V Power Supply
Full Sync Processing
Sync Detect for "Hot Plugging"
Midscale Clamping
Power-Down Mode
Low Power: 500 mW Typical
4:2:2 Output Format Mode

APPLICATIONS
RGB Graphics Processing
LCD Monitors and Projectors
Plasma Display Panels
Scan Converters
Microdisplays
Digital TV

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9883A is a complete 8-bit, 140 MSPS monolithic analog interface optimized for capturing RGB graphics signals from personal computers and workstations. Its 140 MSPS encode rate capability and full power analog bandwidth of 300 MHz supports resolutions up to SXGA (1280 × 1024 at 75 Hz).

The AD9883A includes a 140 MHz triple ADC with internal 1.25 V reference, a PLL, and programmable gain, offset, and clamp control. The user provides only a 3.3 V power supply, analog input, and Hsync and COAST signals. Three-state CMOS outputs may be powered from 2.5 V to 3.3 V.

The AD9883A's on-chip PLL generates a pixel clock from the Hsync input. Pixel clock output frequencies range from 12 MHz to 140 MHz. PLL clock jitter is 500 ps p-p typical at 140 MSPS. When the COAST signal is presented, the PLL maintains its output frequency in the absence of Hsync. A sampling phase adjustment is provided. Data, Hsync, and clock output phase relationships are maintained. The AD9883A also offers full sync processing for composite sync and sync-on-green applications.

A clamp signal is generated internally or may be provided by the user through the CLAMP input pin. This interface is fully programmable via a 2-wire serial interface.

Fabricated in an advanced CMOS process, the AD9883A is provided in a space-saving 80-lead LQFP surface-mount plastic package and is specified over the 0°C to 70°C temperature range.

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703

AD9883A–SPECIFICATIONS

Analog Interface (V_D = 3.3 V, V_{DD} = 3.3 V, ADC Clock = Maximum Conversion Rate unless otherwise noted.)

Parameter	Temp	Test Level	AD9883AKST-110 Min	AD9883AKST-110 Typ	AD9883AKST-110 Max	AD9883AKST-140 Min	AD9883AKST-140 Typ	AD9883AKST-140 Max	Unit
RESOLUTION				8			8		Bits
DC ACCURACY									
Differential Nonlinearity	25°C	I		±0.5	+1.25/–1.0		±0.5	+1.35/–1.0	LSB
	Full	VI			+1.35/–1.0			+1.45/–1.0	LSB
Integral Nonlinearity	25°C	I		±0.5	±1.85		±0.5	±2.0	LSB
	Full	VI			±2.0			±2.3	LSB
No Missing Codes	Full	VI		Guaranteed			Guaranteed		
ANALOG INPUT									
Input Voltage Range									
Minimum	Full	VI			0.5			0.5	V p-p
Maximum	Full	VI	1.0			1.0			V p-p
Gain Tempco	25°C	V		100			100		ppm/°C
Input Bias Current	25°C	IV			1			1	µA
	Full	IV			1			1	µA
Input Offset Voltage	Full	VI		7	50		7	70	mV
Input Full-Scale Matching	Full	VI		1.5	6.0		1.5	8.0	% FS
Offset Adjustment Range	Full	VI	46	49	52	46	49	52	% FS
REFERENCE OUTPUT									
Output Voltage	Full	VI	1.20	1.25	1.32	1.20	1.25	1.32	V
Temperature Coefficient	Full	V		±50			±50		ppm/°C
SWITCHING PERFORMANCE									
Maximum Conversion Rate	Full	VI	110				140		MSPS
Minimum Conversion Rate	Full	IV			10			10	MSPS
Data to Clock Skew	Full	IV	–0.5		+2.0	–0.5		+2.0	ns
t_{BUFF}	Full	VI	4.7			4.7			µs
t_{STAH}	Full	VI	4.0			4.0			µs
t_{DHO}	Full	VI	0			0			µs
t_{DAL}	Full	VI	4.7			4.7			µs
t_{DAH}	Full	VI	4.0			4.0			µs
t_{DSU}	Full	VI	250			250			ns
t_{STASU}	Full	VI	4.7			4.7			µs
t_{STOSU}	Full	VI	4.0			4.0			µs
HSYNC Input Frequency	Full	IV	15		110	15		110	kHz
Maximum PLL Clock Rate	Full	VI	110			140			MHz
Minimum PLL Clock Rate	Full	IV			12			12	MHz
PLL Jitter	25°C	IV		400	700[1]		400	700[1]	ps p-p
	Full	IV			1000[1]			1000[1]	ps p-p
Sampling Phase Tempco	Full	IV		15			15		ps/°C
DIGITAL INPUTS									
Input Voltage, High (V_{IH})	Full	VI	2.5			2.5			V
Input Voltage, Low (V_{IL})	Full	VI			0.8			0.8	V
Input Voltage, High (V_{IH})	Full	V			–1.0			–1.0	µA
Input Voltage, Low (V_{IL})	Full	V			+1.0			+1.0	µA
Input Capacitance	25°C	V		3			3		pF

Parameter	Temp	Test Level	AD9883AKST-110 Min	AD9883AKST-110 Typ	AD9883AKST-110 Max	AD9883AKST-140 Min	AD9883AKST-140 Typ	AD9883AKST-140 Max	Unit
DIGITAL OUTPUTS									
Output Voltage, High (V_{OH})	Full	VI	V_D – 0.1			V_D – 0.1			V
Output Voltage, Low (V_{OL})	Full	VI			0.1			0.1	V
Duty Cycle DATACK	Full	IV	45	50	55	45	50	55	%
Output Coding				Binary			Binary		
POWER SUPPLY									
V_D Supply Voltage	Full	IV	3.0	3.3	3.6	3.15	3.3	3.6	V
V_{DD} Supply Voltage	Full	IV	2.2	3.3	3.6	2.2	3.3	3.6	V
P_{VD} Supply Voltage	Full	IV	3.0	3.3	3.6	3.0	3.3	3.6	V
I_D Supply Current (V_D)	25°C	V		132			180		mA
I_{DD} Supply Current (V_{DD})[2]	25°C	V		19			26		mA
IP_{VD} Supply Current (P_{VD})	25°C	V		8			11		mA
Total Power Dissipation	Full	VI		525	650		650	800	mW
Power-Down Supply Current	Full	VI		5	10		5	10	mA
Power-Down Dissipation	Full	VI		16.5	33		16.5	33	mW
DYNAMIC PERFORMANCE									
Analog Bandwidth, Full Power	25°C	V		300			300		MHz
Transient Response	25°C	V		2			2		ns
Overvoltage Recovery Time	25°C	V		1.5			1.5		ns
Signal-to-Noise Ratio (SNR)	25°C	V		44			43		dB
(Without Harmonics)	Full	V		43			42		dB
f_{IN} = 40.7 MHz									
Crosstalk	Full	V		55			55		dBc
THERMAL CHARACTERISTICS									
θ_{JC} Junction-to-Case Thermal Resistance		V		16			16		°C/W
θ_{JA} Junction-to-Ambient Thermal Resistance		V		35			35		°C/W

NOTES
[1]VCO Range = 10, Charge Pump Current = 110, PLL Divider = 1693.
[2]DATACK Load = 15 pF, Data Load = 5 pF.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_D	3.6 V
V_{DD}	3.6 V
Analog Inputs	V_D to 0.0 V
VREF IN	V_D to 0.0 V
Digital Inputs	5 V to 0.0 V
Digital Output Current	20 mA
Operating Temperature	–25°C to +85°C
Storage Temperature	–65°C to +150°C
Maximum Junction Temperature	150°C
Maximum Case Temperature	150°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

Test Level

I. 100% production tested.

II. 100% production tested at 25°C and sample tested at specified temperatures.

III. Sample tested only.

IV. Parameter is guaranteed by design and characterization testing.

V. Parameter is a typical value only.

VI. 100% production tested at 25°C; guaranteed by design and characterization testing.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9883AKST-140	0°C to 70°C	Thin Plastic Quad Flatpack	ST-80
AD9883AKST-110	0°C to 70°C	Thin Plastic Quad Flatpack	ST-80
AD9883A/PCB	25°C	Evaluation Board	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9883A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION

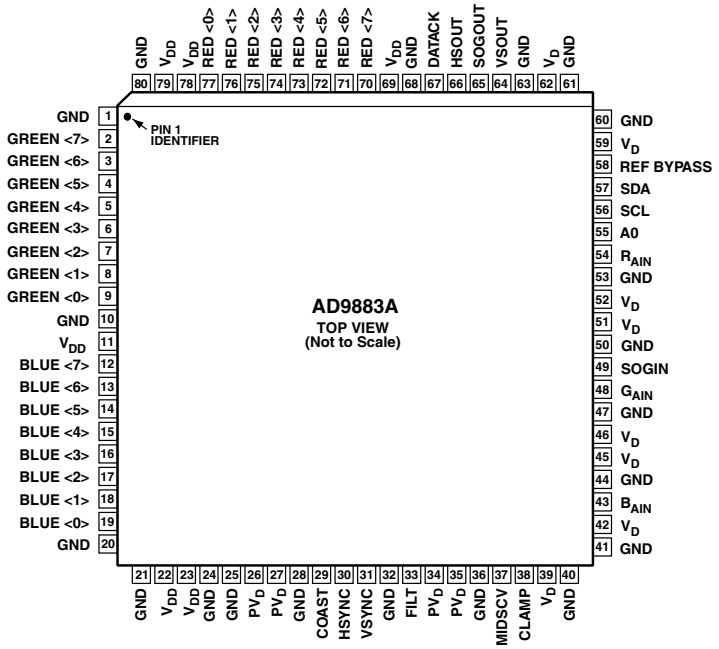


Table I. Complete Pinout List

Pin Type	Mnemonic	Function	Value	Pin Number
Inputs	R_{AIN}	Analog Input for Converter R	0.0 V to 1.0 V	54
	G_{AIN}	Analog Input for Converter G	0.0 V to 1.0 V	48
	B_{AIN}	Analog Input for Converter B	0.0 V to 1.0 V	43
	HSYNC	Horizontal SYNC Input	3.3 V CMOS	30
	VSYNC	Vertical SYNC Input	3.3 V CMOS	31
	SOGIN	Input for Sync-on-Green	0.0 V to 1.0 V	49
	CLAMP	Clamp Input (External CLAMP Signal)	3.3 V CMOS	38
	COAST	PLL COAST Signal Input	3.3 V CMOS	29
Outputs	Red [7:0]	Outputs of Converter "Red," Bit 7 is the MSB	3.3 V CMOS	70–77
	Green [7:0]	Outputs of Converter "Green," Bit 7 is the MSB	3.3 V CMOS	2–9
	Blue [7:0]	Outputs of Converter "Blue," Bit 7 is the MSB	3.3 V CMOS	12–19
	DATACK	Data Output Clock	3.3 V CMOS	67
	HSOUT	HSYNC Output (Phase-Aligned with DATACK)	3.3 V CMOS	66
	VSOUT	VSYNC Output (Phase-Aligned with DATACK)	3.3 V CMOS	64
	SOGOUT	Sync-on-Green Slicer Output	3.3 V CMOS	65
References	REF BYPASS	Internal Reference Bypass	1.25 V	58
	MIDSCV	Internal Midscale Voltage Bypass		37
	FILT	Connection for External Filter Components for Internal PLL		33
Power Supply	V_D	Analog Power Supply	3.3 V	39, 42, 45, 46, 51, 52, 59, 62
	V_{DD}	Output Power Supply	3.3 V	11, 22, 23, 69, 78, 79
	PV_D	PLL Power Supply	3.3 V	26, 27, 34, 35
	GND	Ground	0 V	1, 10, 20, 21, 24, 25, 28, 32, 36, 40, 41, 44, 47, 50, 53, 60, 61, 63, 68, 80
Control	SDA	Serial Port Data I/O	3.3 V CMOS	57
	SCL	Serial Port Data Clock (100 kHz Maximum)	3.3 V CMOS	56
	A0	Serial Port Address Input 1	3.3 V CMOS	55

PIN FUNCTION DESCRIPTIONS

Pin Name	Function
OUTPUTS	
HSOUT	Horizontal Sync Output A reconstructed and phase-aligned version of the Hsync input. Both the polarity and duration of this output can be programmed via serial bus registers. By maintaining alignment with DATACK and Data, data timing with respect to horizontal sync can always be determined.
VSOUT	Vertical Sync Output A reconstructed and phase-aligned version of the video Vsync. The polarity of this output can be controlled via a serial bus bit. The placement and duration in all modes is set by the graphics transmitter.
SOGOUT	Sync-On-Green Slicer Output This pin outputs either the signal from the Sync-on-Green slicer comparator or an unprocessed but delayed version of the Hsync input. See the Sync Processing Block Diagram (Figure 12) to view how this pin is connected. (Note: Besides slicing off SOG, the output from this pin gets no other additional processing on the AD9883A. Vsync separation is performed via the sync separator.)
SERIAL PORT (2-Wire)	
SDA	Serial Port Data I/O
SCL	Serial Port Data Clock
A0	Serial Port Address Input 1 For a full description of the 2-wire serial register and how it works, refer to the 2-Wire Serial Control Port section.
DATA OUTPUTS	
RED	Data Output, RED Channel
GREEN	Data Output, GREEN Channel
BLUE	Data Output, BLUE Channel The main data outputs. Bit 7 is the MSB. The delay from pixel sampling time to output is fixed. When the sampling time is changed by adjusting the PHASE register, the output timing is shifted as well. The DATACK and HSOUT outputs are also moved, so the timing relationship among the signals is maintained. For exact timing information, refer to Figures 7 and 8.
DATA CLOCK OUTPUT	
DATACK	Data Output Clock This is the main clock output signal used to strobe the output data and HSOUT into external logic. It is produced by the internal clock generator and is synchronous with the internal pixel sampling clock. When the sampling time is changed by adjusting the PHASE register, the output timing is shifted as well. The Data, DATACK, and HSOUT outputs are all moved, so the timing relationship among the signals is maintained.
INPUTS	
R_{AIN}	Analog Input for RED Channel
G_{AIN}	Analog Input for GREEN Channel
B_{AIN}	Analog Input for BLUE Channel High impedance inputs that accept the RED, GREEN, and BLUE channel graphics signals, respectively. (The three channels are identical, and can be used for any colors, but colors are assigned for convenient reference.) They accommodate input signals ranging from 0.5 V to 1.0 V full scale. Signals should be ac-coupled to these pins to support clamp operation.
HSYNC	Horizontal Sync Input This input receives a logic signal that establishes the horizontal timing reference and provides the frequency reference for pixel clock generation. The logic sense of this pin is controlled by serial register 0Eh Bit 6 (Hsync Polarity). Only the leading edge of Hsync is active; the trailing edge is ignored. When Hsync Polarity = 0, the falling edge of Hsync is used. When Hsync Polarity = 1, the rising edge is active. The input includes a Schmitt trigger for noise immunity, with a nominal input threshold of 1.5 V.
VSYNC	Vertical Sync Input This is the input for vertical sync.
SOGIN	Sync-on-Green Input This input is provided to assist with processing signals with embedded sync, typically on the GREEN channel. The pin is connected to a high speed comparator with an internally generated threshold. The threshold level can be programmed in 10 mV steps to any voltage between 10 mV and 330 mV above the negative peak of the input signal. The default voltage threshold is 150 mV. When connected to an ac-coupled graphics signal with embedded sync, it will produce a noninverting digital output on SOGOUT. (This is usually a composite sync signal, containing both vertical and horizontal sync information that must be separated before passing the horizontal sync signal to Hsync.) When not used, this input should be left unconnected. For more details on this function and how it should be configured, refer to the Sync-on-Green section.

PIN FUNCTION DESCRIPTIONS (continued)

Pin Name	Function
CLAMP	External Clamp Input This logic input may be used to define the time during which the input signal is clamped to ground. It should be exercised when the reference dc level is known to be present on the analog input channels, typically during the back porch of the graphics signal. The CLAMP pin is enabled by setting control bit Clamp Function to 1, (register 0FH, Bit 7, default is 0). When disabled, this pin is ignored and the clamp timing is determined internally by counting a delay and duration from the trailing edge of the Hsync input. The logic sense of this pin is controlled by Clamp Polarity register 0FH, Bit 6. When not used, this pin must be grounded and Clamp Function programmed to 0.
COAST	Clock Generator Coast Input (Optional) This input may be used to cause the pixel clock generator to stop synchronizing with Hsync and continue producing a clock at its current frequency and phase. This is useful when processing signals from sources that fail to produce horizontal sync pulses during the vertical interval. The COAST signal is generally *not* required for PC-generated signals. The logic sense of this pin is controlled by Coast Polarity (register 0FH, Bit 3). When not used, this pin may be grounded and Coast Polarity programmed to 1, or tied HIGH (to V_D through a 10 kΩ resistor) and Coast Polarity programmed to 0. Coast Polarity defaults to 1 at power-up.
REF BYPASS	Internal Reference BYPASS Bypass for the internal 1.25 V bandgap reference. It should be connected to ground through a 0.1 µF capacitor. The absolute accuracy of this reference is ±4%, and the temperature coefficient is ±50 ppm, which is adequate for most AD9883A applications. If higher accuracy is required, an external reference may be employed instead.
MIDSCV	Midscale Voltage Reference BYPASS Bypass for the internal midscale voltage reference. It should be connected to ground through a 0.1 µF capacitor. The exact voltage varies with the gain setting of the BLUE channel.
FILT	External Filter Connection For proper operation, the pixel clock generator PLL requires an external filter. Connect the filter shown in Figure 6 to this pin. For optimal performance, minimize noise and parasitics on this node.
POWER SUPPLY	
V_D	Main Power Supply These pins supply power to the main elements of the circuit. They should be as quiet and filtered as possible.
V_{DD}	Digital Output Power Supply A large number of output pins (up to 25) switching at high speed (up to 110 MHz) generates a lot of power supply transients (noise). These supply pins are identified separately from the V_D pins so special care can be taken to minimize output noise transferred into the sensitive analog circuitry. If the AD9883A is interfacing with lower voltage logic, V_{DD} may be connected to a lower supply voltage (as low as 2.5 V) for compatibility.
PV_D	Clock Generator Power Supply The most sensitive portion of the AD9883A is the clock generation circuitry. These pins provide power to the clock PLL and help the user design for optimal performance. The designer should provide "quiet," noise-free power to these pins.
GND	Ground The ground return for all circuitry on chip. It is recommended that the AD9883A be assembled on a single solid ground plane, with careful attention to ground current paths.

DESIGN GUIDE

General Description

The AD9883A is a fully integrated solution for capturing analog RGB signals and digitizing them for display on flat panel monitors or projectors. The circuit is ideal for providing a computer interface for HDTV monitors or as the front end to high performance video scan converters.

Implemented in a high performance CMOS process, the interface can capture signals with pixel rates up to 110 MHz.

The AD9883A includes all necessary input buffering, signal dc restoration (clamping), offset and gain (brightness and contrast) adjustment, pixel clock generation, sampling phase control, and output data formatting. All controls are programmable via a 2-wire serial interface. Full integration of these sensitive analog functions makes system design straightforward and less sensitive to the physical and electrical environment.

With a typical power dissipation of only 500 mW and an operating temperature range of 0°C to 70°C, the device requires no special environmental considerations.

Digital Inputs

All digital inputs on the AD9883A operate to 3.3 V CMOS levels. However, all digital inputs are 5 V tolerant. Applying 5 V to them will not cause any damage.

Input Signal Handling

The AD9883A has three high impedance analog input pins for the Red, Green, and Blue channels. They will accommodate signals ranging from 0.5 V to 1.0 V p-p.

Signals are typically brought onto the interface board via a DVI-I connector, a 15-pin D connector, or via BNC connectors. The AD9883A should be located as close as practical to the input connector. Signals should be routed via matched-impedance traces (normally 75 Ω) to the IC input pins.

At that point the signal should be resistively terminated (75 Ω to the signal ground return) and capacitively coupled to the AD9883A inputs through 47 nF capacitors. These capacitors form part of the dc restoration circuit.

In an ideal world of perfectly matched impedances, the best performance can be obtained with the widest possible signal bandwidth. The ultrawide bandwidth inputs of the AD9883A (300 MHz) can track the input signal continuously as it moves from one pixel level to the next, and digitize the pixel during a long, flat pixel time. In many systems, however, there are mismatches, reflections, and noise, which can result in excessive ringing and distortion of the input waveform. This makes it more difficult to establish a sampling phase that provides good image quality. It has been shown that a small inductor in series with the input is effective in rolling off the input bandwidth slightly, and providing a high quality signal over a wider range of conditions. Using a Fair-Rite #2508051217Z0 High-Speed Signal Chip Bead inductor in the circuit of Figure 1 gives good results in most applications.

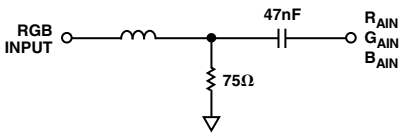


Figure 1. Analog Input Interface Circuit

Hsync, Vsync Inputs
The interface also takes a horizontal sync signal, which is used to generate the pixel clock and clamp timing. This can be either a sync signal directly from the graphics source, or a preprocessed TTL or CMOS level signal.

The Hsync input includes a Schmitt trigger buffer for immunity to noise and signals with long rise times. In typical PC-based graphic systems, the sync signals are simply TTL-level drivers feeding unshielded wires in the monitor cable. As such, no termination is required.

Serial Control Port
The serial control port is designed for 3.3 V logic. If there are 5 V drivers on the bus, these pins should be protected with 150 Ω series resistors placed between the pull-up resistors and the input pins.

Output Signal Handling
The digital outputs are designed and specified to operate from a 3.3 V power supply (V_{DD}). They can also work with a V_{DD} as low as 2.5 V for compatibility with other 2.5 V logic.

Clamping

RGB Clamping
To properly digitize the incoming signal, the dc offset of the input must be adjusted to fit the range of the on-board A/D converters.

Most graphics systems produce RGB signals with black at ground and white at approximately 0.75 V. However, if sync signals are embedded in the graphics, the sync tip is often at ground and black is at 300 mV. Then white is at approximately 1.0 V. Some common RGB line amplifier boxes use emitter-follower buffers to split signals and increase drive capability. This introduces a 700 mV dc offset to the signal, which must be removed for proper capture by the AD9883A.

The key to clamping is to identify a portion (time) of the signal when the graphic system is known to be producing black. An offset is then introduced which results in the A/D converters producing a black output (code 00h) when the known black input is present. The offset then remains in place when other signal levels are processed, and the entire signal is shifted to eliminate offset errors.

In most PC graphics systems, black is transmitted between active video lines. With CRT displays, when the electron beam has completed writing a horizontal line on the screen (at the right side), the beam is deflected quickly to the left side of the screen (called horizontal retrace) and a black signal is provided to prevent the beam from disturbing the image.

In systems with embedded sync, a blacker-than-black signal (Hsync) is produced briefly to signal the CRT that it is time to begin a retrace. For obvious reasons, it is important to avoid clamping on the tip of Hsync. Fortunately, there is virtually always a period following Hsync called the back porch where a good black reference is provided. This is the time when clamping should be done.

The clamp timing can be established by simply exercising the CLAMP pin at the appropriate time (with External Clamp = 1). The polarity of this signal is set by the Clamp Polarity bit.

A simpler method of clamp timing employs the AD9883A internal clamp timing generator. The Clamp Placement register is programmed with the number of pixel times that should pass after the trailing edge of HSYNC before clamping starts. A second register (Clamp Duration) sets the duration of the clamp. These are both 8-bit values, providing considerable flexibility in clamp generation. The clamp timing is referenced to the trailing edge of Hsync because, though Hsync duration can vary widely, the back porch (black reference) always follows Hsync. A good starting point for establishing clamping is to set the clamp placement to 09h (providing 9 pixel periods for the graphics signal to stabilize after sync) and set the clamp duration to 14h (giving the clamp 20 pixel periods to reestablish the black reference).

Clamping is accomplished by placing an appropriate charge on the external input coupling capacitor. The value of this capacitor affects the performance of the clamp. If it is too small, there will be a significant amplitude change during a horizontal line time (between clamping intervals). If the capacitor is too large, then it will take excessively long for the clamp to recover from a large change in incoming signal offset. The recommended value (47 nF) results in recovering from a step error of 100 mV to within 1/2 LSB in 10 lines with a clamp duration of 20 pixel periods on a 60 Hz SXGA signal.

YUV Clamping
YUV graphic signals are slightly different from RGB signals in that the dc reference level (black level in RGB signals) can be at the midpoint of the graphics signal rather than the bottom. For these signals it can be necessary to clamp to the midscale range of the A/D converter range (80h) rather than bottom of the A/D converter range (00h).

Clamping to midscale rather than ground can be accomplished by setting the clamp select bits in the serial bus register. Each of the three converters has its own selection bit so that they can be clamped to either midscale or ground independently. These bits are located in register 10h and are Bits 0–2. The midscale reference voltage that each A/D converter clamps to is provided on the MIDSCV pin, (Pin 37). This pin should be bypassed to ground with a 0.1 μF capacitor, (even if midscale clamping is not required).

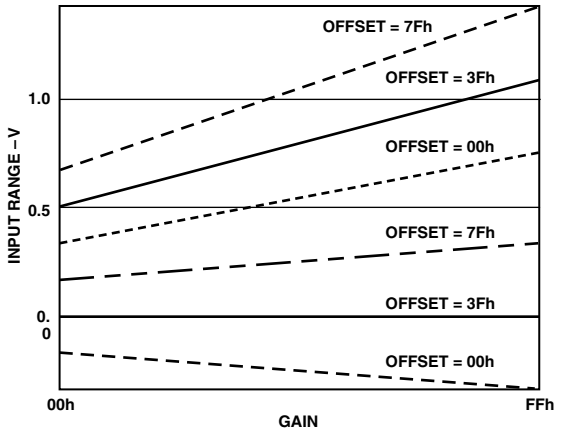


Figure 2. Gain and Offset Control

Gain and Offset Control

The AD9883A can accommodate input signals with inputs ranging from 0.5 V to 1.0 V full scale. The full-scale range is set in three 8-bit registers (Red Gain, Green Gain, and Blue Gain).

Note that *increasing* the gain setting results in an image with *less* contrast.

The offset control shifts the entire input range, resulting in a change in image brightness. Three 7-bit registers (Red Offset, Green Offset, Blue Offset) provide independent settings for each channel.

The offset controls provide a ±63 LSB adjustment range. This range is connected with the full-scale range, so if the input range is doubled (from 0.5 V to 1.0 V) then the offset step size is also doubled (from 2 mV per step to 4 mV per step).

Figure 2 illustrates the interaction of gain and offset controls. The magnitude of an LSB in offset adjustment is proportional to the full-scale range, so changing the full-scale range also changes the offset. The change is minimal if the offset setting is near midscale. When changing the offset, the full-scale *range* is not affected, but the full-scale *level* is shifted by the same amount as the zero scale level.

Sync-on-Green

The Sync-on-Green input operates in two steps. First, it sets a baseline clamp level off of the incoming video signal with a negative peak detector. Second, it sets the sync trigger level to a programmable level (typically 150 mV) above the negative peak. The Sync-on-Green input must be ac-coupled to the Green analog input through its own capacitor as shown in Figure 3. The value of the capacitor must be 1 nF ± 20%. If Sync-on-Green is not used, this connection is not required. Note: The Sync-on-Green signal is always negative polarity.

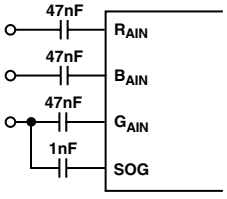


Figure 3. Typical Clamp Configuration

Clock Generation

A phase locked loop (PLL) is employed to generate the pixel clock. In this PLL, the Hsync input provides a reference frequency. A voltage controlled oscillator (VCO) generates a much higher pixel clock frequency. This pixel clock is divided by the PLL divide value (registers 01H and 02H) and phase compared with the Hsync input. Any error is used to shift the VCO frequency and maintain lock between the two signals.

The stability of this clock is a very important element in providing the clearest and most stable image. During each pixel time, there is a period during which the signal is slewing from the old pixel amplitude and settling at its new value. Then there is a time when the input voltage is stable, before the signal must slew to a new value (Figure 4). The ratio of the slewing time to the stable time is a function of the bandwidth of the graphics DAC and the bandwidth of the transmission system (cable and termination). It is also a function of the overall pixel rate. Clearly, if the dynamic characteristics of the system remain fixed, then the slewing and settling time is likewise fixed. This time must be subtracted from the total pixel period, leaving the stable period. At higher pixel frequencies, the total cycle time is shorter, and the stable pixel time becomes shorter as well.

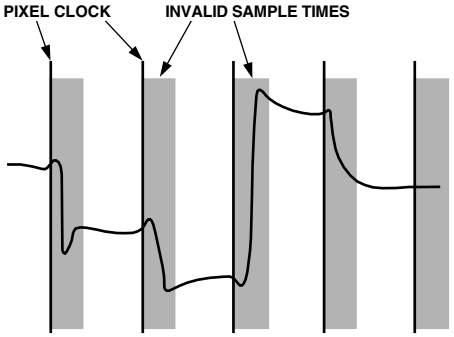


Figure 4. Pixel Sampling Times

Any jitter in the clock reduces the precision with which the sampling time can be determined, and must also be subtracted from the stable pixel time.

Considerable care has been taken in the design of the AD9883A's clock generation circuit to minimize jitter. As indicated in Figure 5, the clock jitter of the AD9883A is less than 5% of the total pixel time in all operating modes, making the reduction in the valid sampling time due to jitter negligible.

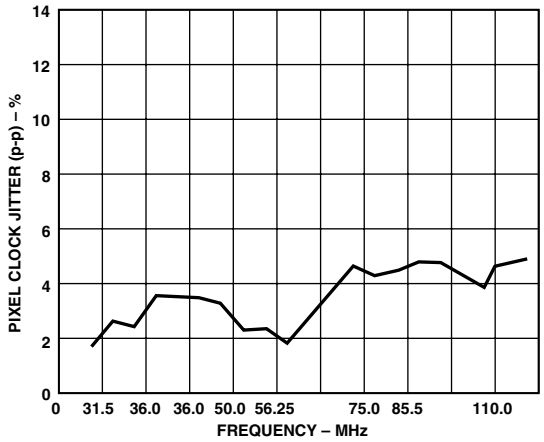


Figure 5. Pixel Clock Jitter vs. Frequency

The PLL characteristics are determined by the loop filter design, by the PLL Charge Pump Current and by the VCO range setting. The loop filter design is illustrated in Figure 6. Recommended settings of VCO range and charge pump current for VESA standard display modes are listed in Table V.

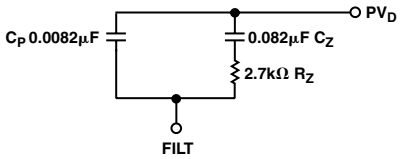


Figure 6. PLL Loop Filter Detail

Four programmable registers are provided to optimize the performance of the PLL. These registers are:

1. The 12-Bit Divisor Register. The input Hsync frequencies range from 15 kHz to 110 kHz. The PLL multiplies the frequency of the Hsync signal, producing pixel clock frequencies in the range of 12 MHz to 110 MHz. The Divisor Register controls the exact multiplication factor. This register may be set to any value between 221 and 4095. (The divide ratio that is actually used is the programmed divide ratio plus one.)
2. The 2-Bit VCO Range Register. To improve the noise performance of the AD9883A, the VCO operating frequency range is divided into three overlapping regions. The VCO Range Register sets this operating range. The frequency ranges for the lowest and highest regions are shown in Table II.

Table II. VCO Frequency Ranges

PV1	PV0	Pixel Clock Range (MHz)	K_{VCO} Gain (MHz/V)
0	0	12–32	150
0	1	32–64	150
1	0	64–110	150
1	1	110–140	180

3. The 3-Bit Charge Pump Current Register. This register allows the current that drives the low pass loop filter to be varied. The possible current values are listed in Table III.

Table III. Charge Pump Current/Control Bits

Ip2	Ip1	Ip0	Current (µA)
0	0	0	50
0	0	1	100
0	1	0	150
0	1	1	250
1	0	0	350
1	0	1	500
1	1	0	750
1	1	1	1500

4. The 5-Bit Phase Adjust Register. The phase of the generated sampling clock may be shifted to locate an optimum sampling point within a clock cycle. The Phase Adjust Register provides 32 phase-shift steps of 11.25° each. The Hsync signal with an identical phase shift is available through the HSOUT pin.

   The COAST pin is used to allow the PLL to continue to run at the same frequency, in the absence of the incoming Hsync signal or during disturbances in Hsync (such as equalization pulses). This may be used during the vertical sync period, or any other time that the Hsync signal is unavailable. The polarity of the COAST signal may be set through the Coast Polarity Register. Also, the polarity of the Hsync signal may be set through the Hsync Polarity Register. If not using automatic polarity detection, the Hsync and COAST Polarity bits should be set to match the respective polarities of the input signals.

Power Management

The AD9883A uses the activity detect circuits, the active interface bits in the serial bus, the active interface override bits, and the power-down bit to determine the correct power state. There are three power states, full-power, seek mode, and power-down. Table IV summarizes how the AD9883A determines what power mode to be in and what circuitry is powered on/off in each of these modes. The power-down command has priority and then the automatic circuitry.

Table IV. Power-Down Mode Descriptions

Mode	Inputs Power-Down[1]	Sync Detect[2]	Powered On or Comments
Full-Power	1	1	Everything
Seek Mode	1	0	Serial Bus, Sync Activity Detect, SOG, Band Gap Reference
Power-Down	0	X	Serial Bus, Sync Activity Detect, SOG, Band Gap Reference

NOTES
[1]Power-down is controlled via Bit 1 in serial bus register 0Fh.
[2]Sync detect is determined by OR-ing Bits 7, 4, and 1 in serial bus register 14h.

Table V. Recommended VCO Range and Charge Pump Current Settings for Standard Display Formats

Standard	Resolution	Refresh Rate	Horizontal Frequency	Pixel Rate	VCORNGE	Current
VGA	640 × 480	60 Hz	31.5 kHz	25.175 MHz	00	110
		72 Hz	37.7 kHz	31.500 MHz	00	110
		75 Hz	37.5 kHz	31.500 MHz	00	110
		85 Hz	43.3 kHz	36.000 MHz	01	100
SVGA	800 × 600	56 Hz	35.1 kHz	36.000 MHz	01	100
		60 Hz	37.9 kHz	40.000 MHz	01	100
		72 Hz	48.1 kHz	50.000 MHz	01	101
		75 Hz	46.9 kHz	49.500 MHz	01	101
		85 Hz	53.7 kHz	56.250 MHz	01	101
XGA	1024 × 768	60 Hz	48.4 kHz	65.000 MHz	10	101
		70 Hz	56.5 kHz	75.000 MHz	10	100
		75 Hz	60.0 kHz	78.750 MHz	10	100
		80 Hz	64.0 kHz	85.500 MHz	10	101
		85 Hz	68.3 kHz	94.500 MHz	10	101
SXGA	1280 × 1024	60 Hz	64.0 kHz	108.000 MHz	10	110
		75 Hz	80.0 kHz	135.000 MHz	11	110

Timing

The following timing diagrams show the operation of the AD9883A.

The output data clock signal is created so that its rising edge always occurs between data transitions, and can be used to latch the output data externally.

There is a pipeline in the AD9883A, which must be flushed before valid data becomes available. This means four data sets are presented before valid data is available.

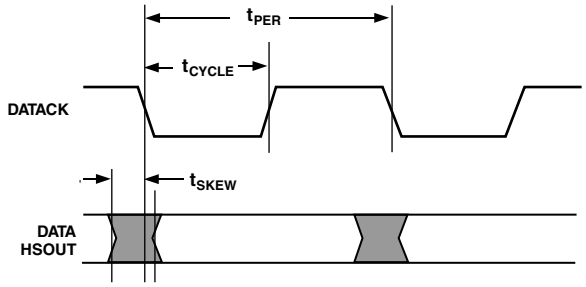


Figure 7. Output Timing

Hsync Timing

Horizontal Sync (Hsync) is processed in the AD9883A to eliminate ambiguity in the timing of the leading edge with respect to the phase-delayed pixel clock and data.

The Hsync input is used as a reference to generate the pixel sampling clock. The sampling phase can be adjusted, with respect to Hsync, through a full 360° in 32 steps via the Phase Adjust Register (to optimize the pixel sampling time). Display systems use Hsync to align memory and display write cycles, so it is important to have a stable timing relationship between Hsync output (HSOUT) and data clock (DATACK).

Three things happen to Horizontal Sync in the AD9883A. First, the polarity of Hsync input is determined and will thus have a known output polarity. The known output polarity can be programmed either active high or active low (register 0EH, Bit 5). Second, HSOUT is aligned with DATACK and data outputs. Third, the duration of HSOUT (in pixel clocks) is set via register 07H. HSOUT is the sync signal that should be used to drive the rest of the display system.

Coast Timing

In most computer systems, the Hsync signal is provided continuously on a dedicated wire. In these systems, the COAST input and function are unnecessary, and should not be used and the pin should be permanently connected to the inactive state.

In some systems, however, Hsync is disturbed during the Vertical Sync period (Vsync). In some cases, Hsync pulses disappear. In other systems, such as those that employ Composite Sync (Csync) signals or embedded Sync-on-Green (SOG), Hsync includes equalization pulses or other distortions during Vsync. To avoid upsetting the clock generator during Vsync, it is important to ignore these distortions. If the pixel clock PLL sees extraneous pulses, it will attempt to lock to this new frequency, and will have changed frequency by the end of the Vsync period. It will then take a few lines of correct Hsync timing to recover at the beginning of a new frame, resulting in a "tearing" of the image at the top of the display.

The COAST input is provided to eliminate this problem. It is an asynchronous input that disables the PLL input and allows the clock to free-run at its then-current frequency. The PLL can free-run for several lines without significant frequency drift.

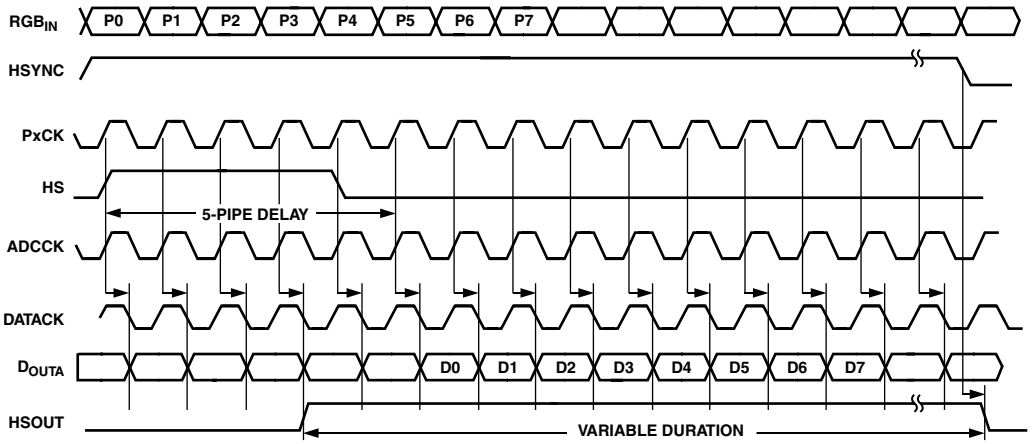


Figure 8. 4:4:4 Mode (For RGB and YUV)

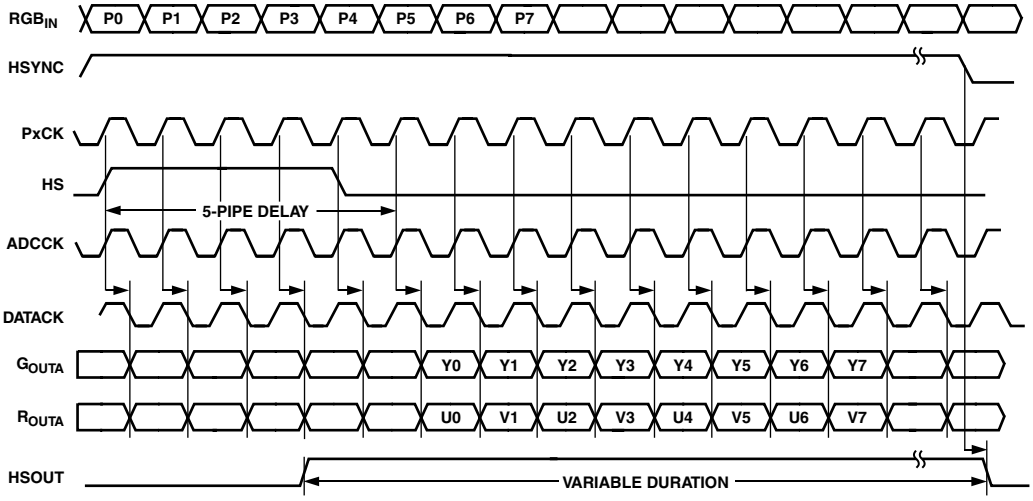


Figure 9. 4:2:2 Mode (For YUV Only)

2-Wire Serial Register Map

The AD9883A is initialized and controlled by a set of registers, which determine the operating modes. An external controller is employed to write and read the control registers through the two-line serial interface port.

Table VI. Control Register Map

Hex Address	Write and Read or Read Only	Bits	Default Value	Register Name	Function
00H	RO	7:0		Chip Revision	An 8-bit register that represents the silicon revision level. Revision 0 = 0000 0000.
01H*	R/$\overline{W}$	7:0	01101001	PLL Div MSB	This register is for Bits [11:4] of the PLL divider. Larger values mean the PLL operates at a faster rate. This register should be loaded first whenever a change is needed. This will give the PLL more time to lock.
02H*	R/$\overline{W}$	7:4	1101****	PLL Div LSB	Bits [7:4] LSBs of the PLL divider word.
03H	R/$\overline{W}$	7:3	01****** **001***		Bits [7:6] VCO Range. Selects VCO frequency range. (See PLL description). Bits [5:3] Charge Pump Current. Varies the current that drives the low pass filter. (See PLL description.)
04H	R/$\overline{W}$	7:3	10000***	Phase Adjust	ADC Clock Phase Adjustment. Larger values mean more delay. (1 LSB = T/32)
05H	R/$\overline{W}$	7:0	10000000	Clamp Placement	Places the Clamp signal an integer number of clock periods after the trailing edge of the Hsync signal.
06H	R/$\overline{W}$	7:0	10000000	Clamp Duration	Number of clock periods that the Clamp signal is actively clamping.
07H	R/$\overline{W}$	7:0	00100000	Hsync Output Pulsewidth	Sets the number of pixel clocks that HSOUT will remain active.
08H	R/$\overline{W}$	7:0	10000000	Red Gain	Controls ADC input range (contrast) of each respective channel. Bigger values give less contrast.
09H	R/$\overline{W}$	7:0	10000000	Green Gain	
0AH	R/$\overline{W}$	7:0	10000000	Blue Gain	
0BH	R/$\overline{W}$	7:1	1000000*	Red Offset	Controls dc offset (brightness) of each respective channel. Bigger values decrease brightness.
0CH	R/$\overline{W}$	7:1	1000000*	Green Offset	
0DH	R/$\overline{W}$	7:1	1000000*	Blue Offset	
0EH	R/$\overline{W}$	7:0	0******* *1****** **0***** ***0**** ****0*** *****0** ******0* *******0	Sync Control	Bit 7 – Hsync Polarity Override. (Logic 0 = Polarity determined by chip, Logic 1 = Polarity set by Bit 6 in register 0Eh.) Bit 6 – Hsync Input Polarity. Indicates polarity of incoming Hsync signal to the PLL. (Logic 0 = Active Low, Logic 1 = Active High.) Bit 5 – Hsync Output Polarity. (Logic 0 = Logic High Sync, Logic 1 = Logic Low Sync.) Bit 4 – Active Hsync Override. If set to Logic 1, the user can select the Hsync to be used via Bit 3. If set to Logic 0, the active interface is selected via Bit 6 in register 14H. Bit 3 – Active Hsync Select. Logic 0 selects Hsync as the active sync. Logic 1 selects Sync-on-Green as the active sync. Note: The indicated Hsync will be used only if Bit 4 is set to Logic 1 or if both syncs are active, (Bits 1, 7 = Logic 1 in register 14H). Bit 2 – Vsync Output Invert. (Logic 1 = No Invert, Logic 0 = Invert) Bit 1 – Active Vsync Override. If set to Logic 1, the user can select the Vsync to be used via Bit 0. If set to Logic 0, the active interface is selected via Bit 3 in register 14H. Bit 0 – Active Vsync Select. Logic 0 selects Raw Vsync as the output Vsync. Logic 1 selects Sync Separated Vsync as the output Vsync. Note: The indicated Vsync will be used only if Bit 1 is set to Logic 1.

Table VI. Control Register Map (continued)

Hex Address	Write and Read or Read Only	Bits	Default Value	Register Name	Function
0FH	R/$\overline{W}$	7:1	0******* *1****** **0***** ***0**** ****1*** *****1** ******1*		Bit 7 – Clamp Function. Chooses between Hsync for Clamp signal or another external signal to be used for clamping. (Logic 0 = Hsync, Logic 1 = Clamp.) Bit 6 – Clamp Polarity. Valid only with external Clamp signal. (Logic 0 = Active High, Logic 1 Selects Active Low.) Bit 5 – Coast Select. Logic 0 selects the coast input pins to be used for the PLL coast. Logic 1 selects Vsync to be used for the PLL coast. Bit 4 – Coast Polarity Override. (Logic 0 = Polarity determined by chip, Logic 1 = Polarity set by Bit 3 in register 0Fh.) Bit 3 – Coast Polarity. Changes polarity of external COAST signal. (Logic 0 = Active Low, Logic 1 = Active High.) Bit 2 – Seek Mode Override. (Logic 1 = allow low-power mode, Logic 0 = Disallow Low Power Mode.) Bit 1 – $\overline{PWRDN}$. Full Chip Power-Down, Active Low. (Logic 0 = Full Chip Power-Down, Logic 1 = Normal.)
10H	R/$\overline{W}$	7:3	10111*** *****0** ******0* *******0	Sync-on-Green Threshold	Sync-on-Green Threshold – Sets the voltage level of the Sync-on-Green slicer's comparator. Bit 2 – Red Clamp Select – Logic 0 selects clamp to ground. Logic 1 selects clamp to midscale (voltage at Pin 37). Bit 1 – Green Clamp Select – Logic 0 selects clamp to ground. Logic 1 selects clamp to midscale (voltage at Pin 37). Bit 0 – Blue Clamp Select – Logic 0 selects clamp to ground. Logic 1 selects clamp to midscale (voltage at Pin 37).
11H	R/$\overline{W}$	7:0	00100000	Sync Separator Threshold	Sync Separator Threshold – Sets how many internal 5 MHz clock periods the sync separator will count to before toggling high or low. This should be set to some number greater than the maximum Hsync or equalization pulsewidth.
12H	R/$\overline{W}$	7:0	00000000	Pre-Coast	Pre-Coast – Sets the number of Hsync periods that Coast becomes active prior to Vsync.
13H	R/$\overline{W}$	7:0	00000000	Post-Coast	Post-Coast – Sets the number of Hsync periods that Coast stays active following Vsync.
14H	RO	7:0		Sync Detect	Bit 7 – Hsync detect. It is set to Logic 1 if Hsync is present on the analog interface; otherwise it is set to Logic 0. Bit 6 – AHS: Active Hsync. This bit indicates which analog Hsync is being used. (Logic 0 = Hsync Input Pin, Logic 1 = Hsync from Sync-on-Green.) Bit 5 – Input Hsync Polarity Detect. (Logic 0 = Active Low, Logic 1 = Active High.) Bit 4 – Vsync Detect. It is set to Logic 1 if V sync is present on the analog interface; otherwise it is set to Logic 0. Bit 3 – AVS: Active Vsync. This bit indicates which analog Vsync is being used. (Logic 0 = Vsync Input Pin, Logic 1 = Vsync from Sync Separator.) Bit 2 – Output Vsync Polarity Detect. (Logic 0 = Active Low, Logic 1 = Active High.) Bit 1 – Sync-on-Green Detect. It is set to Logic 1 if sync is present on the Green video input; otherwise it is set to 0. Bit 0 – Input Coast Polarity Detect. (Logic 0 = Active Low, Logic 1 = Active High.)

Table VI. Control Register Map (continued)

Hex Address	Write and Read or Read Only	Bits	Default Value	Register Name	Function
15H	R/$\overline{W}$	7:0		Test Register	Bits [7:2] Reserved for future use. Bit 1 – 4:2:2 Output Formatting Mode. Bit 0 – Must be set to 0 for proper operation.
16H	R/$\overline{W}$	7:0		Test Register	Reserved for future use.
17H	RO	7:0		Test Register	Reserved for future use.
18H	RO	7:0		Test Register	Reserved for future use.

NOTE
*The AD9883A only updates the PLL divide ratio when the LSBs are written to (register 02h).

2-WIRE SERIAL CONTROL REGISTER DETAIL CHIP IDENTIFICATION

00 7–0 Chip Revision

An 8-bit register that represents the silicon revision. Revision 0 = 0000 0000, Revision 1 = 0000 0001, Revision 2 = 0000 0010.

PLL DIVIDER CONTROL

01 7–0 PLL Divide Ratio MSBs

The 8 most significant bits of the 12-bit PLL divide ratio PLLDIV. (The operational divide ratio is PLLDIV + 1.)

The PLL derives a master clock from an incoming Hsync signal. The master clock frequency is then divided by an integer value, such that the output is phase-locked to Hsync. This PLLDIV value determines the number of pixel times (pixels plus horizontal blanking overhead) per line. This is typically 20% to 30% more than the number of active pixels in the display.

The 12-bit value of the PLL divider supports divide ratios from 2 to 4095. The higher the value loaded in this register, the higher the resulting clock frequency with respect to a fixed Hsync frequency.

VESA has established some standard timing specifications, which will assist in determining the value for PLLDIV as a function of horizontal and vertical display resolution and frame rate (Table V).

However, many computer systems do not conform precisely to the recommendations, and these numbers should be used only as a guide. The display system manufacturer should provide automatic or manual means for optimizing PLLDIV. An incorrectly set PLLDIV will usually produce one or more vertical noise bars on the display. The greater the error, the greater the number of bars produced.

The power-up default value of PLLDIV is 1693 (PLLDIVM = 69h, PLLDIVL = Dxh).

The AD9883A updates the full divide ratio only when the LSBs are changed. Writing to the MSB by itself will not trigger an update.

02 7–4 PLL Divide Ratio LSBs

The 4 least significant bits of the 12-bit PLL divide ratio PLLDIV. The operational divide ratio is PLLDIV + 1.

The power-up default value of PLLDIV is 1693 (PLLDIVM = 69h, PLLDIVL = Dxh).

The AD9883A updates the full divide ratio only when this register is written to.

CLOCK GENERATOR CONTROL

03 7–6 VCO Range Select

Two bits that establish the operating range of the clock generator.

VCORNGE must be set to correspond with the desired operating frequency (incoming pixel rate).

The PLL gives the best jitter performance at high frequencies. For this reason, in order to output low pixel rates and still get good jitter performance, the PLL actually operates at a higher frequency but then divides down the clock rate afterwards. Table VII shows the pixel rates for each VCO range setting. The PLL output divisor is automatically selected with the VCO range setting.

Table VII. VCO Ranges

VCORNGE	Pixel Rate Range
00	12–32
01	32–64
10	64–110
11	110–140

The power-up default value is 01.

03 5–3 CURRENT Charge Pump Current

Three bits that establish the current driving the loop filter in the clock generator.

Table VIII. Charge Pump Currents

CURRENT	Current (μA)
000	50
001	100
010	150
011	250
100	350
101	500
110	750
111	1500

CURRENT must be set to correspond with the desired operating frequency (incoming pixel rate).

The power-up default value is CURRENT = 001.

04 7–3 Clock Phase Adjust
A 5-bit value that adjusts the sampling phase in 32 steps across one pixel time. Each step represents an 11.25° shift in sampling phase.

The power-up default value is 16.

CLAMP TIMING

05 7–0 Clamp Placement
An 8-bit register that sets the position of the internally generated clamp.

When Clamp Function (Register 0Fh, Bit 7) = 0, a clamp signal is generated internally, at a position established by the clamp placement and for a duration set by the clamp duration. Clamping is started (Clamp Placement) pixel periods after the trailing edge of Hsync. The clamp placement may be programmed to any value between 1 and 255.

The clamp should be placed during a time that the input signal presents a stable black-level reference, usually the back porch period between Hsync and the image.

When Clamp Function = 1, this register is ignored.

06 7–0 Clamp Duration
An 8-bit register that sets the duration of the internally generated clamp.

For the best results, the clamp duration should be set to include the majority of the black reference signal time that follows the Hsync signal trailing edge. Insufficient clamping time can produce brightness changes at the top of the screen, and a slow recovery from large changes in the average picture level (APL), or brightness.

When Clamp Function = 1, this register is ignored.

Hsync PULSEWIDTH

07 7–0 Hsync Output Pulsewidth
An 8-bit register that sets the duration of the Hsync output pulse.

The leading edge of the Hsync output is triggered by the internally generated, phase-adjusted PLL feedback clock. The AD9883A then counts a number of pixel clocks equal to the value in this register. This triggers the trailing edge of the Hsync output, which is also phase adjusted.

INPUT GAIN

08 7–0 Red Channel Gain Adjust
An 8-bit word that sets the gain of the RED channel. The AD9883A can accommodate input signals with a full-scale range of between 0.5 V and 1.0 V p-p. Setting REDGAIN to 255 corresponds to an input range of 1.0 V. A REDGAIN of 0 establishes an input range of 0.5 V. Note that increasing REDGAIN results in the picture having less contrast (the input signal uses fewer of the available converter codes). See Figure 2.

09 7–0 Green Channel Gain Adjust
An 8-bit word that sets the gain of the GREEN channel. See REDGAIN (08).

0A 7–0 Blue Channel Gain Adjust
An 8-bit word that sets the gain of the BLUE channel. See REDGAIN (08).

INPUT OFFSET

0B 7–1 Red Channel Offset Adjust
A 7-bit offset binary word that sets the dc offset of the RED channel. One LSB of offset adjustment equals approximately one LSB change in the ADC offset. Therefore, the absolute magnitude of the offset adjustment scales as the gain of the channel is changed. A nominal setting of 63 results in the channel nominally clamping the back porch (during the clamping interval) to Code 00. An offset setting of 127 results in the channel clamping to Code 64 of the ADC. An offset setting of 0 clamps to Code –63 (off the bottom of the range). Increasing the value of Red Offset *decreases* the brightness of the channel.

0C 7–1 Green Channel Offset Adjust
A 7-bit offset binary word that sets the dc offset of the GREEN channel. See REDOFST (0B).

0D 7–1 Blue Channel Offset Adjust
A 7-bit offset binary word that sets the dc offset of the GREEN channel. See REDOFST (0B).

MODE CONTROL 1

0E 7 Hsync Input Polarity Override
This register is used to override the internal circuitry that determines the polarity of the Hsync signal going into the PLL.

Table IX. Hsync Input Polarity Override Settings

Override Bit	Function
0	Hsync Polarity Determined by Chip
1	Hsync Polarity Determined by User

The default for Hsync polarity override is 0 (polarity determined by chip).

0E 6 HSPOL Hsync Input Polarity
A bit that must be set to indicate the polarity of the Hsync signal that is applied to the PLL Hsync input.

Table X. Hsync Input Polarity Settings

HSPOL	Function
0	Active LOW
1	Active HIGH

Active LOW means the leading edge of the Hsync pulse is negative going. All timing is based on the leading edge of Hsync, which is the falling edge. The rising edge has no effect.

Active high is inverted from the traditional Hsync, with a positive-going pulse. This means that timing will be based on the leading edge of Hsync, which is now the rising edge.

The device will operate if this bit is set incorrectly, but the internally generated clamp position, as established by Clamp Placement (Register 05h), will not be placed as expected, which may generate clamping errors.

The power-up default value is HSPOL = 1.

0E 5 Hsync Output Polarity
One bit that determines the polarity of the Hsync output and the SOG output. Table XI shows the effect of this option. SYNC indicates the logic state of the sync pulse.

Table XI. Hsync Output Polarity Settings

Setting	SYNC
0	Logic 1 (Positive Polarity)
1	Logic 0 (Negative Polarity)

The default setting for this register is 0.

0E 4 Active Hsync Override
This bit is used to override the automatic Hsync selection, To override, set this bit to Logic 1. When overriding, the active Hsync is set via Bit 3 in this register.

Table XII. Active Hsync Override Settings

Override	Result
0	Autodetermines the Active Interface
1	Override, Bit 3 Determines the Active Interface

The default for this register is 0.

0E 3 Active Hsync Select
This bit is used under two conditions. It is used to select the active Hsync when the override bit is set (Bit 4). Alternately, it is used to determine the active Hsync when not overriding but both Hsyncs are detected.

Table XIII. Active HSYNC Select Settings

Select	Result
0	HSYNC Input
1	Sync-on-Green Input

The default for this register is 0.

0E 2 Vsync Output Invert
One bit that can invert the polarity of the Vsync output. Table XIV shows the effect of this option.

Table XIV. Vsync Output Invert Settings

Setting	Vsync Output
0	Invert
1	No Invert

The default setting for this register is 0.

0E 1 Active Vsync Override
This bit is used to override the automatic Vsync selection. To override, set this bit to Logic 1. When overriding, the active interface is set via Bit 0 in this register.

Table XV. Active Vsync Override Settings

Override	Result
0	Autodetermine the Active Vsync
1	Override, Bit 0 Determines the Active Vsync

The default for this register is 0.

0E 0 Active Vsync Select
This bit is used to select the active Vsync when the override bit is set (Bit 1).

Table XVI. Active Vsync Select Settings

Select	Result
0	Vsync Input
1	Sync Separator Output

The default for this register is 0.

0F 7 Clamp Input Signal Source
A bit that determines the source of clamp timing.

Table XVII. Clamp Input Signal Source Settings

Clamp Function	Function
0	Internally Generated Clamp
1	Externally Provided Clamp Signal

A 0 enables the clamp timing circuitry controlled by clamp placement and clamp duration. The clamp position and duration is counted from the leading edge of Hsync.

A 1 enables the external CLAMP input pin. The three channels are clamped when the CLAMP signal is active. The polarity of CLAMP is determined by the Clamp Polarity bit (Register 0Fh, Bit 6).

The power-up default value is Clamp Function = 0.

0F 6 Clamp Input Signal Polarity
A bit that determines the polarity of the externally provided CLAMP signal.

Table XVIII. Clamp Input Signal Polarity Settings

Clamp Function	Function
1	Active LOW
0	Active HIGH

A Logic 1 means that the circuit will clamp when CLAMP is LOW, and it will pass the signal to the ADC when CLAMP is HIGH.

A Logic 0 means that the circuit will clamp when CLAMP is HIGH, and it will pass the signal to the ADC when CLAMP is LOW.

The power-up default value is Clamp Polarity = 1.

0F 5 Coast Select
This bit is used to select the active Coast source. The choices are the Coast Input Pin or Vsync. If Vsync is selected the additional decision of using the Vsync input pin or the output from the sync separator needs to be made (Register 0E, Bits 1, 0).

Table XIX. Power-Down Settings

Select	Result
0	Coast Input Pin
1	Vsync (See above Text)

0F 4 Coast Input Polarity Override
This register is used to override the internal circuitry that determines the polarity of the coast signal going into the PLL.

Table XX. Coast Input Polarity Override Settings

Override Bit	Result
0	Coast Polarity Determined by Chip
1	Coast Polarity Determined by User

The default for coast polarity override is 0.

0F 3 Coast Input Polarity
A bit to indicate the polarity of the COAST signal that is applied to the PLL COAST input.

Table XXI. Coast Input Polarity Settings

Coast Polarity	Function
0	Active LOW
1	Active HIGH

Active LOW means that the clock generator will ignore Hsync inputs when COAST is LOW, and continue operating at the same nominal frequency until COAST goes HIGH.

Active HIGH means that the clock generator will ignore Hsync inputs when COAST is HIGH, and continue operating at the same nominal frequency until COAST goes LOW.

This function needs to be used along with the COAST polarity override bit (Bit 4).

The power-up default value is 1.

0F 2 Seek Mode Override
This bit is used to either allow or disallow the low power mode. The low power mode (Seek Mode) occurs when there are no signals on any of the Sync inputs.

Table XXII. Seek Mode Override Settings

Select	Result
1	Allow Seek Mode
0	Disallow Seek Mode

The default for this register is 1.

0F 1 $\overline{\text{PWRDN}}$
This bit is used to put the chip in full power-down. See the section on power management for details of which blocks are actually powered down.

Table XXIII. Power-Down Settings

Select	Result
0	Power-Down
1	Normal Operation

The default for this register is 1.

10 7-3 Sync-on-Green Slicer Threshold
This register allows the comparator threshold of the Sync-on-Green slicer to be adjusted. This register adjusts it in steps of 10 mV, with the minimum setting equaling 10 mV (11111) and the maximum setting equaling 330 mV (00000).

The default setting is 23 and corresponds to a threshold value of 0.15 V.

10 2 Red Clamp Select
A bit that determines whether the RED channel is clamped to ground or to midscale. For RGB video, all three channels are referenced to ground. For YcbCr (or YUV), the Y channel is referenced to ground, but the CbCr channels are referenced to midscale. Clamping to midscale actually clamps to Pin 37.

Table XXIV. Red Clamp Select Settings

Clamp	Function
0	Clamp to Ground
1	Clamp to Midscale (Pin 37)

The default setting for this register is 0.

10 1 Green Clamp Select
A bit that determines whether the GREEN channel is clamped to ground or to midscale.

Table XXV. Green Clamp Select Settings

Clamp	Function
0	Clamp to Ground
1	Clamp to Midscale (Pin 37)

The default setting for this register is 0.

10 0 Blue Clamp Select
A bit that determines whether the BLUE channel is clamped to ground or to midscale.

Table XXVI. Blue Clamp Select Settings

Clamp	Function
0	Clamp to Ground
1	Clamp to Midscale (Pin 37)

The default setting for this register is 0.

11 7:0 Sync Separator Threshold
This register is used to set the responsiveness of the sync separator. It sets how many internal 5 MHz clock periods the sync separator must count to before toggling high or low. It works like a low pass filter to ignore Hsync pulses in order to extract the Vsync signal. This register should be set to some number greater than the maximum Hsync pulsewidth. Note: the sync separator threshold uses an internal dedicated clock with a frequency of approximately 5 MHz.

The default for this register is 32.

12 7-0 Pre-Coast
This register allows the coast signal to be applied prior to the Vsync signal. This is necessary in cases where pre-equalization pulses are present. The step size for this control is one Hsync period.

The default is 0.

13 **7-0 Post-Coast**
This register allows the coast signal to be applied following to the Vsync signal. This is necessary in cases where post-equalization pulses are present. The step size for this control is one Hsync period.

The default is 0.

14 **7 Hsync Detect**
This bit is used to indicate when activity is detected on the Hsync input pin (Pin 30). If Hsync is held high or low, activity will not be detected.

Table XXVII. Hsync Detection Results

Detect	Function
0	No Activity Detected
1	Activity Detected

The sync processing block diagram shows where this function is implemented.

14 **6 AHS – Active Hsync**
This bit indicates which Hsync input source is being used by the PLL (Hsync input or Sync-on-Green). Bits 7 and 1 in this register are what determine which source is used. If both Hsync and SOG are detected, the user can determine which has priority via Bit 3 in register 0EH. The user can override this function via Bit 4 in register 0EH. If the override bit is set to Logic 1, then this bit will be forced to whatever the state of Bit 3 in register 0EH is set to.

Table XXVIII. Active Hsync Results

Bit 7 (Hsync Detect)	Bit 1 (SOG Detect)	Bit 4, Reg 0EH (Override)	AHS
0	0	0	Bit 3 in 0EH
0	1	0	1
1	0	0	0
1	1	0	Bit 3 in 0EH
X	X	1	Bit 3 in 0EH

AHS = 0 means use the Hsync pin input for Hsync.
AHS = 1 means use the SOG pin input for Hsync.

The override bit is in register 0EH, Bit 4.

14 **5 Detected Hsync Input Polarity Status**
This bit reports the status of the Hsync input polarity detection circuit. It can be used to determine the polarity of the Hsync input. The detection circuit's location is shown in the Sync Processing Block Diagram (Figure 12).

Table XXIX. Detected Hsync Input Polarity Status

Hsync Polarity Status	Result
0	Hsync Polarity Is Negative
1	Hsync Polarity Is Positive

14 **4 Vsync Detect**
This bit is used to indicate when activity is detected on the Vsync input pin (Pin 31). If Vsync is held high or low, activity will not be detected.

Table XXX. Vsync Detection Results

Detect	Function
0	No Activity Detected
1	Activity Detected

The Sync Processing Block Diagram (Figure 12) shows where this function is implemented.

14 **3 AVS – Active Vsync**
This bit indicates which Vsync source is being used: the Vsync input or output from the sync separator. Bit 4 in this register determines which is active. If both Vsync and SOG are detected, the user can determine which has priority via Bit 0 in register 0EH. The user can override this function via Bit 1 in register 0EH. If the override bit is set to Logic 1, this bit will be forced to whatever the state of Bit 0 in register 0EH is set.

Table XXXI. Active Vsync Results

Bit 5 (Vsync Detect)	Override	AVS
0	0	0
1	0	1
X	1	Bit 0 in 0EH

AVS = 0 means Vsync input.
AVS = 1 means Sync separator.

The override bit is in register 0EH, Bit 1.

14 **2 Detected Vsync Output Polarity Status**
This bit reports the status of the Vsync output polarity detection circuit. It can be used to determine the polarity of the Vsync output. The detection circuit's location is shown in the Sync Processing Block Diagram (Figure 12).

Table XXXII. Detected Vsync Output Polarity Status

Vsync Polarity Status	Result
0	Vsync Polarity Is Active LOW
1	Vsync Polarity Is Active HIGH

14 **1 Sync-on-Green Detect**
This bit is used to indicate when sync activity is detected on the Sync-on-Green input pin (Pin 49).

Table XXXIII. Sync-on-Green Detection Results

Detect	Function
0	No Activity Detected
1	Activity Detected

The Sync Processing Block Diagram (Figure 12) shows where this function is implemented.

14 **0 Detected COAST Polarity Status**
This bit reports the status of the Coast input polarity detection circuit. It can be used to determine the polarity of the Coast input. The detection circuit's location is shown in the Sync Processing Block Diagram (Figure 12).

Table XXXIV. Detected Coast Input Polarity Status

Hsync Polarity Status	Result
0	Coast Polarity Negative
1	Coast Polarity Positive

This indicates that Bit 1 of Register 5 is the 4:2:2 Output mode select bit.

15 1 **4:2:2 Output Mode Select**
A bit that configures the output data in 4:2:2 mode. This mode can be used to reduce the number of data lines used from 24 down to 16 for applications using YUV, VCbCr, or PbPr graphics signals. A timing diagram for this mode is shown in Figure 9.

Recommended input and output configurations are shown in Table XXXV. In 4:2:2 mode, the Red and Blue channels can be interchanged to help satisfy board layout or timing requirements, but the Green channel must be configured for Y.

Table XXXV. 4:2:2 Output Mode Select

Select	Output Mode
0	4:2:2
1	4:4:4

Table XXXVI. 4:2:2 Input/Output Configuration

Channel	Input Connection	Output Format
Red	V	U/V
Green	Y	Y
Blue	U	High Impedance

2-WIRE SERIAL CONTROL PORT

A 2-wire serial interface control interface is provided. Up to two AD9883A devices may be connected to the 2-wire serial interface, with each device having a unique address.

The 2-wire serial interface comprises a clock (SCL) and a bidirectional data (SDA) pin. The analog flat panel interface acts as a slave for receiving and transmitting data over the serial interface. When the serial interface is not active, the logic levels on SCL and SDA are pulled high by external pull-up resistors.

Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Data on SDA must change only when SCL is low. If SDA changes state while SCL is high, the serial interface interprets that action as a start or stop sequence.

There are five components to serial bus operation:

- Start Signal
- Slave Address Byte
- Base Register Address Byte
- Data Byte to Read or Write
- Stop Signal

When the serial interface is inactive (SCL and SDA are high) communications are initiated by sending a start signal. The start signal is a high-to-low transition on SDA while SCL is high. This signal alerts all slaved devices that a data transfer sequence is coming.

The first 8 bits of data transferred after a start signal comprise a 7-bit slave address (the first 7 bits) and a single R/$\overline{W}$ Bit (the eighth bit). The R/$\overline{W}$ Bit indicates the direction of data transfer, read from (1) or write to (0) the slave device. If the transmitted slave address matches the address of the device (set by the state of the SA_{1-0} input pins in Table XXXIV, the AD9883A acknowledges by bringing SDA LOW on the 9th SCL pulse. If the addresses do not match, the AD9883A does not acknowledge.

Table XXXVII. Serial Port Addresses

Bit 7 A_6 (MSB)	Bit 6 A_5	Bit 5 A_4	Bit 4 A_3	Bit 3 A_2	Bit 2 A_1	Bit 1 A_0
1	0	0	1	1	0	0
1	0	0	1	1	0	1

Data Transfer via Serial Interface
For each byte of data read or written, the MSB is the first bit of the sequence.

If the AD9883A does not acknowledge the master device during a write sequence, the SDA remains high so the master can generate a stop signal. If the master device does not acknowledge the AD9883A during a read sequence, the AD9883A interprets this as "end of data." The SDA remains high so the master can generate a stop signal.

Writing data to specific control registers of the AD9883A requires that the 8-bit address of the control register of interest be written after the slave address has been established. This control register address is the base address for subsequent write operations. The base address autoincrements by one for each byte of data written after the data byte intended for the base address. If more bytes are transferred than there are available addresses, the address will not increment and remains at its maximum value of 14h. Any base address higher than 14h will not produce an acknowledge signal.

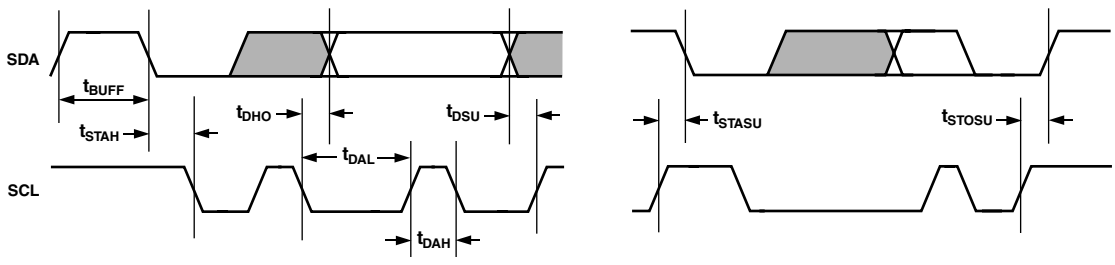


Figure 10. Serial Port Read/Write Timing

Data is read from the control registers of the AD9883A in a similar manner. Reading requires two data transfer operations:

The base address must be written with the R/$\overline{W}$ Bit of the slave address byte LOW to set up a sequential read operation.

Reading (the R/$\overline{W}$ Bit of the slave address byte high) begins at the previously established base address. The address of the read register autoincrements after each byte is transferred.

To terminate a read/write sequence to the AD9883A, a stop signal must be sent. A stop signal comprises a low-to-high transition of SDA while SCL is high.

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

Serial Interface Read/Write Examples

Write to one control register
- Start Signal
- Slave Address Byte (R/$\overline{W}$ Bit = LOW)
- Base Address Byte
- Data Byte to Base Address
- Stop Signal

Write to four consecutive control registers
- Start Signal
- Slave Address Byte (R/$\overline{W}$ Bit = LOW)
- Base Address Byte
- Data Byte to Base Address
- Data Byte to (Base Address + 1)
- Data Byte to (Base Address + 2)
- Data Byte to (Base Address + 3)
- Stop Signal

Read from one control register
- Start Signal
- Slave Address Byte (R/$\overline{W}$ Bit = LOW)
- Base Address Byte
- Start Signal
- Slave Address Byte (R/$\overline{W}$ Bit = HIGH)
- Data Byte from Base Address
- Stop Signal

Read from four consecutive control registers
- Start Signal
- Slave Address Byte (R/$\overline{W}$ Bit = LOW)
- Base Address Byte
- Start Signal
- Slave Address Byte (R/$\overline{W}$ Bit = HIGH)
- Data Byte from Base Address
- Data Byte from (Base Address + 1)
- Data Byte from (Base Address + 2)
- Data Byte from (Base Address + 3)
- Stop Signal

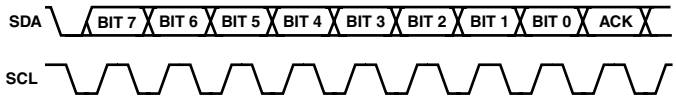


Figure 11. Serial Interface—Typical Byte Transfer

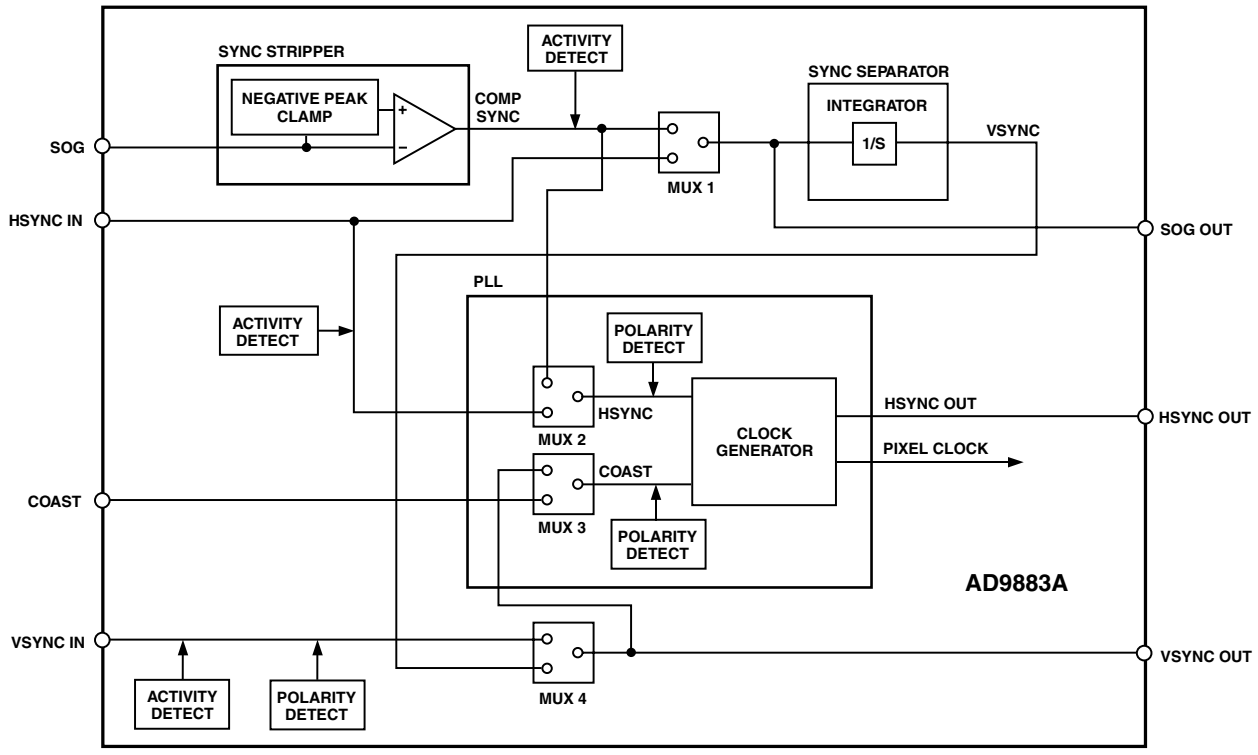


Figure 12. Sync Processing Block Diagram

Table XXXVIII. Control of the Sync Block Muxes via the Serial Register

Mux Nos.	Serial Bus Control Bit	Control Bit State	Result
1 and 2	0EH: Bit 3	0	Pass Hsync
		1	Pass Sync-on-Green
3	0FH: Bit 5	0	Pass Coast
		1	Pass Vsync
4	0EH: Bit 0	0	Pass Vsync
		1	Pass Sync Separator Signal

Sync Slicer
The purpose of the sync slicer is to extract the sync signal from the Green graphics channel. A sync signal is not present on all graphics systems, only those with Sync-on-Green. The sync signal is extracted from the Green channel in a two-step process. First, the SOG input is clamped to its negative peak (typically 0.3 V below the black level). Next, the signal goes to a comparator with a variable trigger level, nominally 0.15 V above the clamped level. The "sliced" sync is typically a composite sync signal containing both Hsync and Vsync.

Sync Separator
A sync separator extracts the Vsync signal from a composite sync signal. It does this through a low pass filter-like or integrator-like operation. It works on the idea that the Vsync signal stays active for a much longer time than the Hsync signal, so it rejects any signal shorter than a threshold value, which is somewhere between an Hsync pulsewidth and a Vsync pulsewidth.

The sync separator on the AD9883A is simply an 8-bit digital counter with a 5 MHz clock. It works independently of the polarity of the composite sync signal. (Polarities are determined elsewhere on the chip.) The basic idea is that the counter counts up when Hsync pulses are present. But since Hsync pulses are relatively short in width, the counter only reaches a value of N before the pulse ends. It then starts counting down eventually reaching 0 before the next Hsync pulse arrives. The specific value of N will vary for different video modes, but will always be less than 255. For example with a 1 µs width Hsync, the counter will only reach 5 (1 µs/200 ns = 5). Now, when Vsync is present on the composite sync the counter will also count up. However, since the Vsync signal is much longer, it will count to a higher number M. For most video modes, M will be at least 255. So, Vsync can be detected on the composite sync signal by detecting when the counter counts to higher than N. The specific count that triggers detection (T) can be programmed through the serial register (0fh).

Once Vsync has been detected, there is a similar process to detect when it goes inactive. At detection, the counter first resets to 0, then starts counting up when Vsync goes away. Similar to the previous case, it will detect the absence of Vsync when the counter reaches the threshold count (T). In this way, it will reject noise and/or serration pulses. Once Vsync is detected to be absent, the counter resets to 0 and begins the cycle again.

PCB LAYOUT RECOMMENDATIONS

The AD9883A is a high precision, high speed analog device. As such, to get the maximum performance out of the part it is important to have a well laid out board. The following is a guide for designing a board using the AD9883A.

Analog Interface Inputs
Using the following layout techniques on the graphics inputs is extremely important.

Minimize the trace length running into the graphics inputs. This is accomplished by placing the AD9883A as close as possible to the graphics VGA connector. Long input trace lengths are undesirable because they will pick up more noise from the board and other external sources.

Place the 75 Ω termination resistors (see Figure 1) as close to the AD9883A chip as possible. Any additional trace length between the termination resistors and the input of the AD9883A increases the magnitude of reflections, which will corrupt the graphics signal.

Use 75 Ω matched impedance traces. Trace impedances other than 75 Ω will also increase the chance of reflections.

The AD9883A has very high input bandwidth (500 MHz). While this is desirable for acquiring a high resolution PC graphics signal with fast edges, it means that it will also capture any high frequency noise present. Therefore, it is important to reduce the amount of noise that gets coupled to the inputs. Avoid running any digital traces near the analog inputs.

Due to the high bandwidth of the AD9883A, sometimes low pass filtering the analog inputs can help to reduce noise. (For many applications, filtering is unnecessary.) Experiments have shown that placing a series ferrite bead prior to the 75 Ω termination resistor is helpful in filtering out excess noise.

Specifically, the part used was the #2508051217Z0 from Fair-Rite, but each application may work best with a different bead value. Alternately, placing a 100 Ω to 120 Ω resistor between the 75 Ω termination resistor and the input coupling capacitor can also benefit.

Power Supply Bypassing
It is recommended to bypass each power supply pin with a 0.1 µF capacitor. The exception is in the case where two or more supply pins are adjacent to each other. For these groupings of powers/grounds, it is only necessary to have one bypass capacitor. The fundamental idea is to have a bypass capacitor within about 0.5 cm of each power pin. Also, avoid placing the capacitor on the opposite side of the PC board from the AD9883A, as that interposes resistive vias in the path.

The bypass capacitors should be physically located between the power plane and the power pin. Current should flow from the power plane to the capacitor to the power pin. Do not make the power connection between the capacitor and the power pin. Placing a via underneath the capacitor pads, down to the power plane, is generally the best approach.

It is particularly important to maintain low noise and good stability of PV_D (the clock generator supply). Abrupt changes in PV_D can result in similarly abrupt changes in sampling clock phase and frequency. This can be avoided by careful attention to regulation, filtering, and bypassing. It is highly desirable to provide separate regulated supplies for each of the analog circuitry groups (V_D and PV_D).

Some graphic controllers use substantially different levels of power when active (during active picture time) and when idle (during horizontal and vertical sync periods). This can result in a measurable change in the voltage supplied to the analog supply regulator, which can in turn produce changes in the regulated analog supply voltage. This can be mitigated by regulating the analog supply, or at least PV_D, from a different, cleaner power source (for example, from a 12 V supply).

It is also recommended to use a single ground plane for the entire board. Experience has repeatedly shown that the noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental because each separate ground plane is smaller, and long ground loops can result.

In some cases, using separate ground planes is unavoidable. For those cases, it is recommended to at least place a single ground plane under the AD9883A. The location of the split should be at the receiver of the digital outputs. For this case it is even more important to place components wisely because the current loops will be much longer (current takes the path of least resistance). An example of a current loop:

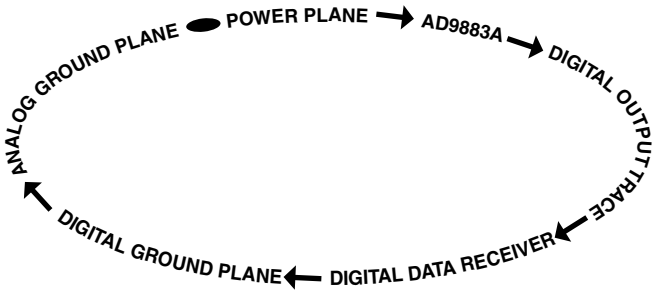


Figure 13. Current Loop

PLL
Place the PLL loop filter components as close to the FILT pin as possible.

Do not place any digital or other high frequency traces near these components.

Use the values suggested in the data sheet with 10% tolerances or less.

Outputs (Both Data and Clocks)
Try to minimize the trace length that the digital outputs have to drive. Longer traces have higher capacitance, which requires more current, which causes more internal digital noise.

Shorter traces reduce the possibility of reflections.

Adding a series resistor of value 50 Ω to 200 Ω can suppress reflections, reduce EMI, and reduce the current spikes inside of the AD9883A. If series resistors are used, place them as close to the AD9883A pins as possible (although try not to add vias or extra length to the output trace in order to get the resistors closer).

If possible, limit the capacitance that each of the digital outputs drives to less than 10pF. This can easily be accomplished by keeping traces short and by connecting the outputs to only one device. Loading the outputs with excessive capacitance will increase the current transients inside of the AD9883A creating more digital noise on its power supplies.

Digital Inputs
The digital inputs on the AD9883A were designed to work with 3.3 V signals, but are tolerant of 5.0 V signals. So, no extra components need to be added if using 5.0 V logic.

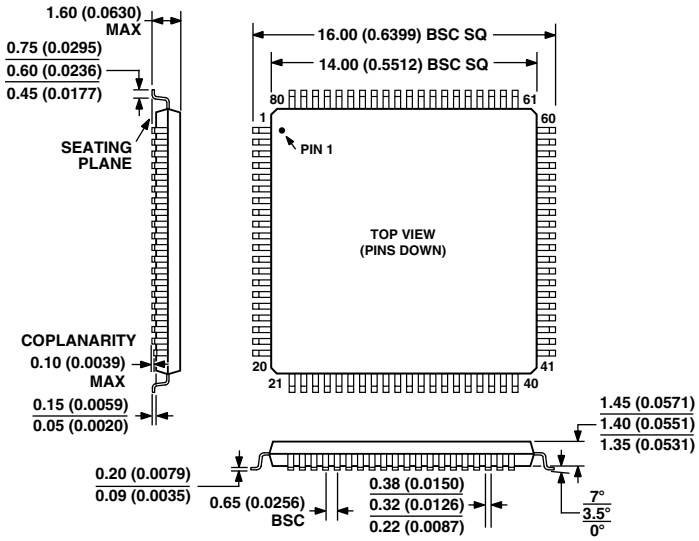
Any noise that gets onto the Hsync input trace will add jitter to the system. Therefore, minimize the trace length and do not run any digital or other high frequency traces near it.

Voltage Reference
Bypass with a 0.1 µF capacitor. Place as close to the AD9883A pin as possible. Make the ground connection as short as possible.

OUTLINE DIMENSIONS

Dimensions shown in millimeters and (inches)

80-Lead Thin Plastic Quad Flatpack [LQFP]
(ST-80)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

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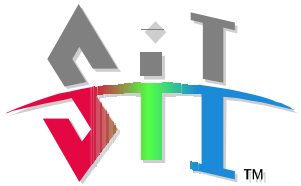

Silicon Image, Inc

PanelLink™ Technology

EMC Design Application Note
LCD Monitor & Notebook Applications
Revision B

Silicon Image, Inc.

Revision B
April 21, 1998

SiI/AN-0003-B

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1. INTRODUCTION

The purpose of this document is to provide you with basic mechanical and PCB layout guidelines to address EMC issues that they apply to LCD flat panel display applications. This document does not guarantee compliance with international emissions standards, but serves as a guideline to help minimize basic design flaws in the initial design. As with any other type of engineering, EMC designs will usually require 2 or more iterations to achieve the final production form. The goal of this document is to help reduce the number of iterations.

This document will go into some detail about electro-magnetics and material properties, but only to the extent necessary to convey the purpose or theory behind a given situation. This document focuses mostly on LCD monitor applications, but has special sections that apply to notebook applications. Basic EMI and ESD system-level design guidelines for PanelLink applications will be covered herein.

2. MECHANICAL CONSTRUCTION

LCD monitor designers do not have the extreme size and weight constraints that notebook computer designers do, but they are still limited by the market expectations of a thin, lightweight flat panel display.

Many times the mechanical construction of an electronic device is ignored for EMC purposes since the prevailing belief is that EMI/EMC is strictly an electronic issue. This is simply not the case. In most instances, mechanical design comprises one half of the EMC solutions applied to failing systems. Saving a few pennies here and a few ounces there may seem attractive at first, but if the end results are cost overruns and schedule delays due to EMC issues, the savings are more than canceled out. If you are developing a new product i.e. not a revision of an existing product, it would be better to save the cost in a cost-reduced product after the original is already in production. ***Do not overlook the importance of the mechanical design on the system's EMC performance.***

2.1. Using Conductive Plastics and Coated Plastics

Conductive plastics are plastics which have been doped with various materials to make them electrically conductive. Coated plastics are standard plastics that have been coated with conductive coatings or paints applied to their surfaces to make them effective reflectors of low impedance RF energy. Both types are discussed below:

Conductive Plastics: Conductive Plastics can be effective shields, *but only in limited cases*. Without going into the details of near field wave analysis, it is important to realize that conductive plastics are only effective against **electric fields.** This is true because the high wave impedance of an electric field in the near field allows a relatively high impedance material (~100Ω/❑) such as conductive plastic to act as an effective shield for electric fields. Of course in an assembly this is true only if the different pieces of the enclosure are in good electrical contact with each other. Unfortunately, electric fields are only generated by high voltage, low-current situations which are not prevalent in today's electronics. Furthermore, if conductive plastic is used as a ground path between two assembles, the high surface resistance of the plastic offers too great an impediment to RF currents and creates an RF potential difference between them, usually resulting in enhanced radiation. The high impedance of the plastic can be utilized to reduce the

magnitude of personnel generated ESD currents that occur during use. However, from an high frequency (>1 MHz) electromagnetic standpoint, *conductive plastic is not presently useful as a shield and will remain so until the conductive plastic's surface resistance can be reduced to below 0.1* W/❑.

Coated Plastics: Most present-day electronic systems are generally low voltage (3.3-5.0V) high current systems and generate mostly high frequency **magnetic fields.** For reasonable shielding, a material is required to have a surface resistance that is less than 50 milli-Ω/❑ **at the frequencies of interest** and to be at least 0.03 mm thick in order to be effective. Presently there are coatings that meet these criteria. Among them are silver coated copper particle paints that measure less than 50 milli-Ω/❑ at .03 mm which have successfully been used as RF image planes and shields. They are not useful as heat sinks and have had only limited success as ground paths between assembles separated by more than 3 cm when significant signal return currents (>10 mA) are flowing.

Coated plastics can be quite effective for purposes of magnetic field shielding, but certain precautions must be taken:

⇒ The conductive plating should be connected (referenced) to the chassis ground through multiple contact points.

⇒ The conductive plating should not be directly grounded to a PCB ground plane close to any high speed components. Ideally, the conductive plating should be grounded to the chassis which is then connected to the PCB ground. See Figure 3.

⇒ Most plastic enclosures come in several pieces which fit together. Usually the seam joints of these parts make very poor electrical contact with each other due to small imperfections in the plastics. Not only does this create a leaky shield, but it greatly reduces the shielding effectiveness of any isolated pieces. Use copper spring fingers in several places to make good electrical contact between the front and back shells and make sure the seam joints have significant overlap to reduce EMI leaks. See Section 2.3.

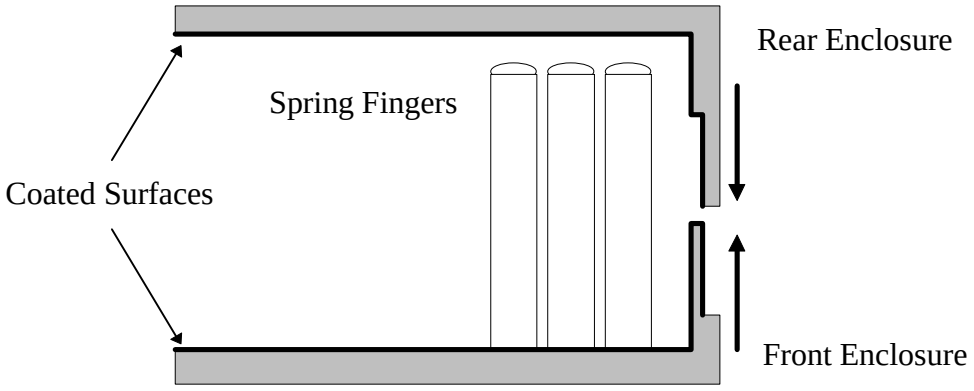


Figure 1: Creating Good Contact and Preventing Leaks with Coated Plastics

Summary: For magnetic field emissions (which is probably the main concern for the type of systems discussed in this document), effective shielding is accomplished by allowing the magnetic fields to induce currents in the shielding. **Conductive plastics are ill-suited for this role and should not be depended on for shielding or ground contacts due to their high impedance at RF**. This is not to say that they cannot be used to minimize ESD currents, but they should not be relied upon as a ground, a shield, or treated as a true metallic conductor. The most effective high frequency shielding material for most purposes is non–ferrous, low resistance (less than 5 milli-ohms per square) metal, preferably copper. The

second most effective high frequency shielding materials are low surface resistance coatings (less than 50 milli-ohm per square at 0.03 mm thick) such as silver coated copper particle paint.

2.2. Metal Chassis

A metal chassis which has good electrical contact to the main ground reference is the best situation to have for shielding and a return path for induced currents. Many times, this role can be "doubled-up" with metal in the system that is used for another purpose, such as heat sinks or mounting plates. The ideal situation would be to create a Faraday cage around the entire system. This can be accomplished through a combination of the main system chassis, the overall cable braid/shield, and the display chassis.

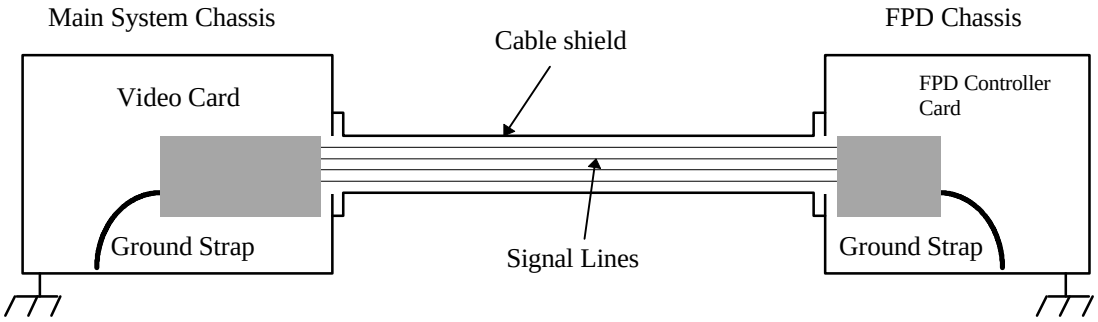


Figure 2: Overall chassis and shield configuration (Ideal situation)

The purpose of this Faraday cage is two-fold. The first is to provide a "cold" RF potential reference for the entire system, i.e. a ground reference for the ground planes. The second is to contain any emissions within the boundaries of the chassis and shield by either reflecting the noise off the metal walls and/or inducing a return current in the shield which flows back to the source, canceling the emission. *It is for both these reasons that the shield/chassis should never intentionally be used as a ground plane or return line for signals*. This is especially true for the cable shield which is the most susceptible to causing radiation. Signal lines in the cable must have their own return lines within the cable bundle. The cable shield must be free of signal related currents since its purpose is to contain common-mode or other uncompensated noise propagating on the internal wires.

Here are some basic guidelines for grounding the shielding and chassis:

- ⇒ Never ground the cable shield or connector shell directly to a PCB ground plane. Ground planes can contain a lot of noise currents which will contaminate the shield.
- ⇒ The PCB grounds should be terminated to the main chassis at several points making sure that the contact points on the PCB are not too close to any high speed IC's (within ~4cm).
- ⇒ The cable shield and connector shells should be terminated to the chassis. The idea behind this is to make the chassis the common RF ground potential to which all circuits are referenced. Choose one chassis to be the MAIN reference (usually the host system chassis) and contact everything else to it through a low impedance path. In the case of the monitor chassis, this is connected back to the main chassis through the cable shielding. If possible, also terminate the monitor chassis to earth ground as well to give it a direct reference to the main chassis reference. This is illustrated in Figure 3 below.

⇒ Any conductive coatings should be treated as a cable shield, not as a metal chassis. As such, *do not ground any conductively coated plastics directly to the PCB ground planes*. Conductive coatings should be terminated to the chassis as in the case of the cable shields.

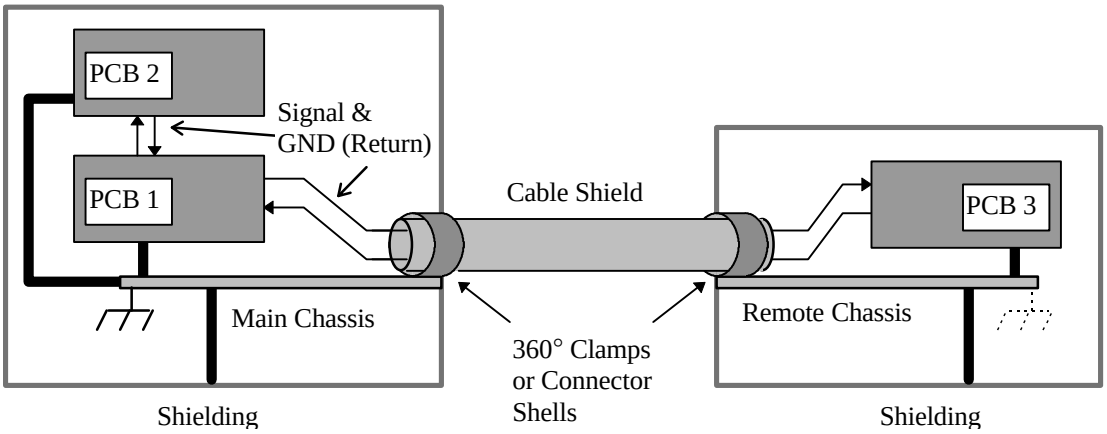


Figure 3: Chassis Grounding Scheme

Note above that every signal must have a return line (GND) and would preferably have more than one to reduce the return line impedance. The reason is that if no low-impedance return line is provided, the signal has no option but to return to the source through the chassis, cable shield, or through the air (radiation). The dark lines above represent ground straps or metal standoffs which provide numerous contacts to the chassis.

In a simplified drawing, the overall scheme should be each electrical component having direct reference to the chassis ground, not through another component:

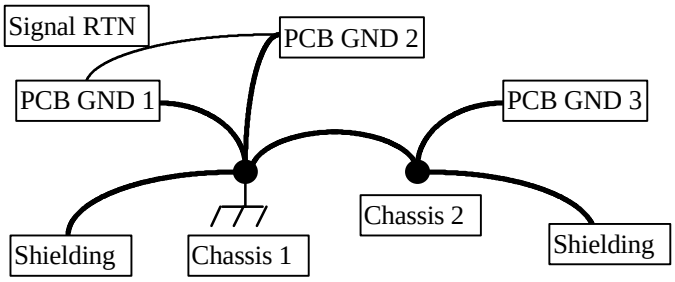


Figure 4: Single Point Grounding for Monitors

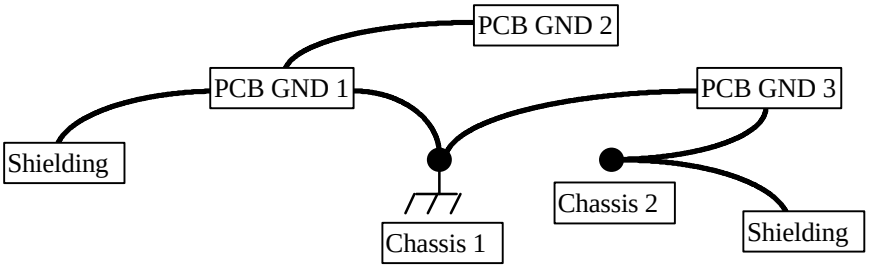


Figure 5: Improper Grounding Scheme

In Figure 4, the grounding scheme assumes that the contact between Chassis 1 and Chassis 2 is low impedance effectively forming a single chassis. A properly terminated cable shield is not zero impedance, but is as good as is practically possible and can be used for this purpose. Also note that the ground RETURN lines for signals between PCBs go directly between the PCBs (not through the chassis) to provide a direct return for signal currents. This minimizes the currents that return through the chassis.

Figure 5 illustrates an improper way of terminating shields and ground planes. The issue with this scheme is that return currents induced in the shield from PCB 2, for example, have to return through PCB 1. This type of situation can cause interference as well as emissions problems.

Finally, it is very common to use the terms “GROUND” and “RETURN” interchangeably when they are in fact not the same thing. They may be both tied to the same DC potential, but their purposes are very different. The chassis GROUND is the absolute potential reference for the system, the signal RETURNS or “grounds” are tied to the ground reference, but their primary function is to provide a current return for signal currents.

2.3. Apertures

The reality is that an ideal Faraday cage is a near impossibility. Real enclosures are not completely sealed and cannot be due to thermal requirements, connector openings, and service accessibility requirements. However, if certain guidelines are followed, a practical EMI enclosure can be constructed and still perform as a very effective shield.

In any practical system enclosure, there must be holes made in the metal to provide ventilation and exit points for I/O connectors. What is important for shield effectiveness is to remember that what makes the shield leaky is the longest *linear* dimension that is open, not the largest area. For example:

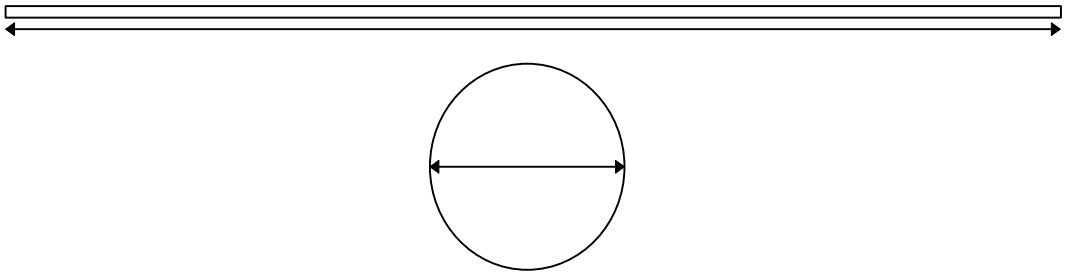


Figure 6: Shield aperture comparison

The aperture shown at the top of Figure 6 is a much more leaky opening than the large circular hole shown at bottom since its longest linear opening is much wider. Therefore, one must be careful of large seams since a poor contact along two long pieces of metal can leave a very large opening.

In the case of a lid for an enclosure, there are generally two ways to seal off the seams: 1) use EMI gaskets, 2) increase the depth of the contact seam. The first option usually involves beryllium-copper spring fingers which can be more expensive and difficult to manufacture. Increasing the seam depth is illustrated below:

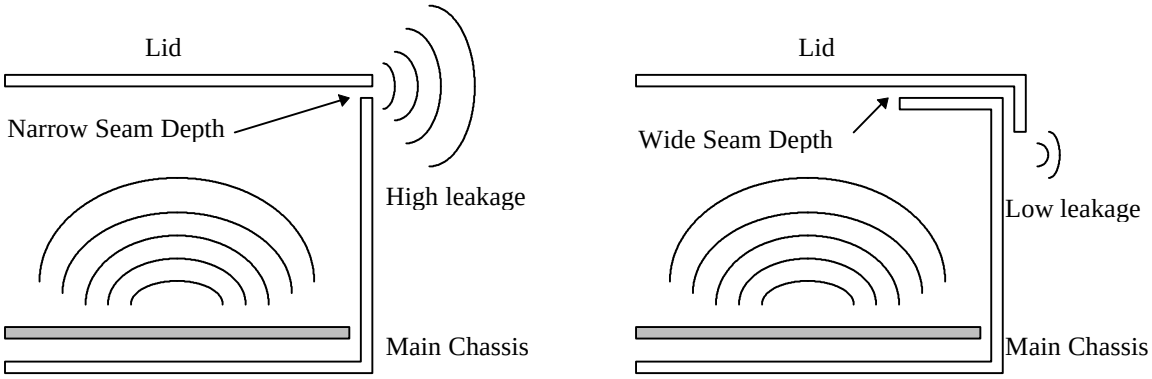


Figure 7: Seam depth and shield leakage

The reason there is much lower leakage from the enclosure on the right is that emissions from the PWB on the inside must pass through the "waveguide" of the folded metal seam. Waves emitted on the inside must reflect back and forth between the lid and main chassis numerous times before exiting the seam. The signal is attenuated with each reflection and is significantly reduced by the time it reaches the opening.

If a very tight EMI seal is required, you can either screw together the lid and chassis at close intervals (2" or less), or you can place EMI gaskets (spring fingers) between the lid and chassis as shown below:

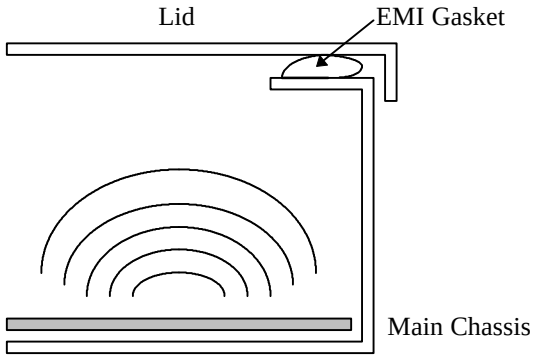


Figure 8: Use of EMI Gaskets

As mentioned earlier, it is the linear dimension, not the area that defines how much radiation escapes the enclosure. Given that, it is better to have many small holes, than one big one. There are two reasons for this. First of all, the obvious reason is that the larger hole will let more radiation out, but the second less obvious reason is that a single large hole requires any return current that happens to be flowing on the chassis to route itself around this opening. The larger the opening, the larger the deviation resulting in a higher impedance. The end result is a significantly less effective shield.

2.4. Hinges (Notebook PC Applications)

A common problem that is seen in notebook designs is the electrical separation of the flat panel chassis from the main system chassis. Often this separation is unintentional since the designer has assumed

electrical contact through either the hinges and/or the conductive plastic. *Neither of these provide acceptable conductivity at high frequencies*. Hinges should be treated mainly as a mechanical pivot which allows the display to fold downward and close the notebook computer, not as an electrical connection between the panel and system chassis grounds.

The LCD panel in a notebook should be treated similarly to the LCD monitor as shown in Figures 2-4. The panel chassis and main system chassis should be tied together as well as possible:

⇒ Make multiple contact points between the main ground planes of the LCD controller board and main system boards to the metal or conductively coated chassis of each. These contact points should not be near (within 4cm) high speed IC's. This helps insure that induced return currents are given a low impedance return to their sources.

⇒ Provide low RF impedance contact between the panel chassis and main system chassis. This low impedance connection should be provided by a low impedance metallic contact (other than the hinges), preferably by a wide strip (1 cm width or more) of copper. It is possible to provide this contact with the shielding of the signal cables routed between the main system and the flat panel display (see section 2.3 Signal Cables).

There are a few special considerations to look out for:

⇒ Do not use the chassis as the deliberate return path for signals or as a ground plane. Using the chassis as a ground plane introduces this noise onto the chassis ground which may in turn inject this noise onto the cable shielding that is terminated to it. For more details on grounding, see section 3.2 Ground Planes.

⇒ Cable shields should be terminated to chassis ground. Do not terminate any of the cable shields to the ground plane of the motherboard. Ground planes are direct return paths for signals and may have significant noise or "ground bounce." Connecting cable shields to this will inject common mode noise onto the shields and cause radiation. Chassis grounds are relatively "cold" grounds which provide return paths for currents induced on shielding.

⇒ As was noted several times before, hinges and conductive plastic do ***not*** make good contact at high frequencies and should not be the sole connection between the flat panel and main system chassis grounds.

2.5. Signal Cables

Signal cables are the most efficient radiators in an electrical system since a cable is very similar to an antenna. Cables need to be used carefully and have their length minimized wherever possible. Many flat panel displays have their controller hardware mounted at the top of the display which is undesirable due to the increased cable length. If possible, locate the panel controller hardware at the bottom of the display to minimize cable length. Also, due to their high radiating efficiency, all cables should be shielded (flat cable and twisted pair) and have space allowances for ferrite beads both in the system enclosure and at the controller. Additionally, the cable should be mechanically constrained to lie as close to the chassis metal (or coating) as possible. This will further reduce the cable's ability to act as an antenna. Refer to sections 3.4 and 3.5.

For every signal and power line in the cable, there should be at least one corresponding return line, as illustrated below:

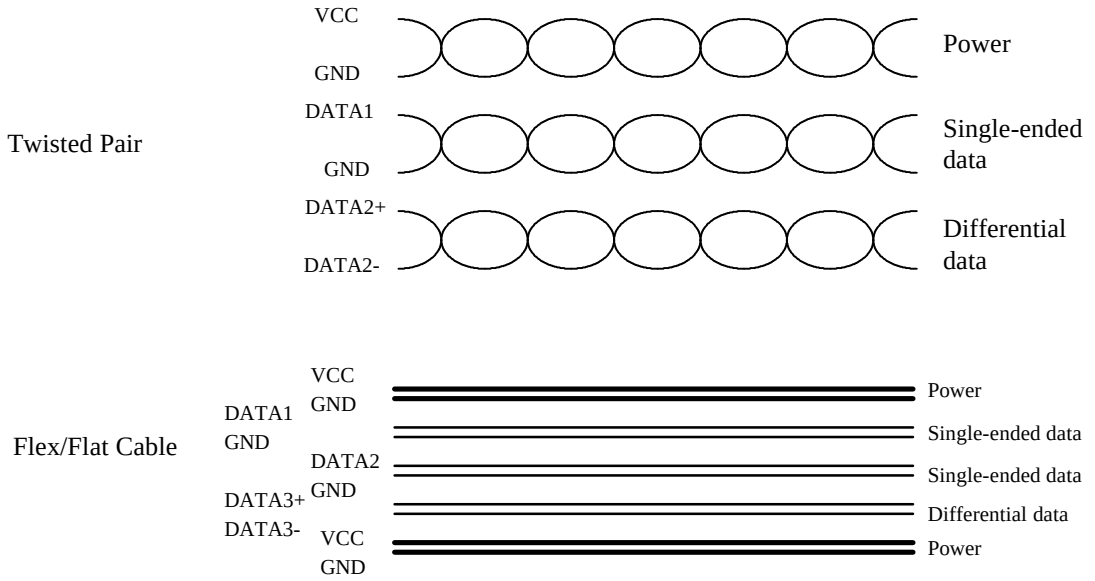


Figure 9: Signal and return line pairing

The +/- data shown above indicates differential signals whereas data coupled with a GND line indicates single-ended signaling.

Wherever possible, there should be multiple parallel power/ground lines to insure that enough current can be supplied to the display, and reduce the return path impedance. If there are any unused pins, connect them to the system/FPD ground reference (NOT chassis ground). All power lines should be filtered before exiting on the cable (See Section 3.4).

Applying shielding to the cable(s) is an important, but somewhat confusing exercise. The designer should be careful to connect each part of the shield to the appropriate location on the system and be careful to not confuse the signal return with a shield. For example, mini-coax is often used for sending signals. Coaxial cable consists of an inner signal conductor, a dielectric surrounding the inner conductor, and an outer braid enclosing that dielectric as shown below:

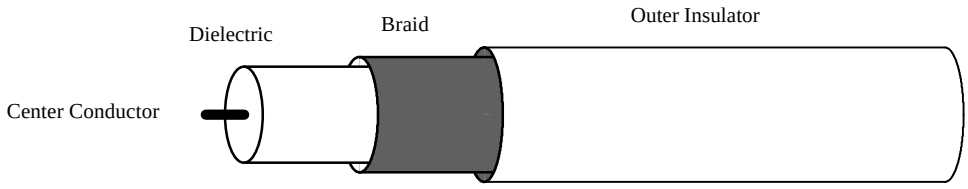


Figure 10: Typical coaxial cable

The braid shown in Figure 10 is a signal return not a shield. Thus you should not consider the above cable to be shielded because:

⇒ There will be common-mode currents on both the braid and center since the braid will be connected to the ground plane.

⇒ The braid is likely terminated in a long twisted wire ("pig-tail")" that greatly increases the impedance of the signal return and common-mode noise as well.

Common-mode currents occur very often and need not be very large to cause very high emissions. A common-mode current on the order of a few micro-amperes or less is enough to cause emissions high enough to fail CISPR22 B if left unshielded. "Pig-tail" braid terminations are common in high density signal connectors and are not always avoidable. Therefore it is often (almost always) necessary to have an overall shield that encloses the entire signal cable bundle. A preferred configuration for a cable bundle is illustrated below:

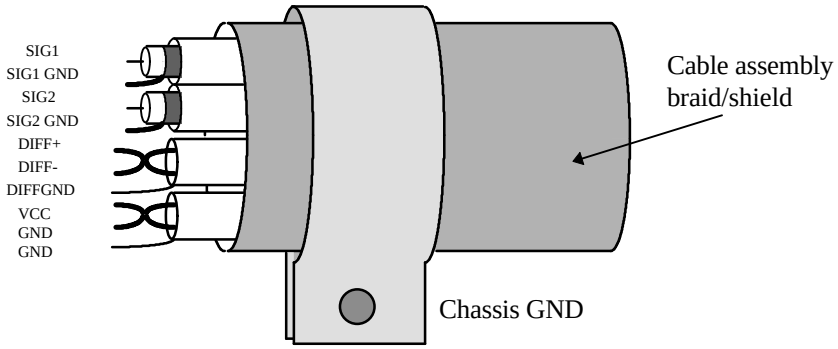


Figure 11: Cable shield termination

This cable assembly should be terminated (RF Bonded) as shown above at both the flat panel and main system chassis. The clamp used to contact the overall shield should have as large a contact area as possible with the chassis and shield, preferably a 360° contact. Using only the fasteners as contact points to the chassis will significantly lower the shielding effectiveness and is NOT recommended. Using a "pig-tail" on the overall exterior shield is NOT recommended. Space should be made for a 360° clamp for the best RF contact. Pig-tails are very inductive and will significantly compromise and most probably will destroy the effectiveness of the shield. In addition, since this overall shield also serves as a low inductance connection between the panel and system chassis grounds, any additional inductance here will further degrade EMI performance by introducing a significant RF potential difference between the two chassis grounds. The pig-tails on the small inner coax lines should be as short as possible or eliminated altogether if special connectors are available. The twisted pair lines may be shielded or non-shielded, but are shown with individual shields just for illustration purposes.

If flat ("flex") cables are used in the system, a similar configuration can be used. It is preferable that copper planes be used to connect the flat panel chassis and the main system chassis and the flat cable shields can be used for this purpose. In order to limit the number of layers in the flat cable to keep flexibility, a three layer design is recommended (if concerns about flex endurance dictate, only the bottom layer of the shield should be used):

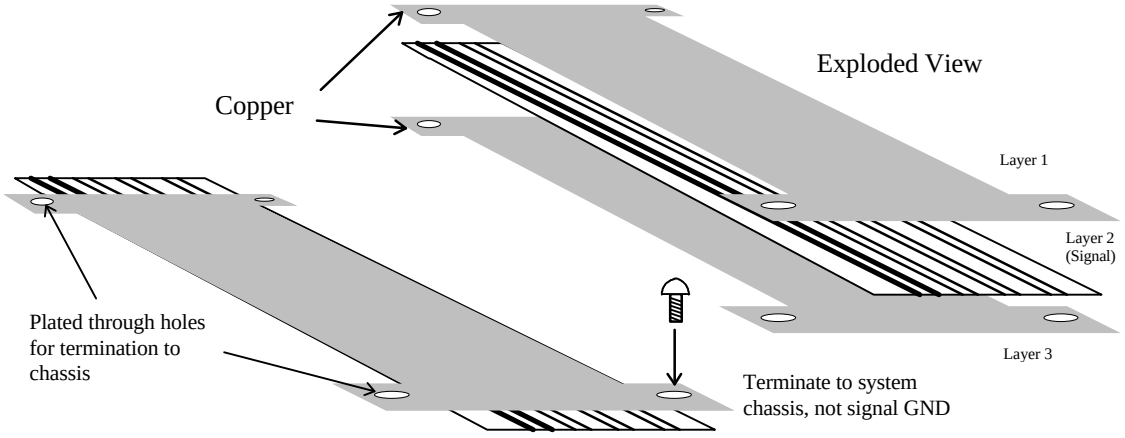


Figure 12: Three-layer FPC (flex cable)

The flat cable has the signal and power lines enclosed between two solid copper layers which comprise the shield of the cable. This shield should NOT be used as a ground for signals carried on the cable. Each signal line should have a closely coupled (i.e. physically close) ground/return line. Also, any power lines carried on the cable should have its ground/return located physically close to it on a separate trace on the signal layer—Note: .065 inch traces on .075 inch centers will have a 25 ohm characteristic impedance. The shield itself should be terminated to the chassis (on both the panel and system ends) and NOT to the ground planes of the panel or system PCBs. Although the ground planes do contact the chassis as mentioned in Section 2.2, connecting the cable shield to the chassis is NOT the same as connecting it to the ground planes directly. This is because there may be noise on the ground planes and connecting the shield to those grounds will contaminate the shield with that noise. By connecting the shield to the chassis, any noise on the power or signal lines induces reverse currents in the shield which return to the source therefore reducing the (common mode) current entering the shield and causing emissions. Depending on the system design, common mode chokes may be needed on the signal and clock lines. Power lines must be filtered at the connector, preferably with a low pass filter and/or a two wire common mode choke. See Section 3.4 Filtering for more detail on filters and CM chokes.

2.6. Contact Points

Once a proper shielding configuration has been established for the signal cables, it is important to insure that they are connected to the rest of the system correctly. Although, this has been stated in the previous section, this section will provide examples of how the system chassis grounds, shields, and cables should be connected to one another.

In the case of a system using twisted pair signal lines shielded by an overall braid shield, the signal lines should be connected as shown in the beginning of Section 2.3. The overall system configuration should look something like the following:

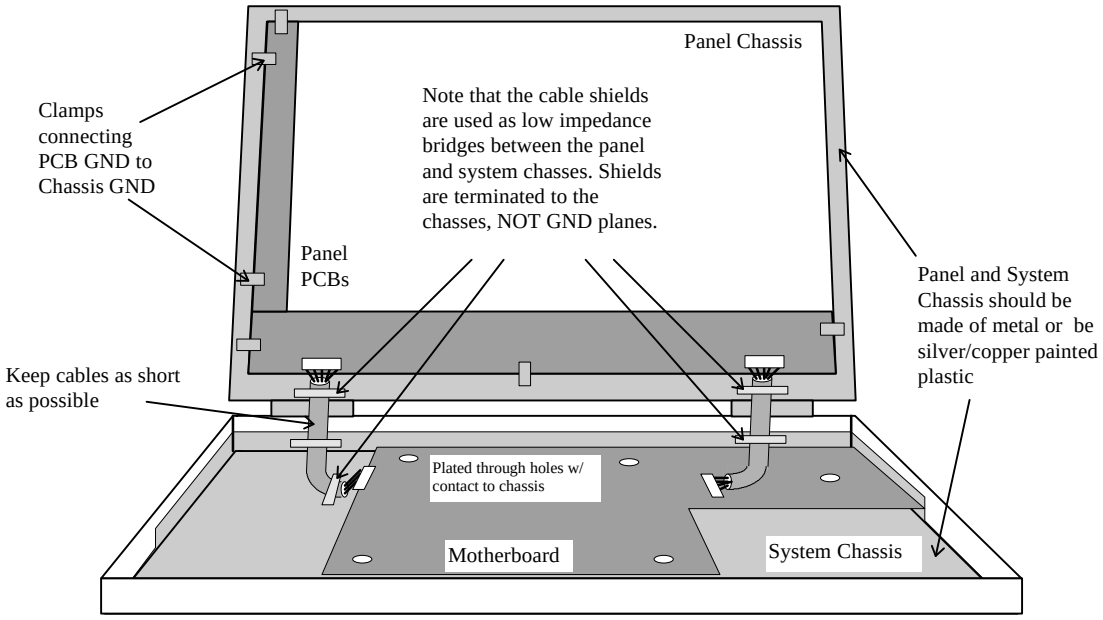


Figure 13: Chassis connection points for notebook PCs

The configuration for a system using flat cables is very similar except that instead of using metal clamps to terminate the shield to the system chassis, the plated-through mounting holes shown in Figure 12 are used to terminate the flat cable shield. Note that this is a direct implementation of the architecture shown in Figures 2-4.

The figure above is the same electrical configuration shown in the LCD monitor example shown in Figure 3, but is illustrated here in a notebook application to show a different arrangement of the same configuration.

The motherboard as well as the panel PCBs must make good ground contact with the chassis through multiple contact points with a few caveats:

⇒ In notebook designs, the chassis is generally made of light gauge material to save weight so it is very important that the chassis contact points are not near any chips with high speed clocks since this can cause a significant amount of local ground noise. It does not matter if the clocks are not even routed outside the chip since the internal clock can create noise through its ground or power pins.

⇒ Any additional shielding (conductive coatings, metalized mylar, etc.) should be terminated to the chassis, NOT a PCB ground plane.

In addition, the designer must be careful to not use the chassis as a ground plane or intentionally route return currents onto the chassis:

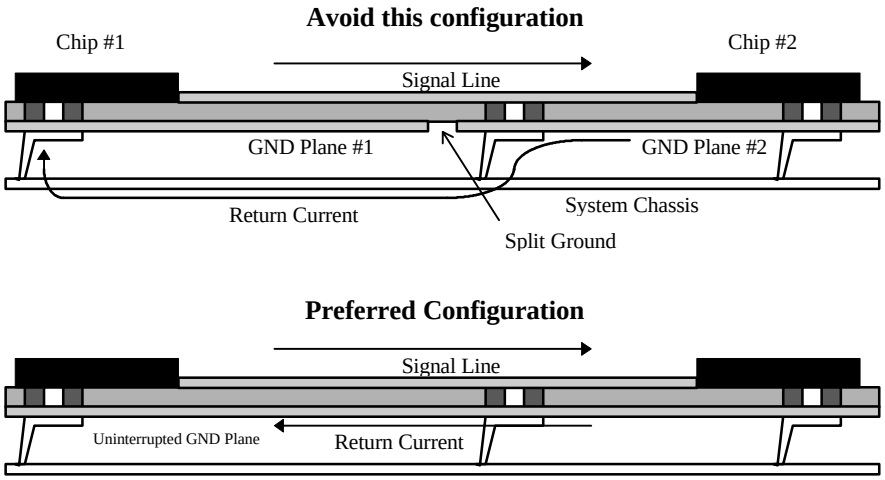


Figure 14: Broken Ground Planes

Although it is sometimes necessary to have separate ground planes, in most cases it is better (and easier) to have a single ground plane. That way it is easy to insure that a signal line is not routed over a break in the ground plane/return path. The mechanical designer should coordinate with the system layout designer to insure that the situation shown at the top of Figure 7 does not occur. Signal return currents inadvertently or deliberately traveling on the chassis may cause it to radiate. For more information on ground planes, see Section 3.2 Ground Planes.

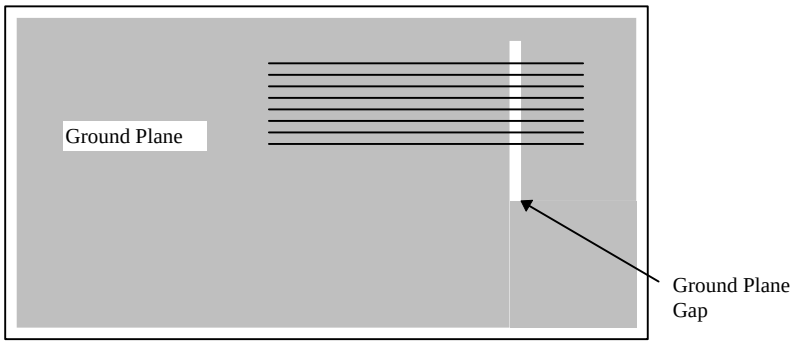


Figure 15: Gapped Ground Plane (see 3.2)

Signal traces run over a gap will cause increased ground bounce and increase common mode current generation at ALL I/O connectors.

2.7. Summary

The figure below is an example illustrating some of the mechanical guidelines described in this section.

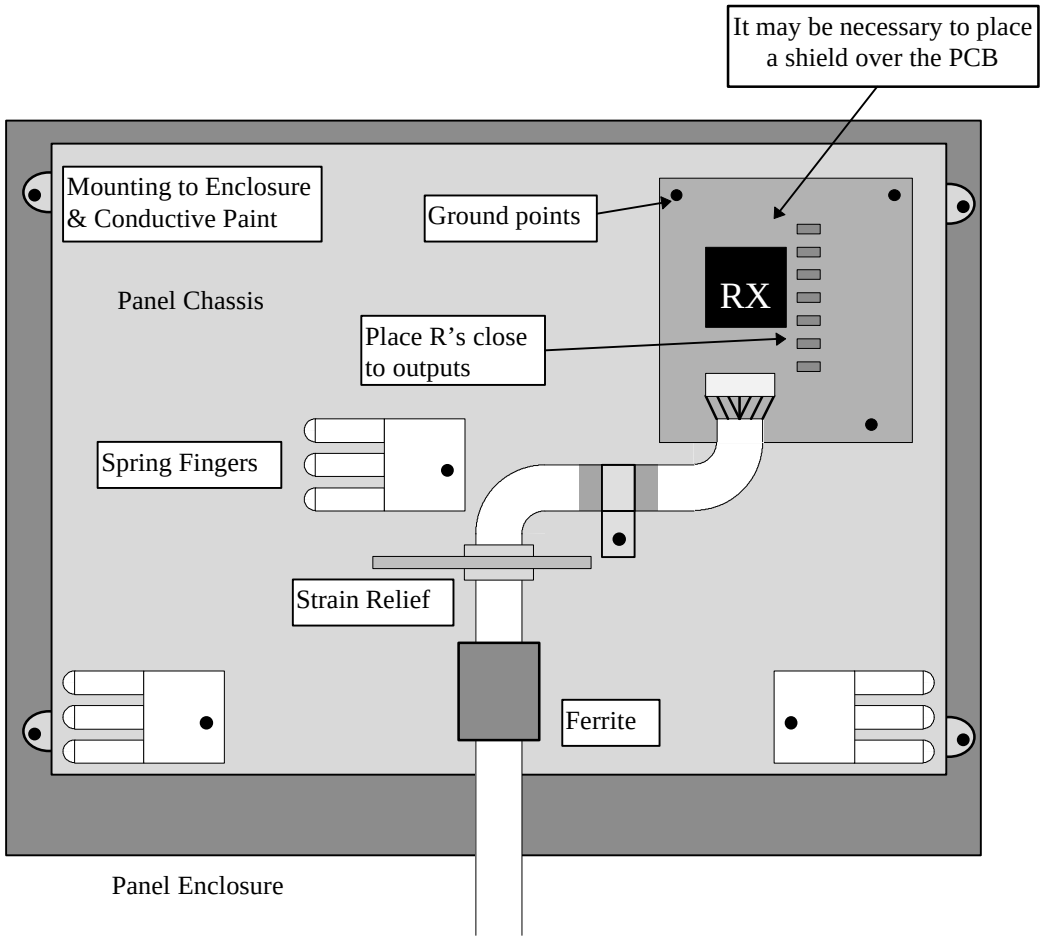


Figure 16: LCD Monitor Example

Conductive Plastics

⇒ The use of conductive plastic does not hurt, but it should NOT be relied upon as the primary shield or chassis ground. Conductive plastic helps reduce electric field emissions and ESD currents, but it is ineffective for general shielding purposes. Shielding must be metal, preferably copper or a low impedance plastic coating.

Metal chassis and hinges

⇒ The chassis of the main system and panel should have many contacts to their PCB main ground planes.

⇒ The hinges should NOT be relied upon to provide electrical contact between the main system and flat panel display chassis. There should be low impedance electrical contacts (flat wide bonds) between the panel and system chassis to reduce the RF potential between them.

⇒ Cable shields should be terminated to the chassis ground.

⇒ All metal backings and supports in the display must be RF bonded to its chassis frame, and All metal backings and supports of component assemblies mounted over the counterpoise or image plane of the main chassis must be RF bonded to it.

Signal Cables

⇒ Each signal should be paired with its appropriate return line as closely as possible to establish maximum mutual inductance. This would be the signal's ground line (if single-ended), or its opposite differential line if double ended.

⇒ Power lines should be paired with their return line as closely as possible to establish maximum mutual inductance.

⇒ Cables should be shielded if possible. The cable shield should be terminated to the panel and display chassis at both the panel and system ends and as close to the cable connectors as possible.

⇒ If shielding is not possible, make sure that a single common mode choke is used on all signal and clock lines and that common mode filtering is also applied to the power lines (see section 3.4 Filtering).

Contact Points

⇒ As mentioned above, the panel chassis should have a good metallic contact (RF bond) with the main system chassis other than the hinges.

⇒ Cable shields should directly contact the panel and system chassis near the cable connectors.

⇒ The motherboard and panel controller PCBs should have good contact with the chassis ground, but not use the chassis grounds as signal return paths.

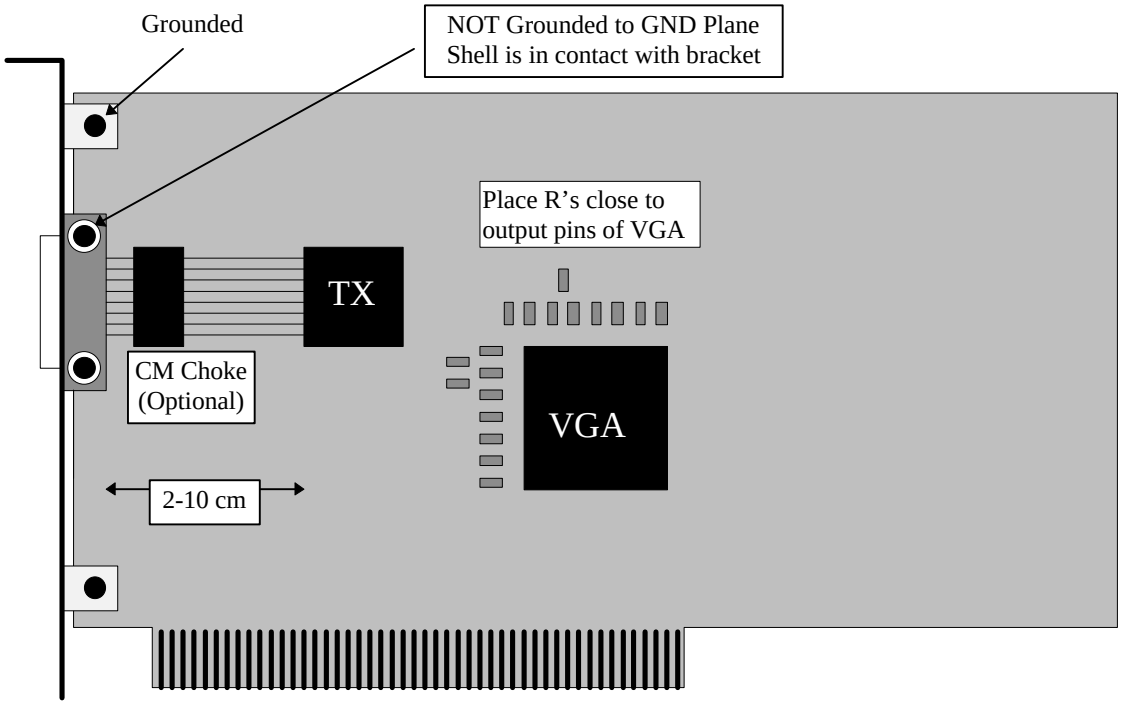


Figure 17: Typical Add-in card layout

3. GENERAL ELECTRICAL CONSIDERATIONS

Before addressing application issues specific to PanelLink™, there are some general electrical design considerations that need to be taken into account. These design considerations apply to the application of other controller or driver chips as well as the proper implementation of ground planes and filtering.

3.1. Capacitive Decoupling

All active components such as VGA controllers and driver chips require input power to operate. It is not enough to merely connect these power pins to the closest VCC plane since this can result in radiated emissions due to inadequate charge supply and inductance over power supply traces and vias. All high speed active components should have capacitive decoupling on their supply lines, preferably very close to each power and GND pin:

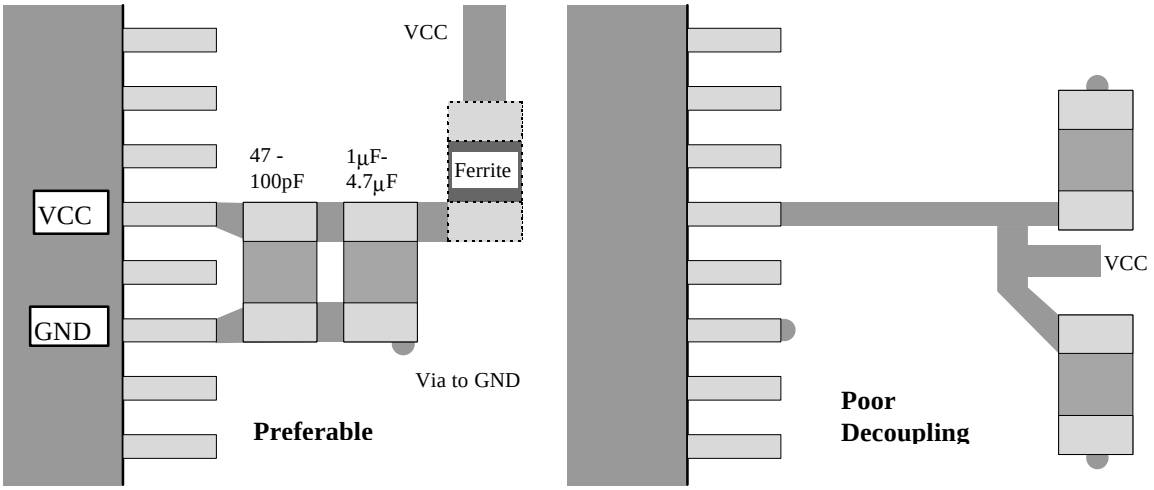


Figure 18: Capacitive decoupling

The ferrite is shown with a dotted line because it is used in special situations where a chip has two or more separate power planes (for noise or performance reasons). If one of the power planes generates a significant amount of noise, a ferrite and properly implemented decoupling capacitors can contain the noise within that local power plane and not allow it to propagate throughout the entire system's power plane, or prevent outside noise from corrupting a sensitive power input.

Note that the capacitors are connected directly to the pins to minimize the lead inductance of the decoupling loop between the power and ground pins. It seems unimportant until you realize the internal structure of an integrated circuit. See Figure 19. The internal bond wires used to connect the silicon contact pads to the pins usually have a characteristic inductance of 4nH which cannot be avoided. Thus any inductance you have on the exterior of the chip adds to this impedance. BGA packages may appear to be better in this respect, but are often the same or worse due to the routing required on the small PCB to the contact balls.

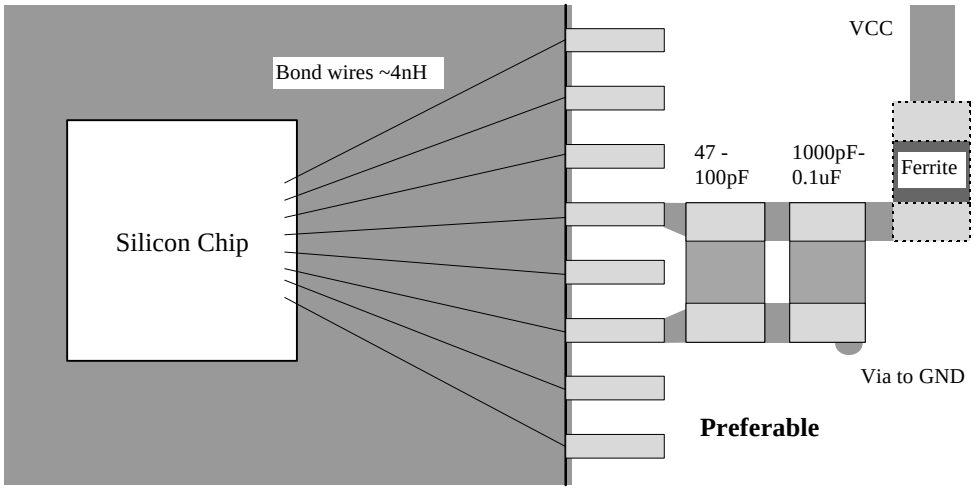


Figure 19: Internal bond wires in integrated circuits

The ground plane is contacted by the vias on the capacitor ground pads. This is for potential reference and current return but is not in the direct decoupling path of VCC and GND. This is because each via has between 1 and 2 nH's of inductance and this circuit avoids their series impedances. These inductances, in series with the inductance of the lead pins and the bonding wires within the IC itself, would seriously degrade the effectiveness of the decoupling capacitors.

Also indicated on the drawing on the left of Figure 18 are the approximate value ranges of the capacitors used in decoupling the power and ground pins. The capacitor on the left is smaller than the one on the right. This is because the smaller value capacitors' will resonate at higher frequencies and can therefore supply higher frequency currents. The "slower" large capacitor on the right is used to store additional charge and hold up the voltage on the power input. The smaller capacitor should be placed closest to the VCC/GND pins. In addition, 10 μF electrolytic capacitors should be placed at various points across the PCB's to provide low frequency energy storage. A rule of thumb is to provide 47 μF of capacitance for each Ampere of current the PCB uses.

A rule of "Decoupling At The Point Of Use" should be applied wherever possible to avoid high frequency currents flowing over long traces and/or power planes and creating potential noise radiation problems. During the PCB layout phase, care must be taken to allow space for decoupling on any VCC lines to any high speed integrated circuits.

3.2. Ground Planes

Proper use of ground planes within an electronic system is very important with respect to the amount of radiation that system produces. The ground plane serves as a direct return path for signals sent from one part of the system to another and should be as low an impedance as possible. Many times, designers operate under the notion that "a ground is a ground" and route their traces as such. Unfortunately, this is rarely the case in real world applications since a "ground" at one location on the PCB may have a potential difference (i.e. non-negligible impedance) relative to another point on the ground plane. This is due to the intrinsic ground plane inductance of 0.4 nH or more per inch along the plane. The inductive noise spikes caused by fast rise and fall time signal currents traveling down the board create potential differences along the plane and this "ground bounce" acts as a common mode current generator for cables leaving the board. In addition, the board itself resonates at its characteristic frequency as a consequence of

the spikes and also provides RF emissions. The designer's job is to minimize all these effects and reduce the emissions to only the level that results from normal board operation.

When routing signals, the designer should be careful to not route signal lines over breaks in the ground plane:

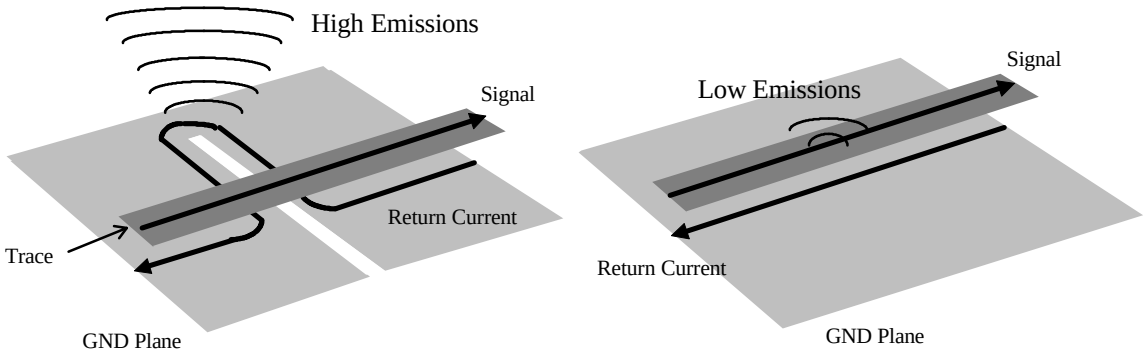


Figure 20: Effect of ground plane breaks

Breaking the ground plane must be avoided since it will be very easy to create the situation shown on the left. It is better to have a single ground plane and insure a direct return path for all signal currents. Another situation was described earlier in Section 2.4 where a divided ground plane forced a return current to travel through the chassis ground (Figure 7). This is also not recommended because 1) the signal return through the chassis will not be closely coupled to the outbound signal current, and 2) this introduces signal-related currents on the chassis possibly corrupting the chassis with noise. Close coupling with the original signal is important since it creates a lower inductance path for the return current (due to magnetic coupling), and the opposing fields tend to cancel thus reducing emissions.

In general, ferrites should not be placed between ground planes or on ground pins. This is because this places an RF potential between a returning signal current (and its reference plane) and the main Reference plane. The two planes form an antenna and radiate at the noise frequencies generated across the ferrite.

As mentioned in an earlier section, one must be careful to not terminate cable shields to the ground plane but instead terminate them to the chassis. There can be significant "ground bounce" due to current transitions of circuits using the ground plane. If this ground plane is then connected to a cable shield the noise will generate common mode current that will in turn cause the cable to radiate. The designer should remember that:

⇒ The braid surrounding the signal line of a coaxial cable is not a shield. It is primarily the return line for the signal. It should be terminated to the ground plane.

⇒ The external shield over the coaxial and/or twisted pair signal lines should be terminated to the chassis ground at both ends. If there is no external shield over the signal lines, it is highly recommended that common mode chokes or filters be applied to those signal lines and their return lines and a ferrite be placed on the cable at the source (typically the system) end and possibly the display end.

3.2.1. PCB Layout, Ground Planes and ESD

During an ESD event, a large positive or negative voltage pulse is imparted on the electronic system. Since most semiconductor devices are fairly sensitive to such discharges, it is up to the system designer to make sure that such devices are properly protected.

The most effective way to combat ESD events is to bypass potential entry points and design the system so that the pulse is dispersed as quickly as possible. One major source of ESD problems comes from improper layout of the PCB and ground planes. With high power analog systems such as CRTs, it is possible to use two layer PCBs and relatively slow bypass mechanisms such as spark gaps to protect these systems. However, with the static-sensitive integrated circuits used today, it is necessary to take additional measures.

First of all, unless all signal routing can be done on the top layer, it is recommended that a 4 layer PCB be used. This is so that there can be at least one *solid* ground plane. Using a two layer PCB with dual-sided signal routing usually results in narrow ground traces and smaller ground islands linked together by vias. Not only is this a problem for EMI, but the high impedance between the different sections of the "ground" prevents any fast transient voltage spikes from dissipating evenly throughout the system. The result is a localized high voltage area that tends to destroy integrated circuits. For example:

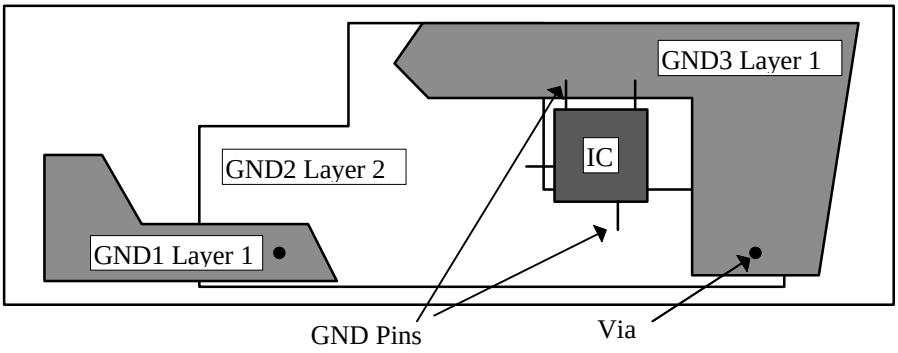


Figure 21: Ground Planes Joined by Vias

The example shown in Figure 21 is typical of a two-layer PCB ground design. At DC, the separate ground planes appear to be the same potential so not much attention is paid to the layout. However, at higher frequencies, the following is an equivalent circuit:

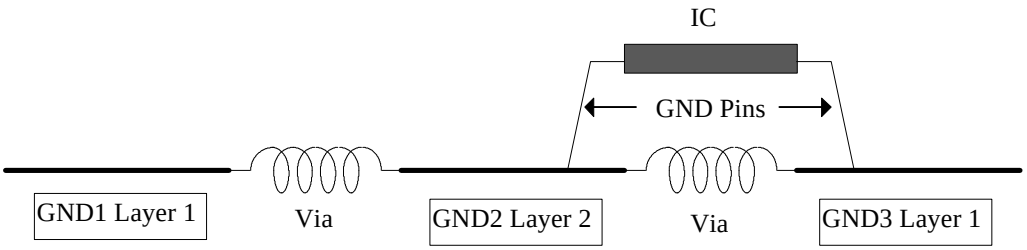


Figure 22: Equivalent Circuit of Figure 19

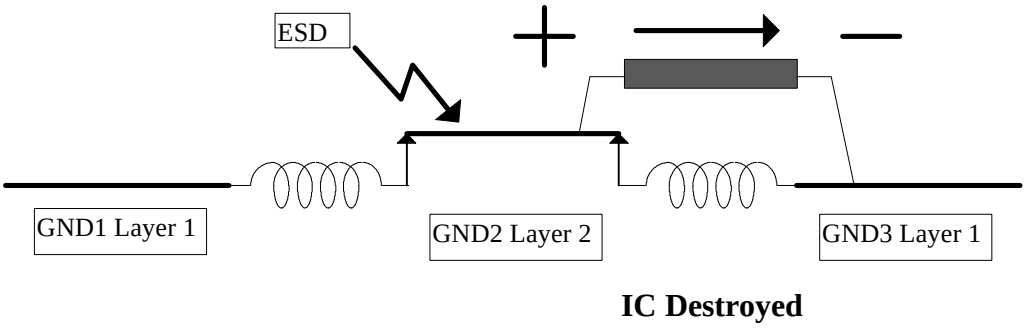


Figure 23: Potential Shift after ESD

Since the inductance of the vias prevents the discharge from dispersing evenly throughout the ground system, the local ground which has direct contact with the discharge rises very rapidly in potential with respect to the other “ground planes”. This in turn causes a large potential difference within the integrated circuit. The large internal currents caused by this potential difference destroys the integrated circuit.

Thus, with a solid ground plane, the voltage spike is dispersed quickly and evenly improving ESD survivability of the system.

Capacitive and diode bypassing is also important for ESD protection. A power plane may be subject to a static discharge as well as a ground plane. This is why there should be capacitive bypassing provided between the power planes and the ground plane since the capacitors will bypass the pulse to the ground plane and disperse the pulse (assuming that you have not split the ground plane as in Figure 21).

Signal lines that are accessible to the external environment are subject to static discharges and may also need to be protected. Typically, this is done with fast, low-capacitance diodes that are placed on the signal lines. Usually, each signal line has one diode to VCC and one to GND. Make sure that these diodes are placed near the signal lines and wide traces are used. If there is too much inductance in the traces or vias to the diodes, their effectiveness is greatly reduced. Refer to Section 4.6 for PanelLink implementation.

3.3. Power Planes and Power Lines

Obviously, no active circuit can operate without power and proper distribution is important to the performance of the system as well as the radiation it produces. In general, it is better and easier to have a large overall power plane (usually digital VCC) that supplies power to all the active components. If a special segregated power supply plane is required, it can be derived from this main power plane using decoupling capacitors and series ferrite as shown in Figure 18 in Section 3.1. If a large separate power plane is required, it also can be isolated from the main power plane with a ferrite, but the ground plane must remain common to both power planes. Since it is possible for a power plane to serve as a return path for AC signals, there should also be allowances made for small bypass capacitors between each power plane and the ground plane.

Insure that all power planes have adequate charge storage capacitors placed on them so that current drawn on one power plane does not require excessive current from any other planes coupled to it. Charge storage capacitors (for example, 47µF electrolytic capacitors) should be evenly distributed throughout each power plane so that charge storage is more uniformly distributed on that power plane. The purpose of these large

storage capacitors is to provide low frequency currents and hold up the voltage on the power plane from any lower frequency voltage fluctuations.

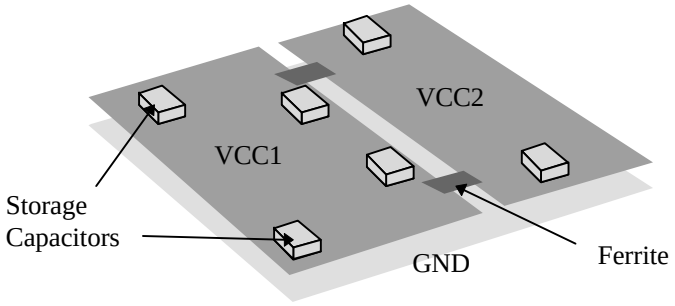


Figure 24: Illustration of Separate Power Planes and Charge Storage Capacitors

As mentioned in the previous section, allowances should be made for numerous smaller bypass capacitors between power and ground for ESD protection.

Sending power over a cable usually increases emissions, but is often necessary, especially in flat panel displays. Power planes (and their grounds) are often quite noisy due to all the circuits that are drawing current from them. In general they generate varying levels of common mode currents. Remembering that only a very small amount of common-mode current is necessary to fail most emissions standards (<15 μA at 30 MHz flowing through a 1 meter cable), the designer should be very careful to not let common mode voltages drive unshielded cables. To prevent common-mode noise on cables due to power distribution, filters need to be placed on the power lines as close as possible to the connector. See the next section, 3.4 Filtering.

3.4. Filtering

Filters selectively attenuate certain ranges of frequencies and are usually composed of inductors (or ferrites) and capacitors arranged in various configurations. Ideally, a filter will block unwanted frequencies while leaving desired signals unaffected. In reality, a filter will always affect all signals flowing though it, but if correctly chosen for the application, will reject only the required frequencies. There are both passive and active filters, but active filters cannot handle the frequencies that are of interest for EMI, and introduce noise and heat themselves due to the active components involved. Passive filters utilize only inductors, ferrites, capacitors and resistors and are used in numerous applications. This discussion will be restricted to passive filters.

Filters can be constructed from discrete components or can be purchased as self-contained surface mount packages. Two commonly used filter configurations are shown below:

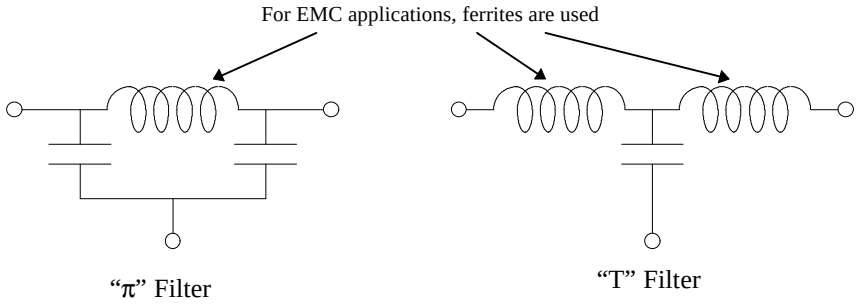


Figure 25: Common filter configurations

Both of these filters are low pass filters, i.e. they pass frequencies up to the cutoff point and attenuate frequencies beyond that. The "π" filter has a steeper cutoff characteristic and is better suited for use on signal lines although they can be used on power lines as well. Due to their simplicity, "T" filters are popular for use on low frequency lines or power lines. "T" filters have a long gradual cutoff and will probably affect any signals sent through that filter. Thus, "T" filters are generally used on power lines where good frequency response is not necessary. The cutoff curves for each type look similar to the following graphs:

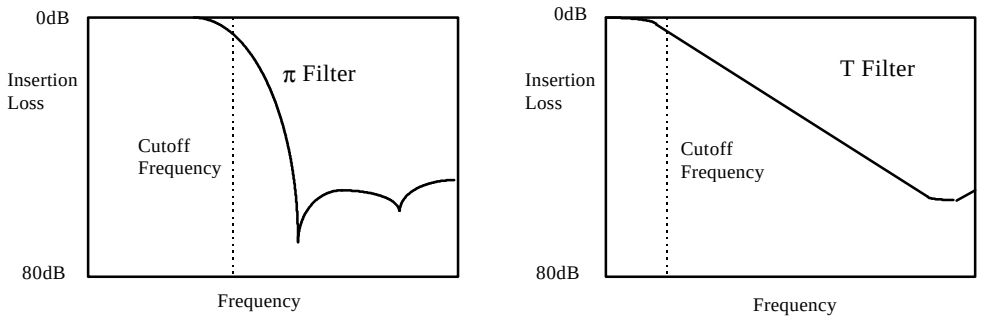


Figure 26: Filter attenuation curves

In general, ferrite beads are used in these noise filters as opposed to inductors. This is because a ferrite is a dissipative element and converts electromagnetic energy to heat, whereas inductors largely reflect this energy and may cause other problems. An other useful property of ferrites is their zero voltage drop for DC currents.

Filters are utilized as shown on the diagram below. The signal enters one of the top terminals and exits the other. The bottom terminal is connected to a reference, usually signal ground. The filter itself must be placed near the connector where the signal/power line exits the board to a cable.

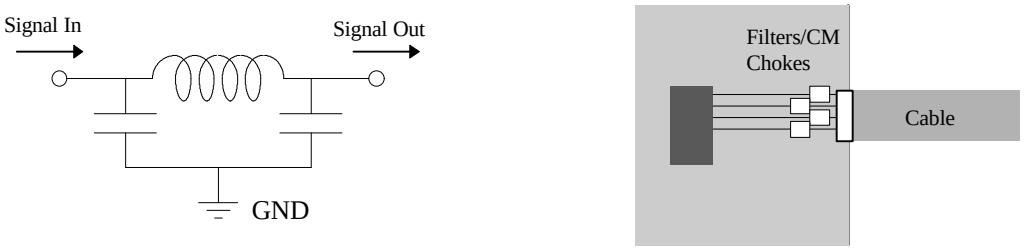


Figure 27: Physical placement of filters

As far as component values are concerned, typical available ferrite impedances lie in the range of 30 to 600Ω. Basically, the higher the impedance, the greater the attenuation at high frequencies. In general, changing the capacitance value moves the cutoff frequency for the filter. A reduction in capacitance moves the cutoff point to a higher frequency. An increase in capacitance moves the cutoff point to a lower frequency.

In the case of differential signals the signal is on two lines, each carrying an equal but opposite polarity current or voltage. In this case, the filters described above are difficult to implement and in addition may adversely affect signal flow. This is of no importance since seldom is differential noise generation on balanced pairs a problem. However, a major concern for these signal lines is common-mode noise. This is noise that is generated by currents of the same polarity flowing along both of the signal lines simultaneously. As has been pointed out elsewhere in this document, very low values of common mode current cause very high emissions so the matter must be given great attention. Further, these currents are usually not related to the signals on the lines affected but are generated elsewhere in the system as explained in the introduction to section 3.2. In either case, a method of common mode attenuation is needed. Fortunately, common-mode chokes exist that act as impediments to common mode currents. Even more fortunately, the filters do not affect differential signals. Their operation is explained below.

As an illustration, a common-mode choke is shown below that has two wires wound around a magnetic core such that the induced flux fields within the core caused by differential currents (i.e. the signal) subtract from each other and the flux adds to zero. In this case, since the signal does not create an inductive reactance, the signal passes through unchanged. However, the induced fields caused by currents flowing simultaneously in the same direction (i.e. common-mode noise) add to each other. Since inductance is defined to be proportional to flux generated by a current, a considerable amount of inductance is created and its reactance impedes the signal. This creates the favorable situation where signals encounter a low impedance and pass through, while common-mode current encounter a high impedance and is reduced.

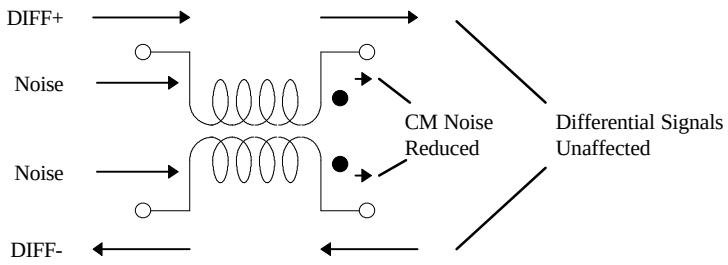


Figure 28: Effect of common-mode chokes

Common-mode (CM) chokes should be located similarly to the single-ended filters, i.e. near the connector where the signal(s) exit the board onto the cable. Also as with single-ended filters, common-mode chokes are available as self-contained surface mount packages.

During layout, space should be allotted near the connector for filters and/or common-mode chokes on all signal and power lines that enter or exit onto the cable, especially if the cable is unshielded. In general, common-mode chokes should be applied to signal lines (and their returns if single-ended), and filters applied to the power lines. The reason common-mode chokes are applied to single-ended signals is that if the topology shown in Figure 28 is used, the signal and its return current are in effect differential. A CM choke is also less likely to affect the signal adversely or introduce unpredictable phase effects.

3.5. Ferrites

Ferrites are sometimes thought of as some magical cure for EMI, frequently not well understood and sometimes misapplied. Ferrites can be small surface mount beads, or large toroids, A ferrite bead is similar to an inductor in that it presents a high impedance to high frequencies, but is different in that the impedance is mostly dissipative. Thus, ferrites dissipate a significant portion of the frequencies they impede as heat. An inductor stores the offending frequency in its magnetic flux field and releases it later to the adjacent circuitry, e.g., "ringing"(this characteristic is not useful for filters dealing with abruptly changing currents). Because of their dissipative nature, ferrites are much more suitable for high frequency filtering.

As such, ferrites may appear to "absorb EMI" but are actually high frequency resistors and serve as attenuators that reduce high frequencies in the circuits where they are placed. With this in mind, it should be reiterated that ferrites should NOT be placed on grounds or the ground pins of integrated circuits. If this is done, the ferrite beads will not "absorb" the noise on the ground plane, but will instead develop noise voltage across the ferrite proportional to its magnitude and the IC or ground plane will radiate. To mitigate against noisy grounds, remedies are:

⇒ Better capacitive decoupling on integrated circuits

⇒ More charge storage on the power plane(s)

There are typically two applications of ferrites, 1) ferrite chip beads, and 2) ferrite cores. Ferrite chips should generally be applied to power lines in conjunction with capacitors to form filters (See section 3.4). They can also be used with decoupling capacitors to isolate a power plane on an integrated circuit (See Figure 8). Ferrite cores are larger ferrites that are placed around the entire cable, i.e., sleeves. A ferrite core placed over a cable assembly in effect creates a large common-mode choke for the entire cable. Thus, any common-mode current that is present on all lines of a cable will be reduced because the ferrite presents a high common-mode impedance. The attenuation of the noise can be increased by increasing the impedance of the choke. This is accomplished by either increasing the impedance properties of the ferrite material, or winding the cable through the ferrite multiple times. The addition of more ferrite cores will also increase noise attenuation slightly. Unfortunately, the most important cable properties are its length and capacitance to nearby objects, i.e. the cable's behavior as an antenna.

If possible, a ferrite core should be placed at both the system end and at the panel display end of display cables. This way any common-mode currents generated by either the system or the display will see an impedance in the common-mode current and its consequential radiation will be reduced. Whenever a cable is utilized, common-mode currents will flow and can cause high RF emissions. If possible, space should be allowed for placement of ferrites on the display cable to reduce its ability to act as an antenna.

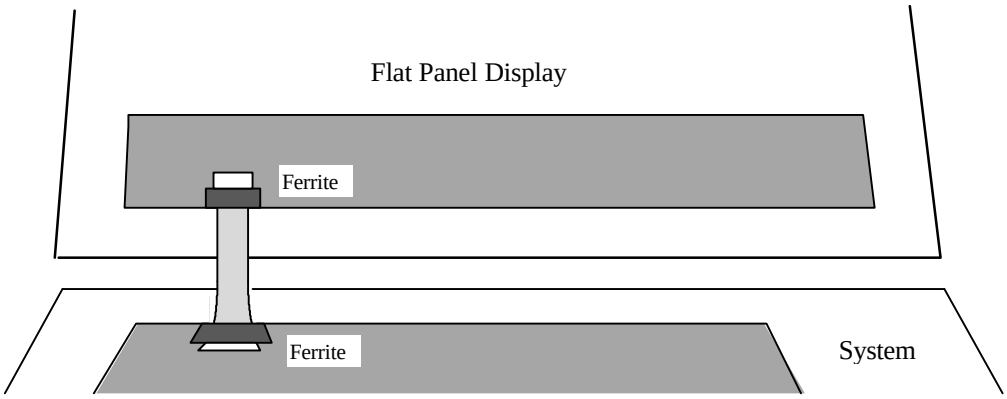


Figure 29: Ferrite core placement in a notebook PC

3.6. Summary

In summary, a designer should make sure they take the following electrical design points into consideration:

- ⇒ Insure that there is adequate capacitive decoupling on the power pins of all high speed integrated circuits.
- ⇒ Avoid dividing ground planes whenever possible and never route signal lines over breaks in the ground plane.
- ⇒ Do not place ferrites on grounds or ground pins.
- ⇒ Different power planes may be separated by ferrites, but make sure that adequate charge storage and capacitive bypassing is provided on each power plane.
- ⇒ Make space in the layout for common-mode chokes and filters at the cable connectors.
- ⇒ Leave room in the enclosure for placement of ferrite sleeves or clamp–ons on display and signal cables.

4. PanelLink™ APPLICATION CONSIDERATIONS

Now that general design considerations for flat panel displays/monitors have been discussed, there are some electrical and mechanical design considerations that are specific to the application of the PanelLink transmitter and receiver. Proper implementation of the PanelLink parts can prevent the conduction of radiating currents from the main system onto the PanelLink display cable and the system signal cable(s). Improper implementation of the PanelLink parts can cause increased levels of high frequency currents propagating through the system and negate any positive effects of the special PanelLink transition minimization encoding scheme.

4.1. Capacitive Decoupling

Like the VGA controller and other high speed integrated circuits, the PanelLink transmitter and receiver chips also need to have proper capacitive decoupling. The PanelLink chip pair has several separate power planes such as VCC, PVCC, and AVCC. The TX also has an IVCC which supplies current to the core logic, and the RX has OVCC which supplies power to the output data buffers. The AVCC/AGND pins provide power to the high speed differential lines and should have adequate decoupling to provide fast currents and minimize this current loop. Because of this, the following configuration is recommended on both the transmitter and receiver:

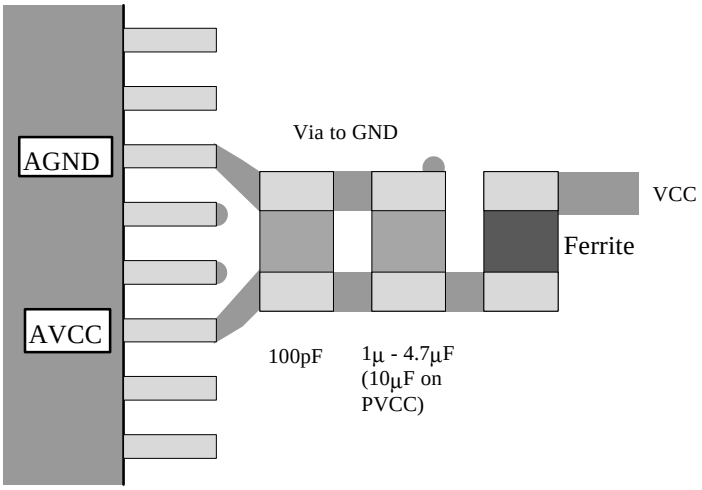


Figure 30: PanelLink decoupling scheme

Since the differential data lines are located between AVCC and AGND, what is typically done is to run the differential signals through a via to the second layer then to the connector. As noted in the Silicon Image "Basic PanelLink Design" applications note, running the differential lines through vias is acceptable due to PanelLink's skew tolerance. However, if vias are used, they should be used sparingly *and applied symmetrically within a +/- pair*.

SPECIAL NOTE: PVCC/PGND supplies power to the internal PLL and should also be decoupled as above to maximize performance and should have a voltage regulator to filter power line noise. Also, the outer decoupling capacitor for PVCC should be 10µF.

IVCC (on TX only) and VCC should have a 1000pF capacitor placed as close to each pin as possible.

OVCC on the RX draws a significant amount of current and it is important to have adequate charge storage on these pins. Place at least a 1000pF capacitor in parallel with a 1µF capacitor close to the OVCC pins to supply current to the data output buffers. Since data-related emissions comprise the majority of emissions from digital video systems, it would preferable to decouple OVCC as in Figure 30.

Make sure that there is a significant amount of decoupling and charge storage on the FPD controller boards. Insufficient charge storage will result in current being drawn from other sources (most likely over the cables) causing radiated noise. Usually, four to six 22-47µF capacitors distributed throughout the PWB are adequate to hold the voltage level.

4.2. Parallel Data Line Loading

Through the course of various EMI experiments and scans it has been determined by Silicon Image, Inc. that the parallel data lines feeding the TX and coming out of the RX create a significant amount of radiated emissions. This is largely due to the fact that both the VGA controller and the RX were designed to drive unknown loads and as such are capable of sourcing large amounts of abruptly changing currents. Although the VGA controller in a notebook typically feeds directly into the TX over a very short distance, the excessive digital current driving the system ground plane's inductance produces significant amounts of "board bounce" voltage near the display cable connector. This in turn causes common mode currents to be generated on the display cable and the cable and the display radiate with data-related RF emissions. Similarly, the RX typically feeds directly into the flat panel controller ASIC over a short distance and similarly radiates.

The best solution to this is to place series resistors on the parallel data lines as close to the source as possible. This reduces the currents charging the signal trace and IC capacitance. The reduction of charging currents is sufficient to reduce board bounce and lower emissions substantially. The most effective location of resistors is at the parallel output pins of the VGA controller and the RX chip:

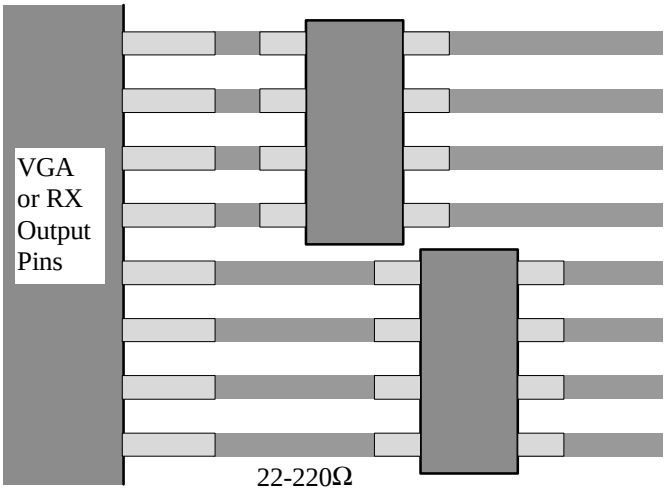


Figure 31: Resistor pack placement on parallel data lines

Even if space is limited on the motherboard, the PWBs should have spaces allocated for resistors on all parallel outputs of the VGA controller to the TX, including the clock line. Generally, flat panel controller PWBs are less space constrained, but should also allow the placement of these resistors. The effect of the

series resistors should not be underestimated. During experiments, Silicon Image confirmed that the current limiting resistors on the parallel data lines reduced emissions by 10-15dB.

The values of the resistors shown above vary from 22-220Ω and the actual value used will depend on the individual system. The important thing is to insure that the PWB layouts include the solder pads for these components on the VGA and RX outputs so they can be easily added/changed.

4.3. Power Distribution and Ground Planes

Main power to DVCC on the SiI100 (TX) and SiI101 (RX) is supplied by the main system 3.3V power supply plane. Power to AVCC and PVCC are derived from this main power supply through ferrites (to filter noise from the main supply) and decoupling capacitors which provide charge storage for current drawn on those pins. The IVCC and OVCC power source depends on the voltage level of the input and output signals respectively. If the data being fed to the SiI100 is from a 5.0V source, IVCC must be derived from the main 5.0V source on the system. If the input data is 3.3V, DVCC can be used. Likewise, if the FPD controller ASIC is 5.0V, OVCC must be 5.0V. If the FPD controller ASIC is 3.3V, DVCC can be used to supply OVCC.

Therefore, the suggested power distribution configuration for a 3.3V system is illustrated as follows:

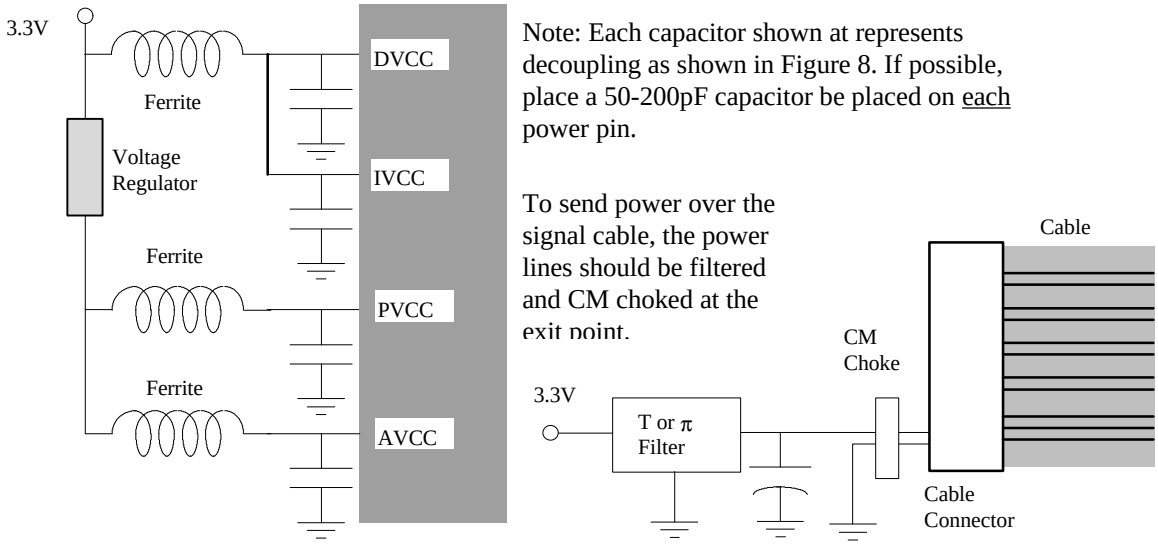


Figure 32: Supplying Power to the chips

Thus at the PWB level, PVCC and AVCC are not separate power planes themselves, but are derived from the main power. PVCC and AVCC may need to be regulated in noisy power environments such as motherboards with some bypass and charge storage capacitors. The ferrites block excessive high frequency noise from entering PVCC and AVCC, and also serve to contain any noise that may be generated by PVCC and AVCC so that it will not permeate throughout the main power plane. The main 3.3V power plane should be distributed throughout the motherboard and FPD (via the cables) and all other VCCs are derived from it on the both the transmitter and receiver side.

In most cases, power to the FPD hardware must be supplied from the main system by a cable. Before power is sent over the cable, it should be filtered so that any high frequency currents generated by the system are blocked from entering the cable and radiating. A final electrolytic capacitor is placed after the

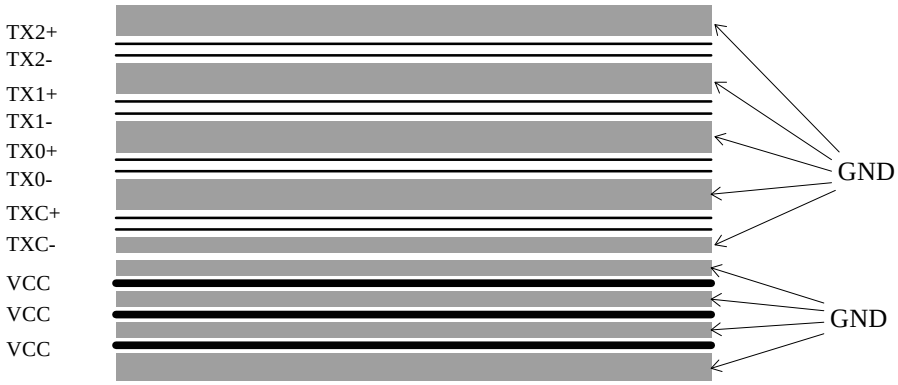
filter to hold up the DC voltage level followed by a common mode choke to keep the board bounce off of the display cable. On the receiving side, the power lines should be similarly filtered to prevent any noise generated by the FPD hardware from getting on the cable, and an electrolytic capacitor placed before the filter to hold up the voltage on the receiver side.

Although there are separate DGND, PGND, OGND and AGND pins on the transmitter and receiver chips, it is highly recommended that a large common ground be used on the PWB. This is because the high speed circuits in the transmitter/receiver can induce significant ringing in small separate ground planes and cause radiation. This is especially true if the separate grounds are sent over a cable since this will essentially create a dipole antenna with the two oscillating ground planes as a source. This applies not just to PanelLink, but to any high speed integrated circuit. The best and simplest solution is to have one large common ground plane on the PWB that is tied to a chassis ground at multiple contact points.

The signal cable typically carries the differential clock and data pairs as well as the power lines to the FPD logic. For suggested configurations for the signal cable, see the next section.

4.4. Signal Cable Configuration

Most notebook designers that use flat cables (FPCs) will generally prefer to use a 2-layer flex circuit as opposed to the 3-layer design shown in Figure 12 due to flexibility reasons. Therefore, in order to meet this requirement, a suggested 2-layer configuration for the signal cable is illustrated below:



Signal Layer (layer 1)

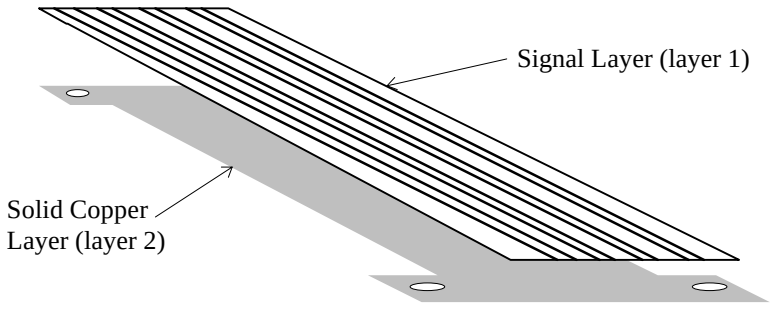


Figure 33: Two-layer FPC (flex cable)

The solid copper second layer serves as a partial shield for the cable (since it will most likely be looped over itself a few times in the hinge) and also serves as an RF contact between the flat panel chassis and the main system chassis. Terminate this second layer to the chassis on each side of the cable, not the ground plane on the PWBs.

Thus, with a 2-layer flex cable and ferrite clamps, the assembly should be connected as follows:

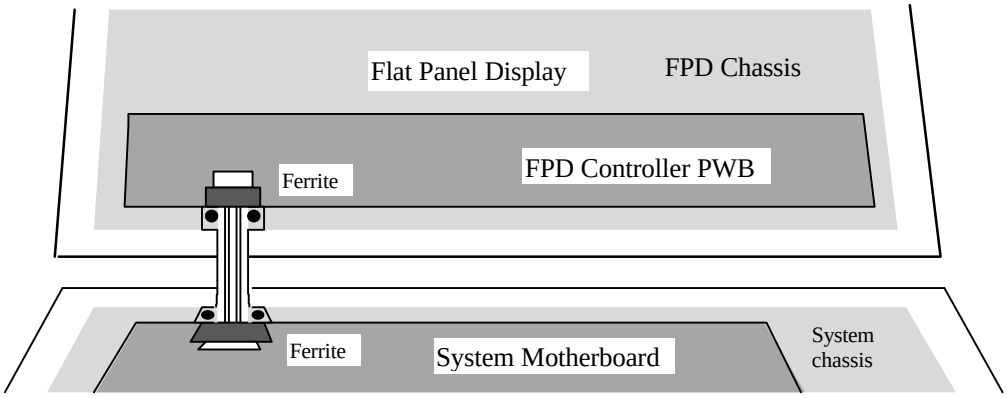


Figure 34: FPC termination and ferrite core placement

For twisted pair cables, it is recommended that individually shielded twisted pairs be used. If possible, an external overall shield is also recommended to contain any common-mode noise on the twisted pairs and to RF bond the display to the system. The twisted pair lines should be connected to each differential pair and the “shield” connected to AGND. The individual shield of each pair serves as a close-coupled return path for the signal currents. If there are any common-mode currents on both the shield and signal lines, the overall external shield will serve to contain those emissions. The shielded twisted pair cable should look something like this:

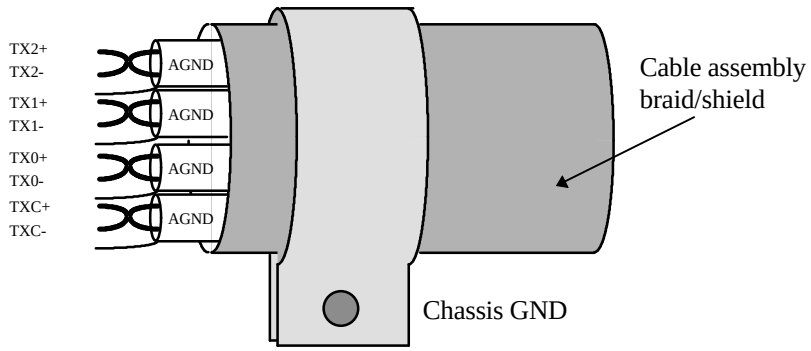


Figure 35: Twin-ax shield termination

If there are power lines being sent as well, the power lines should be paired with lines tied to their associated ground planes. Power should be sent over several pairs (3 or 4 pairs) to take advantage of parallel impedance in the lines.

If non-twin-ax twisted pair is used, *be sure to include several extra pairs of wires to serve as return lines for the signals*. Tie these extra lines to the ground plane on both the transmitter and receiver sides. These return lines are not the same as the chassis ground that the external overall shield is tied to. If these lines are not included, return currents are forced to return by the shield/chassis possibly corrupting the entire chassis with noise. The non-shielded configuration is not as ideal as the shielded twisted pair arrangement since the return lines will not be as closely coupled to the signal lines. In this case the use of ferrite sleeves at both ends of the cable may be crucial.

4.5. Filtering

When utilizing a common mode choke fix on unshielded or partially shielded signal cable, it is highly recommended that all signal and clock lines utilize the same choke core to avoid skew problems. The common mode choke should be installed near the point where the cable exits the system (as illustrated in Figure 13). It is more likely that the main system will produce higher levels of common mode and differential noise since there are many more active components operating on that PWB.

Power lines should be filtered at the exit point as shown in Figure 17 since the power plane can have a significant amount of noise, especially if the VGA controller or other high speed IC's are improperly decoupled. At a minimum, bypass capacitors and a common mode choke should be placed at the exit point of the power lines.

4.6. ESD Protection

Because the differential lines are exposed to the external environment, it may be necessary to apply special protection against ESD. The devices to use for this purpose are low-capacitance, fast diodes. Diodes with capacitance of 2-4pF are readily available and can be used for this purpose.

The diodes should be placed in shunt between each signal line and the power and ground plane as shown below:

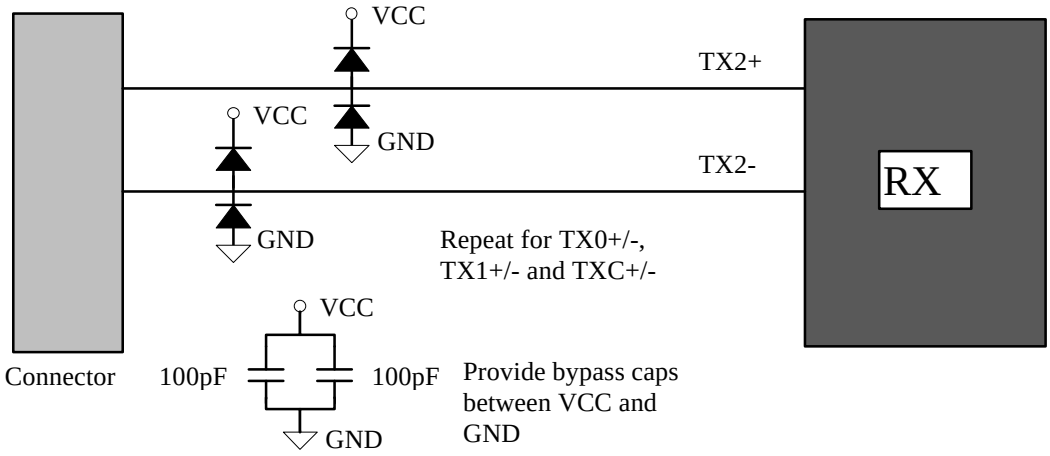


Figure 36: ESD Protection Diodes

These diodes should be placed as close to the signal lines as possible to minimize trace inductances. Protection diodes on the transmitter may also be needed IF there will be direct discharge tests done on the pins of the output connector. Typically, this is not necessary since tests on the host usually involve air discharges which the system chassis provides protection for.

4.7. Summary

In summary, it is important that certain application details of the PanelLink™ system not be overlooked. Although an electronic system may be completely functional, addressing EMC issues after the design is complete can lead to time consuming troubleshooting and retesting. Ensure that all high speed IC's have adequate decoupling on their power pins and that spaces for filters, CM chokes, and ferrites are allowed for. If they are found to be unnecessary, they can always be removed later as a cost cutting measure after production has begun, schedules have been met and controlled retesting and component evaluation can be performed.

When designing with the PanelLink™ system make sure that the following items are addressed adequately:

⇒ There is sufficient capacitive decoupling on all power pins on both the TX and RX.

⇒ There are current reduction resistors placed on the parallel lines at the outputs of the VGA controller and the RX. These should be placed as close to the output pins as possible.

⇒ PVCC and AVCC should be derived from the main 3.3V supply, but should be isolated by filters to contain any noise generated by those lines, and keep out noise from the main supply.

⇒ Differential and common mode filters should be placed on all power lines at their exit point nearest the display cable connector.

⇒ A shared common-mode choke (to reduce skew problems) should be placed at the signal exit points nearest the display cable connector.

⇒ Closely couple any signal or power line with its return line(s) on the cable, i.e. place them physically close to each other.

⇒ If only a two-layer FPC cable is feasible, place the close-coupled signals on the top layer and a second solid copper layer on the bottom. Tie the copper layer to the chassis on both sides and at both ends of the cable.

⇒ Leave room for a small ferrite core on any cable used in the system (not just the PanelLink™ signal cable).

⇒ Terminate braided shields with a 180° metal clamp with a wide contact area. DO NOT terminate braided shields in a twisted wire ("pig-tail") configuration.

⇒ Provide a good low impedance contact between the panel and main system chassis. The cable shield (braid or solid copper plane) can be used as this contact as long it is terminated properly. Hinges and conductive plastics are not suitable for this purpose.

5. EMI TROUBLESHOOTING TIPS AND CONCLUSIONS

Too often, when a product is found to be out of compliance with agency regulations, the first reaction is to begin applying fixes in the hopes that they will eliminate those emissions. Unless one is very experienced with the behavior of a particular system, this is usually the wrong thing to do and can lead to a lot of confusion.

EMC is not too much unlike other fields of engineering in that in order to apply an effective fix, the source of the problem must be first found. If an integrated circuit has a bug, designers do not begin blindly applying fixes in the hopes that one of them works. The source, or at least the characteristics of the bug are determined first before the fixes are found and applied.

With this in mind, one should determine (as best as is possible) the source and characteristics of the emissions before the fixes are applied. Since the motherboard is the origin of all signals, one should start at the far end of the signals and work back to the main system. This will allow you to better isolate the radiation point of the problem emissions. Remember that just because you know that an emission is from a certain subsystem it does not mean that it is radiating from there. The source may be deep within the main system, but actually radiating through the ground lines of a peripheral. Analyzing frequency harmonics tells you the *source*, disconnecting cables and powering down peripheral systems tells you where the *radiation point* is. Often the two are at very different locations.

In the case of PanelLink™, the power down pins are particularly useful. Perform an EMI scan between each of the steps below. The following steps are usually very helpful in determining the contribution of various sub-systems to the emissions levels of the entire assembly:

⇒ In the case of the 141 and 151, tie the PDO pin low. This shuts down the parallel data lines and shows the contribution of the video data. These signals will be present regardless of whether you use PanelLink, LVDS or straight parallel data since this is the ultimate format that the panel controller requires. PanelLink and LVDS drive these signals the exact same way.

⇒ Tie the PD pin of the RX low. In effect, this disables all active signaling on the FPD sub-system. A scan at this point will tell you the contribution of all the panel circuitry.

⇒ Power down the TX by tying its PD pin low. With the RX in PD, the TX is still actively signaling. A scan at this point will tell you the contribution of the TX chip

⇒ Disconnect the signal cable at the RX board. Scanning at this point will determine the level of emissions generated by the display cable, the FPD PWB and the FPD chassis.

⇒ Disconnect the signal cable at the TX. By comparing to the previous reading above, one can determine what emissions are generated by the cable and which are generated by the main system board.

⇒ Power down the VGA controller if possible.

PanelLink™ is an advanced, high-speed data transmission scheme but misapplication can lead to problems as with any complex system. It is important to follow good general electrical design guidelines and apply the recommendations explained in this document as much as possible. EMC is an overall system design issue more than it is a component-level issue, EMC design requires designers to consider more than just making sure point A is connected to point B or thinking “a ground is a ground”. Although tweaking certain components can improve emissions (or immunity), it is the initial system layout and

design that often determines how hard or easy it will be to bring a system into emission and immunity compliance.

It is important to realize the value of good trace routing and component placement. Although a digital multi-meter may register a short circuit between a ground pin and the main ground plane, at high frequencies, a long, thin trace is essentially an open circuit. Thus, at high frequencies the inductance of traces and other leads can not be ignored. For example, a via from the bottom layer to the top layer of a 1/8” thick PWB when compared to initial capacitor lead inductance increases the inductance between the capacitor and IC by more than 50%. Thus, if the traces between the capacitor and power pin are too long, the excessive series inductance will negate most positive high frequency benefits of the decoupling capacitor.

Also, when a signal is sent from one point to another, it is important to realize that the electrons do not just disappear—they must return to their source. Controlling the loop and its size is a critical part of good EMC design. The more this return path is impeded or convoluted, the higher the emissions will be as a consequence. If a signal is sent to the FPD without a direct, low impedance signal return, the resulting emissions will increase.

In conclusion, it should be reiterated that following all the guidelines explained herein will not guarantee that there will not be radiation issues with the overall system. However, the reader will at least avoid some basic design mistakes and be able to concentrate only on issues specific to their system.

SiI 169 HDCP PanelLink Receiver
Preliminary Datasheet

General Description

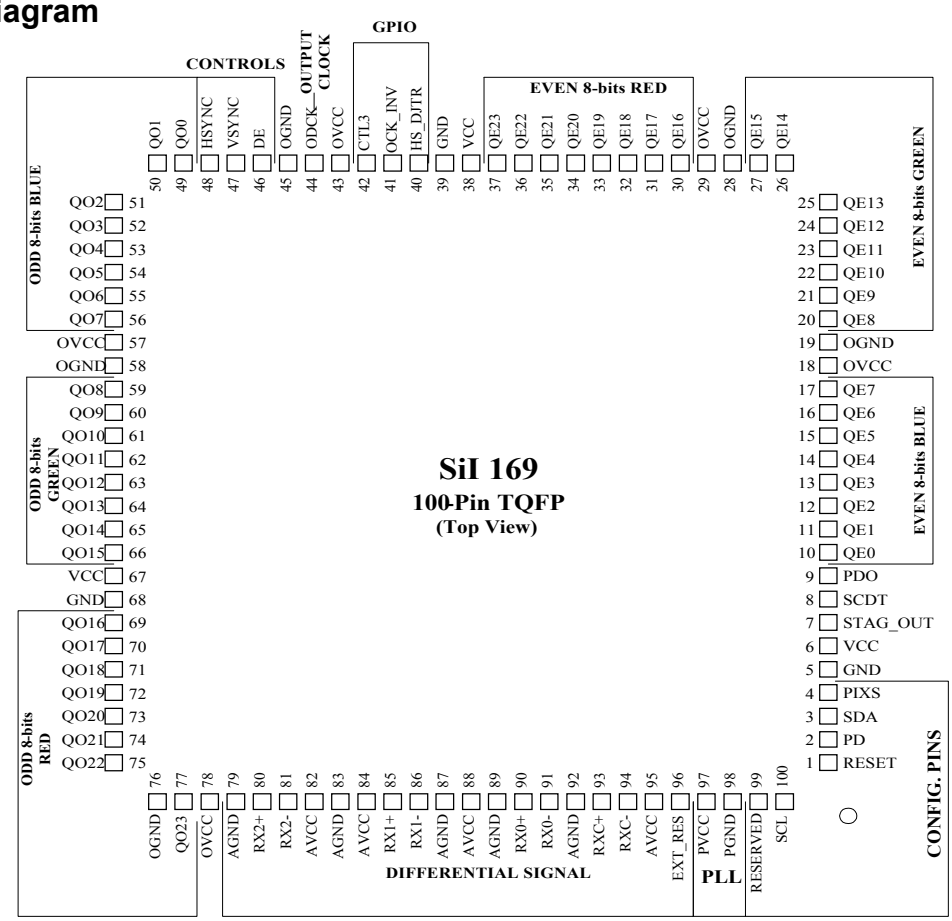
The SiI169 Receiver uses PanelLink Digital technology to support digital displays from VGA up to UXGA resolution (25-165 Mega-pixels/sec) with a PanelLink receiver core. It features High-bandwidth Digital Content Protection (HDCP) for secure delivery of high-definition video in consumer electronics. The SiI169 come pre-programmed with integrated HDCP keys, greatly simplifying manufacturing and providing the highest level of security. For improved ease of use, the SiI169 has an enhanced jitter tolerance and a low standby power mode.

PanelLink Digital technology is the world's leading DVI solution, providing a digital interface solution that is easy to implement and low cost. PanelLink further simplifies the display interface design by resolving many of the system level issues associated with high-speed mixed signal circuits.

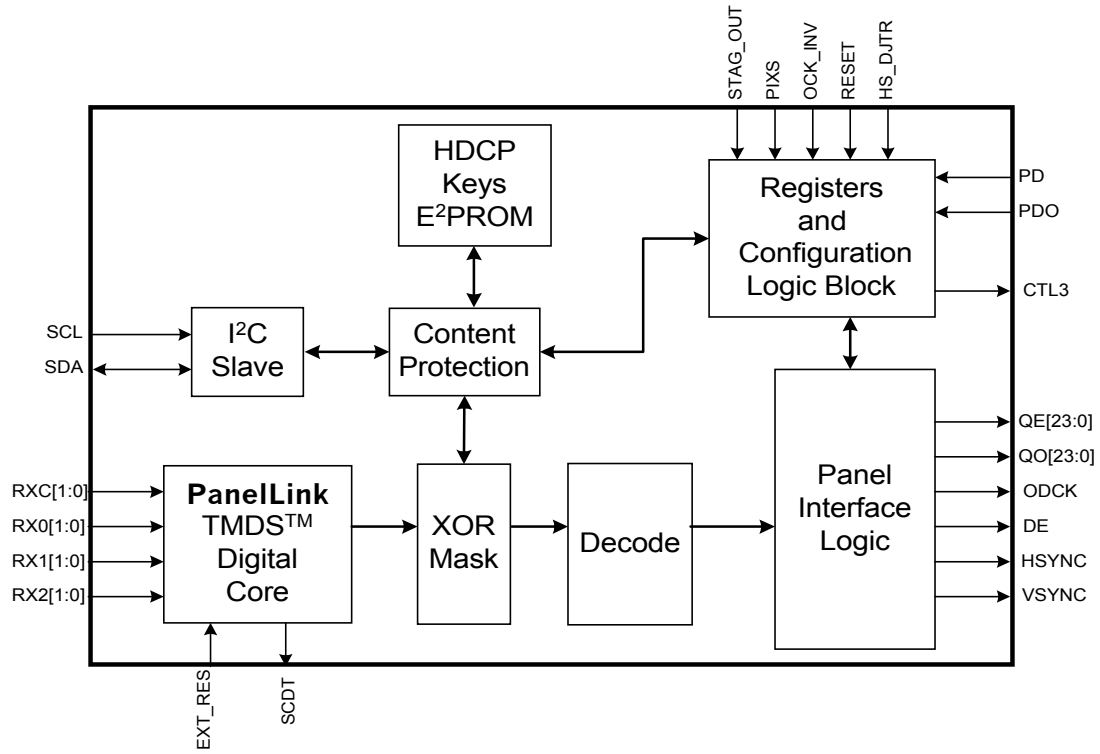
Features

- Supports VGA – UXGA resolutions
- 25MHz - 165MHz PanelLink core
- Integrated High-bandwidth Digital Content Protection (HDCP)
- Pre-programmed HDCP keys provide highest level of key security, simplifies manufacturing
- Enhanced jitter tolerance
- Time staggered data output for reduced ground bounce
- High Skew Tolerance: 1 full input clock cycle (6ns at 165MHz)
- Backwards compatible with SiI161B
- Sync Detect for "Hot Plugging"
- Flexible low power modes with automatic power down when input clock is inactive
- Low power 3.3V core operation
- Compliant with DVI 1.0 (DVI is backwards compatible with VESA® P&D™ and DFP)

SiI169 Pin Diagram



Functional Block Diagram



Absolute Maximum Conditions[1,2]

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage 3.3V	-0.3		4.0	V
V_I	Input Voltage	-0.3		V_{CC}+ 0.3	V
V_O	Output Voltage	-0.3		V_{CC}+ 0.3	V
T_A	Ambient Temperature (with power applied)	-25		105	°C
T_{STG}	Storage Temperature	-65		125	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)		TBD		°C/W

Notes: [1] Permanent device damage may occur if absolute maximum conditions are exceeded.
[2] Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{CCN}	Supply Voltage Noise			100	mV_{P-P}
T_A	Ambient Temperature (with power applied)	0		70	°C

DC Digital I/O Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage		2.0			V
V_{IL}	Low-level Input Voltage				0.8	V
V_{OH}	High-level Output Voltage		2.4			V
V_{OL}	Low-level Output Voltage				0.4	V
V_{CINL}	Input Clamp Voltage[1]	I_{CL} = -18mA			GND -0.8	V
V_{CIPL}	Input Clamp Voltage[1]	I_{CL} = 18mA			IVCC + 0.8	V
V_{CONL}	Output Clamp Voltage[1]	I_{CL} = -18mA			GND -0.8	V
V_{COPL}	Output Clamp Voltage[1]	I_{CL} = 18mA			OVCC + 0.8	V
I_{OL}	Output Leakage Current	High Impedance	-10		10	µA

Note: [1] Guaranteed by design. Voltage undershoot or overshoot can not exceed absolute maximum conditions for a pulse of greater than 3 ns or one third of the clock cycle.

DC Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{ODC}	Output Drive Data and Controls	V_{OUT} = 2.4V	TBD	TBD	TBD	mA
		V_{OUT} = 0.8V	TBD	TBD	TBD	mA
		V_{OUT} = 0.4V	TBD	TBD	TBD	mA
I_{OC}	ODCK Drive	V_{OUT} = 2.4V	TBD	TBD	TBD	mA
		V_{OUT} = 0.8V	TBD	TBD	TBD	mA
		V_{OUT} = 0.4V	TBD	TBD	TBD	mA
V_{ID}	Differential Input Voltage Single Ended Amplitude		75		1000	mV
I_{PD}	Power-down Current[2]	PD = LOW, RXC± Inactive			TBD	mA
I_{CLKI}	Power-down Current	PD = HIGH, RXC± Inactive			TBD	mA
I_{PDO}	Power-down Current, Outputs Disabled	ODCK=82.5MHz, 2-pixel/clock mode C_{LOAD}= 10pF R_{EXT_SWING} = 510Ω PDO = LOW Typical Pattern[3]			TBD	mA
I_{CCR}	Receiver Supply Current	ODCK=82.5MHz, 2-pixel/clock mode C_{LOAD}= 10pF R_{EXT_SWING} = 510Ω Typical Pattern, HDCP on[3]			TBD	mA
		ODCK=82.5MHz, 2-pixel/clock mode C_{LOAD} = 10pF R_{EXT_SWING} = 510Ω Worst Case Pattern, HDCP off[4]			TBD	mA

Notes: [1] Guaranteed by design.
[2] The transmitter must be in power-down mode, powered off, or disconnected for the current to be under this maximum.
[3] The Typical Pattern contains a gray scale area, checkerboard area, and text.
[4] Black and white checkerboard pattern, each checker is two pixel wide.

AC Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{DPS}	Intra-Pair (+ to -) Differential Input Skew[1]	165MHz			245	ps
T_{CCS}	Channel to Channel Differential Input Skew[1]	165MHz			4	ns
T_{IJIT}	Worst Case Differential Input Clock Jitter tolerance[2,3]	65 MHz			465	ps
		112 MHz			270	ps
		165 MHz			182	ps
D_{LHT}	Low-to-High Transition Time: Data and Controls (70 °C, 82.5 MHz, 2-pixel/clock, PIXS = 1)	C_L = 10pF			TBD	ns
	Low-to-High Transition Time: Data and Controls (70 °C, 165 MHz, 1-pixel/clock, PIXS = 0)	C_L = 10pF			TBD	ns
D_{HLT}	High-to-Low Transition Time: Data and Controls (70 °C, 82.5 MHz, 2-pixel/clock, PIXS = 1)	C_L = 10pF			TBD	ns
	High-to-Low Transition Time: Data and Controls (70 °C, 165 MHz, 1-pixel/clock, PIXS = 0)	C_L = 10pF			TBD	ns
T_{SETUP}	Data, DE, VSYNC, HSYNC, and CTL[3:1] Setup Time to ODCK falling edge (OCK_INV = 0) or to ODCK rising edge (OCK_INV = 1) at 165 MHz	C_L = 10pF	TBD			ns
		C_L = 10pF	TBD			ns
T_{HOLD}	Data, DE, VSYNC, HSYNC, and CTL[3:1] Hold Time from ODCK falling edge (OCK_INV = 0) or to ODCK rising edge (OCK_INV = 1) at 165 MHz	C_L = 10pF	TBD			ns
		C_L = 10pF	TBD			ns
R_{CIP}	ODCK Cycle Time[1] (1-pixel/clock)		6.06		40	ns
F_{CIP}	ODCK Frequency[1] (1-pixel/clock)		25		165	MHz
R_{CIP}	ODCK Cycle Time[1] (2-pixels/clock)		12.1		80	ns
F_{CIP}	ODCK Frequency[1] (2-pixels/clock)		12.5		82.5	MHz
R_{CIH}	ODCK High Time[4] (165MHz, 1-pixel/clock, PIXS = 0)	C_L = 10pF	TBD			ns
		C_L = 5pF	TBD			ns
R_{CIL}	ODCK Low Time[4] (165MHz, 1-pixel/clock, PIXS = 0)	C_L = 10pF	TBD			ns
		C_L = 5pF	TBD			ns
T_{HSC}	Link disabled (DE inactive) to SCDT low[1]			100		ms
	Link disabled (Tx power down) to SCDT low[5]				250	ms
T_{FSC}	Link enabled (DE active) to SCDT high[1]			25		DE edges
T_{CLKPD}	Delay from RXC± inactive to high impedance outputs[1]	RXC± = 25 MHz			TBD	µs
T_{CLKPU}	Delay from RXC± active to data active	RXC± = 25 MHz			TBD	µs
T_{PDL}	Delay from PD Low to high impedance outputs[1]				10	ns
T_{ST}	ODCK high to even data output[1]			0.25		R_{CIP}

Notes:
1. Guaranteed by design.
2. Jitter defined as per DVI 1.0 Specification, Section 4.6 *Jitter Specification*.
3. Jitter measured with Clock Recovery Unit as per DVI 1.0 Specification, Section 4.7 *Electrical Measurement Procedures*.
4. Output clock duty cycle is independent of the differential input clock duty cycle and the IDCK duty cycle.
5. Measured when transmitter was powered down (see SiI-AN-0005 “PanelLink Basic Design/Application Guide,” Section 2.4).

Setup and Hold Timings for Various Data Rates

The AC measurements listed above are minimum setup and hold timings based on the maximum data rate of 165 MHz. To estimate the setup and hold times for slower data rates (for either different resolutions or 2 pixel per clock mode), the following formulas can be used:

$$T_{SETUP}\,(\text{at new frequency}) = T_{SETUP}\ (165\text{MHz}) + \left(\frac{\text{Clock Period at new frequency} - \text{Clock Period at 165 MHz}}{2}\right)$$

$$T_{HOLD}\,(\text{at new frequency}) = T_{HOLD}\ (165\text{MHz}) + \left(\frac{\text{Clock Period at new frequency} - \text{Clock Period at 165 MHz}}{2}\right)$$

Table 1 shows the minimum set up and hold times for speeds other than 165 MHz (based on a 10 pF load and standard ODCK [OCK_INV = 0]).

Table 1. Set-up and Hold Times

Data Rate (MHz)	Clock (ns)	Setup (ns)	Hold (ns)	Resolution	Pixels/ Clock
165	6.06	TBD	TBD	UXGA	1
112	8.93	TBD	TBD	SXGA	1
86	11.6	TBD	TBD	XGA	1
82.5	12.1	TBD	TBD	UXGA	2
74.25	13.5	TBD	TBD	720p/1080i	1
56	17.9	TBD	TBD	SXGA	2
43	23.3	TBD	TBD	XGA	2
27	37.0	TBD	TBD	480p	1

Timing Diagrams

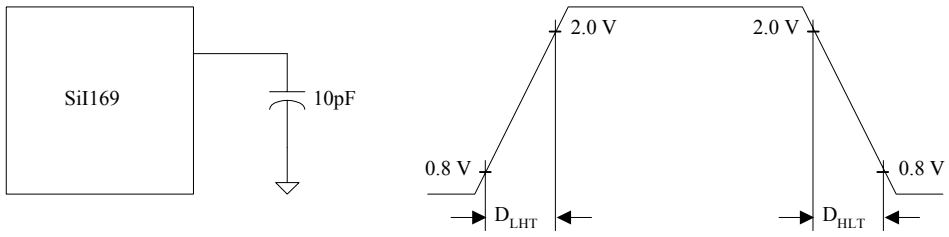


Figure 1. Digital Output Transition Times

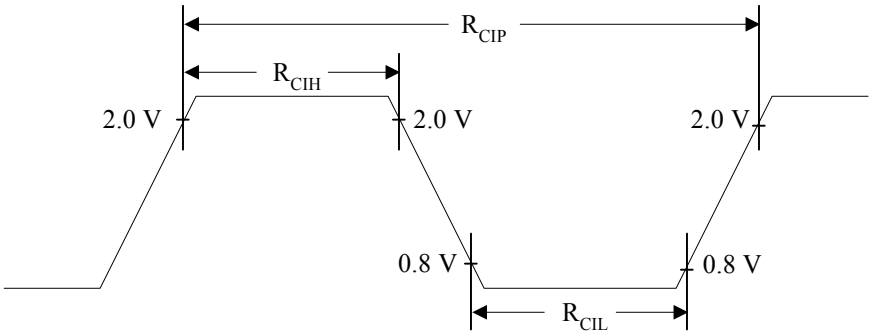


Figure 2. Receiver Clock Cycle/High/Low Times

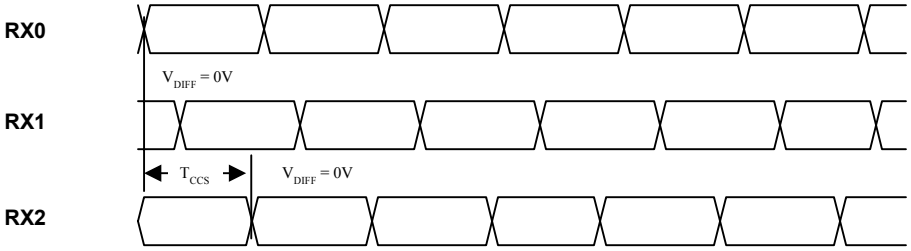


Figure 3. Channel-to-Channel Skew Timing

Output Timing

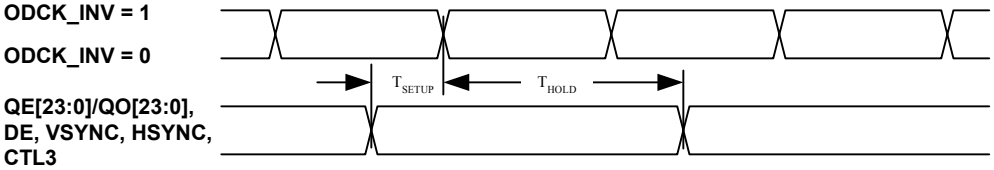


Figure 4. Output Data, DE, and Control Signal Setup/Hold Times to ODCK Falling Edge when ODCK_INV=0, or ODCK Rising Edge when ODCK_INV = 1.

Output Timing *(continued)*

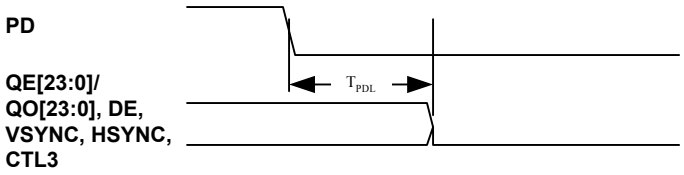


Figure 5. Output Signals Disabled Timing from PD Active

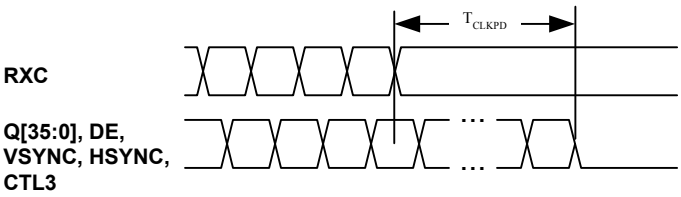


Figure 6. Output Signals Disabled Timing from PD Active

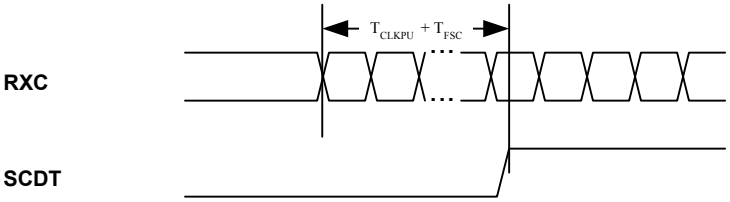


Figure 7. Wake-up on Clock Detect

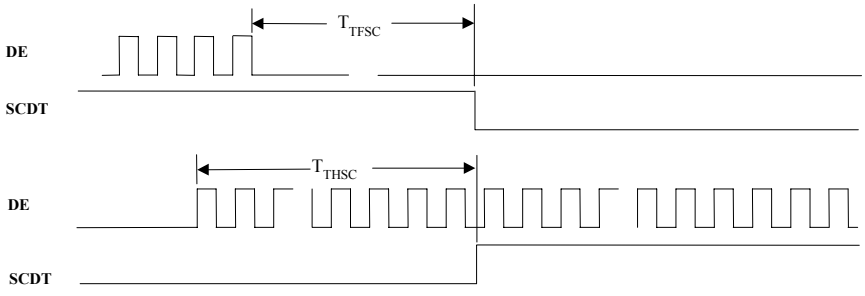


Figure 8. SCDT Timing from DE Inactive/Active

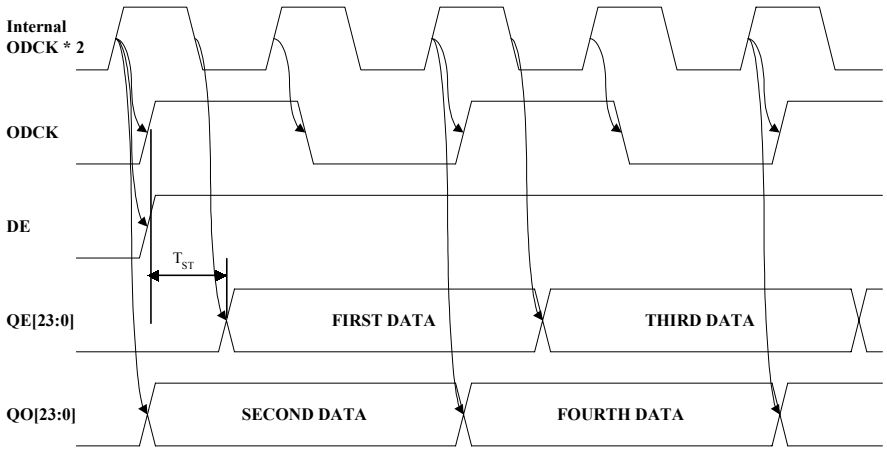


Figure 9. TFT 2-Pixels/Clock Staggered Output Timing Diagram

Output Pins Description

Pin Name	Pin #	Type	Description
QE23-QE0	See SiI 169 Pin Diagram	Out	Output Even Data. Output Even Data[23:0] corresponds to 24-bit pixel data for 1-pixel/clock input mode and to the first 24-bit pixel data for 2-pixels/clock mode. Output data is synchronized with output data clock (ODCK). Refer to the TFT Signal Mapping section later in the datasheet that tabulates the relationship between the input data to the transmitter and output data from the receiver. A low level on PD or PDO will put the output drivers into a high impedance (tri-state) mode.
QO23-QO0	See SiI 169 Pin Diagram	Out	Output Odd Data. Output Odd Data[23:0] corresponds to the second 24-bit pixel data for 2-pixels/clock mode. During 1-pixel/clock mode, these outputs are driven low. Output data is synchronized with output data clock (ODCK). Refer to the TFT Signal Mapping section later in the datasheet that tabulates the relationship between the input data to the transmitter and output data from the receiver. A low level on PD or PDO will put the output drivers into a high impedance (tri-state) mode.
ODCK	44	Out	Output Data Clock. This output can be inverted using the OCK_INV pin. A low level on PD or PDO will put the output driver into a high impedance (tri-state) mode.
DE	46	Out	Output Data Enable. This signal qualifies the active data area. A HIGH level signifies active display time and a LOW level signifies blanking time. This output signal is synchronized with the output data. A low level on PD or PDO will put the output driver into a high impedance (tri-state) mode.
HSYNC VSYNC	48 47	Out Out	Horizontal Sync control signal. Vertical Sync control signal.

Configuration/HDCP Pin Description

Pin Name	Pin #	Type	Description
PIXS	4	In	Pixel Select. A LOW level indicates one pixel (up to 24-bits) per clock mode using QE[23:0]. A HIGH level indicates two pixels (up to 48-bits) per clock mode using QE[23:0] for first pixel and QO[23:0] for second pixel.
STAG_OUT	7	In	Staggered Output. A HIGH level selects normal simultaneous outputs on all odd and even data lines. A LOW level selects staggered output drive. This function is only available in 2-pixels per clock mode.
RESET	1	In	Power-On Reset for cipher block. This pin should be connected to an external power-on reset chip. This pin should be tied HIGH for normal operation. This pin should be pulled low for a minimum of TBD ns for proper resetting of the cipher block.
HS_DJTR	40		HSYNC De-Jitter. This pin is used to enable or disable the HSYNC de-jitter circuitry. This circuitry defaults as disabled (tie pin 40 LOW) and may be enabled by tying this pin HIGH.
OCK_INV	41		Output Clock Invert.
CTL3	42	Out	General output control signal 3. This is CTL3, General Output Control Signal 3.
SCL	100	In	DDC I^2C Clock. This is the clock for the DDC (I^2C) bus.
SDA	3	In/Out	DDC I^2C Data. This is the data line for the DDC (I^2C) bus. HDCP KSV, $A_{n,}$ and R_i values are exchanged over this I^2C port during authentication.

Reserved Pin Description

Pin Name	Pin #	Type	Description
RESERVED	99	In	Must be tied HIGH for normal operation.

Power Management Pin Description

Pin Name	Pin #	Type	Description
SCDT	8	Out	Sync Detect. A HIGH level is outputted when DE is actively toggling indicating that the link is alive. A LOW level is outputted when DE is inactive, indicating the link is down. SCDT can be connected to PDO to power down the outputs when DE is not detected. The SCDT output remains in the active mode at all times.
PD	2	In	Power Down. A HIGH level indicates normal operation and a LOW level indicates power down mode. During power down mode, all output buffers are disabled and brought low, all analog logic is powered down, and all inputs are disabled.
PDO	9	In	Output Driver Power Down. A HIGH level indicates normal operation. A LOW level puts all the output drivers (except SCDT) into a high impedance (tri-state) mode. PDO is a sub-set of PD.

Differential Signal Data Pin Description

Pin Name	Pin #	Type	Description
RX0+	90	Analog	TMDS Low Voltage Differential Signal input data pairs.
RX0-	91	Analog	
RX1+	85	Analog	
RX1-	86	Analog	
RX2+	80	Analog	
RX2-	81	Analog	
RXC+	93	Analog	TMDS Low Voltage Differential Signal input data pairs.
RXC-	94	Analog	
EXT_RES	96	Analog	Impedance Matching Control. Resistor value should be approximately ten times the characteristic impedance of the cable. In the common case of 50Ω transmission line, an external 390Ω resistor must be connected between AVCC and this pin.

Power and Ground Pin Description

Pin Name	Pin #	Type	Description
VCC	6,38,67	Power	Digital Core VCC, must be set to 3.3V.
GND	5,39,68	Ground	Digital Core GND.
OVCC	18,29,43,57,78	Power	Output VCC, must be set to 3.3V.
OGND	19,28,45,58,76	Ground	Output GND.
AVCC	82,84,88,95	Power	Analog VCC must be set to 3.3V.
AGND	79,83,87,89,92	Ground	Analog GND.
PVCC	97	Power	PLL Analog VCC must be set to 3.3V.
PGND	98	Ground	PLL Analog GND.

TFT Panel Data Mapping

The following table shows the output data mapping in one pixel per clock mode for the SiI 169. This output data mapping is dependent upon the SiI PanelLink transmitters having the exact same type of input data mappings. Please refer to the SiI PanelLink transmitter for the specific input data mappings and to the TFT Signal Mapping application note (SiI-AN-0007).

SiI 169 1-Pixel/Clock Output		
Data	**18bpp**	**24bpp**
BLUE[7:0]	QE[7:2]	QE[7:0]
GREEN[7:0]	QE[15:10]	QE[15:8]
RED[7:0]	QE[23:18]	QE[23:16]

Table 2. One Pixel/Clock Mode Data Mapping

SiI 169 2-Pixel/Clock Output		
Data	**18bpp**	**24bpp**
BLUE[7:0] - 0	QE[7:2]	QE[7:0]
GREEN[7:0] – 0	QE[15:10]	QE[15:8]
RED[7:0] – 0	QE[23:18]	QE[23:16]
BLUE[7:0] – 1	QO[7:2]	QO[7:0]
GREEN[7:0] – 1	QO[15:10]	QO[15:8]
RED[7:0] – 1	QO[23:18]	QO[23:16]

Table 3. Two Pixel/Clock Mode Data Mapping

Note: For 18-bit mode, the Flat Panel Timing Controller interfaces to the SiI169 exactly the same as in the 24-bit mode; however, only 6-bits per channel (color) are interfaced instead of the full 8. As can be seen from the above table, the data mapping for less than 24-bit per pixel interfaces are MSB justified.

Power Management

The SiI 169 includes a number of flexible power management features. There are three power-down modes; Output Power-down, Clock Inactive and Power-down. Pulling the PDO pin LOW disables all the outputs excluding SCDT. If the input Clock signal goes inactive, the SiI 169 will automatically go into power-down with all the internal circuitry powered off except the input clock detect circuitry. Complete power-down is achieved by pulling the PD pin LOW. In this mode, the device goes into full power down reducing total power consumption to less than TBD.

Table 4. Power Management Functionality Table

Mode	Pin Status				Active Circuitry			Typical Power
	RXC±	PD	PDO	SCDT	TMDS Core	Output	HDCP Logic	
Full Power	Active	HIGH	HIGH	Active	ON	ON	ON	I_{CCR}
Output Power-down	Active	HIGH	LOW	Active	ON	OFF[2]	ON	I_{PDO}
Clock Inactive[1]	Inactive	HIGH	N/A	Active	ON	OFF	OFF	I_{CLKI}
Power-down	Inactive	LOW	N/A	Inactive	OFF	OFF	OFF	I_{PD}

N/A = Not applicable.

Notes: [1] Auto Power Down mode continuously monitors the link activity and is activated automatically when the link is inactive. This mode will automatically re-activate all outputs when the link becomes active again.

[2] Excluding SCDT.

I²C Registers

The SiI169 includes a DDC I²C serial interface that is used for HDCP Authentication. This port and the associated registers are described in the HDCP 1.0 Specification (February 2000) in ***Section 2.6 HDCP Port***. The I²C address for this port is 0x74. Read and Write operations to this port must complete in 100 ms per byte transferred.

I²C Register Mapping

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	BKSV_1 (RO)							
0x01	BKSV_2 (RO)							
0x02	BKSV_3 (RO)							
0x03	BKSV_4 (RO)							
0x04	BKSV_5 (RO)							
0x05	RSVD[3] (RO)							
0x06	RSVD[3] (RO)							
0x07	RSVD[3] (RO)							
0x08	Ri'_1 (RO)							
0x09	Ri'_2 (RO)							
0x0A	RSVD[3] (RO)							
0x0B	RSVD[3] (RO)							
0x0C	RSVD[3] (RO)							
0x0D	RSVD[3] (RO)							
0x0E	RSVD[3] (RO)							
0x0F	RSVD[3] (RO)							
0x10	WR_AKSV_1 (WO)							
0x11	WR_AKSV_2 (WO)							
0x12	WR_AKSV_3 (WO)							
0x13	WR_AKSV_4 (WO)							
0x14	WR_AKSV_5 (WO)							
0x15	RSVD[3] (RO)							
0x16	RSVD[3] (RO)							
0x17	RSVD[3] (RO)							
0x18	WR_AN_1 (WO)							
0x19	WR_AN_2 (WO)							
0x1A	WR_AN_3 (WO)							
0x1B	WR_AN_4 (WO)							
0x1C	WR_AN_5 (WO)							
0x1D	WR_AN_6 (WO)							
0x1E	WR_AN_7 (WO)							
0x1F	WR_AN_8 (WO)							

Notes: 1 All values are Bit 7 [MSB] and Bit 0 [LSB].
2 RW = Read/Write register, RO = Read Only register.
3 RSVD = Reserved read only register. All bytes read as 0x00.
4 All registers do not retain their values after a RESET.

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x20 to 0x3F	RSVD[3] (RO) (32 bytes in size)							
0x40	Bcaps (RO)							
	RSVD[3]	REPEATER	RSVD	FAST	RSVD[3]			
0x41 to 0xFA	RSVD[3] (RO) (175 bytes in size)							
0xFB	DEV_ID (RO)					DEV_REV (RO)		
0xFC	RSVD (RO)					PDO (RO)	RSVD	OCK_INV (RO)
0xFD	RSVR[4] (RO)							
0xFE	RSVR[4] (RO)							
0xFF	RSVS(RW)[5]							RESET[6,7] (RW)

Notes: 1 All values are Bit 7 [MSB] and Bit 0 [LSB].
2 RW = Read/Write register, RO = Read Only register, WO = Write Only register.
3 RSVD = Reserved read only register. All bytes read as 0x00.
4 RSVR = Silicon Image reserved read only register. Value is indeterminate.
5 RSVS = Silicon Image reserved read/write register.
6 The default value for **RESET** is LOW. Setting **RESET** to HIGH is the equivalent to asserting the chip's RESET pin (Pin 1) to LOW.
7 All register values are cleared after a RESET.

I²C Register Definition

Register Name	Access	Description
BKSV	RO	Video receiver's key selection vector (KSV). This value must always be available for reading, and may be used to determine that the video receiver is HDCP capable. Valid KSVs contain 20 ones and 20 zeros, a characteristic that must be verified by the video transmitter hardware before encryption is enabled.
Ri'	RO	Link verification response. Updated every 128th frame. It is recommended that graphics systems protect against errors in the I²C transmission by re-reading this value when unexpected values are received. This value must be available at all times between updates. R_0' is available a maximum of 100 ms after Aksv is received. Subsequent R_i' values are available a maximum of 128 pixel clocks following the assertion of CTL3.
WR_AKSV	WO	Video transmitter's key selection vector (KSV). Writes to this multi-byte value are written least significant byte first. Five bytes: 1 is the LSB, 5 is the MSB. All five should be read from the transmitter and then written here. The final write to 0x14 (byte 5) should be written last and will trigger the authentication process in the receiver.
WR_AN	WO	Session random number. A 64-bit pseudo-random value written from the transmitter during authentication process. Alternatively, this value may be generated by software or hardware, and then written here. Eight bytes: 1 is the LSB, 8 is the MSB. This multi-byte value must be written by the graphics system before the KSV is written.
Bcaps	RO	Bit 7: Reserved. Read as 0x00. Bit 6: REPEATER, Video repeater capability. This bit is set to 0 describing the device as a DVI end point. Bit 5: Reserved. Read as TBD. Bit 4: FAST, I²C transfers speed. This bit is 0 when 100 KHz is the maximum transfer rate supported and a 1 when 400 KHz is the maximum rate. The SiI169 will always show this register as a 1. Bits 3-0: Reserved. All bytes read as 0x00.
DEV_ID	RO	Device ID. (1Bh)
DEV_REV	RO	Revision Number. (1Bh)
PDO	RO	Output Power Down. This bit reflects the status of the PDO pin (pin 9). This bit will be set to 1 when the SiI169's outputs are disabled (excluding SCDT and CTL1) and 0 when the outputs are enabled.
OCK_INV	RO	ODCK Invert. This bit reflects the status of the OCK_INV. This bit reflects normal operation when set to 0, inverted ODCK if set to 1.
DBG	RW	Bits 7-1: RSVS, Silicon Image reserved register. This is available for future use by Silicon Image, Inc. Bit 0: RESET, Software reset. The default value for RESET is LOW. Setting RESET to HIGH is the equivalent to asserting the chip's RESET pin to LOW.
RSVD	RO	Read only reserved register. All bytes read as 0x00.

Notes: RW = Read/Write register, RO = Read Only register, WO = Write Only register

HDCP Operation

HDCP provides a secure method of delivering high-definition content between a host (Set-top Box, DVD, D-VHS) and display (HDTV, Projector, A/V Receiver). Security is maintained by means of an authentication process whereby the host verifies that a valid display is connected. This authentication process is repeated by the host every 128 frames (approximately 2 seconds) to verify that the display has not been replaced with a non-authenticated device. Each and every host and display have a unique set of HDCP 'keys' and Key Selection Vector (KSV) that are licensed from Digital Content Protection, LLC (www.digital-cp.com).

The authentication process involves exchanging calculated values based on the keys and KSV. A software driver running on the host controls the exchange of these values between the host transmitter (SiI170) and display's receiver (SiI907B, SiI169). The KSV and two other values, A_n and R_i, are exchanged over DVI's DDC channel (I^2C bus). Both the transmitter and receiver are slaves on this I^2C bus. Figure 10 shows a typical HDCP system configuration.

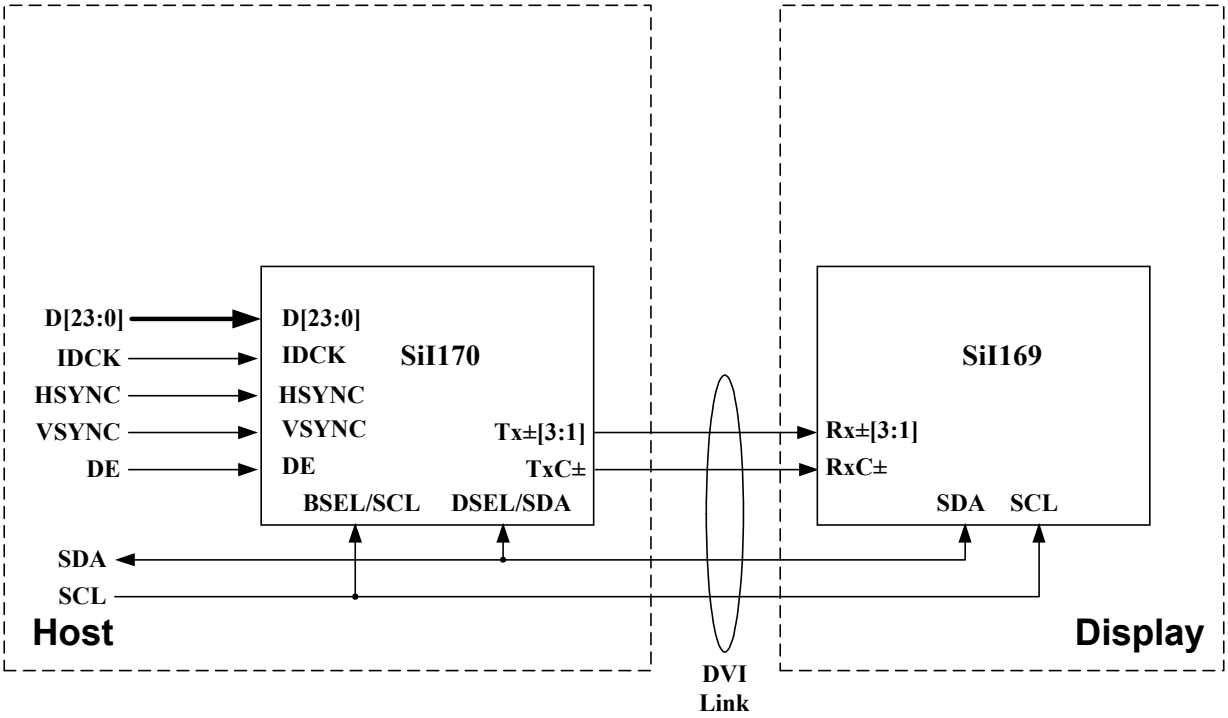


Figure 10. HDCP System Architecture

HDCP Authentication

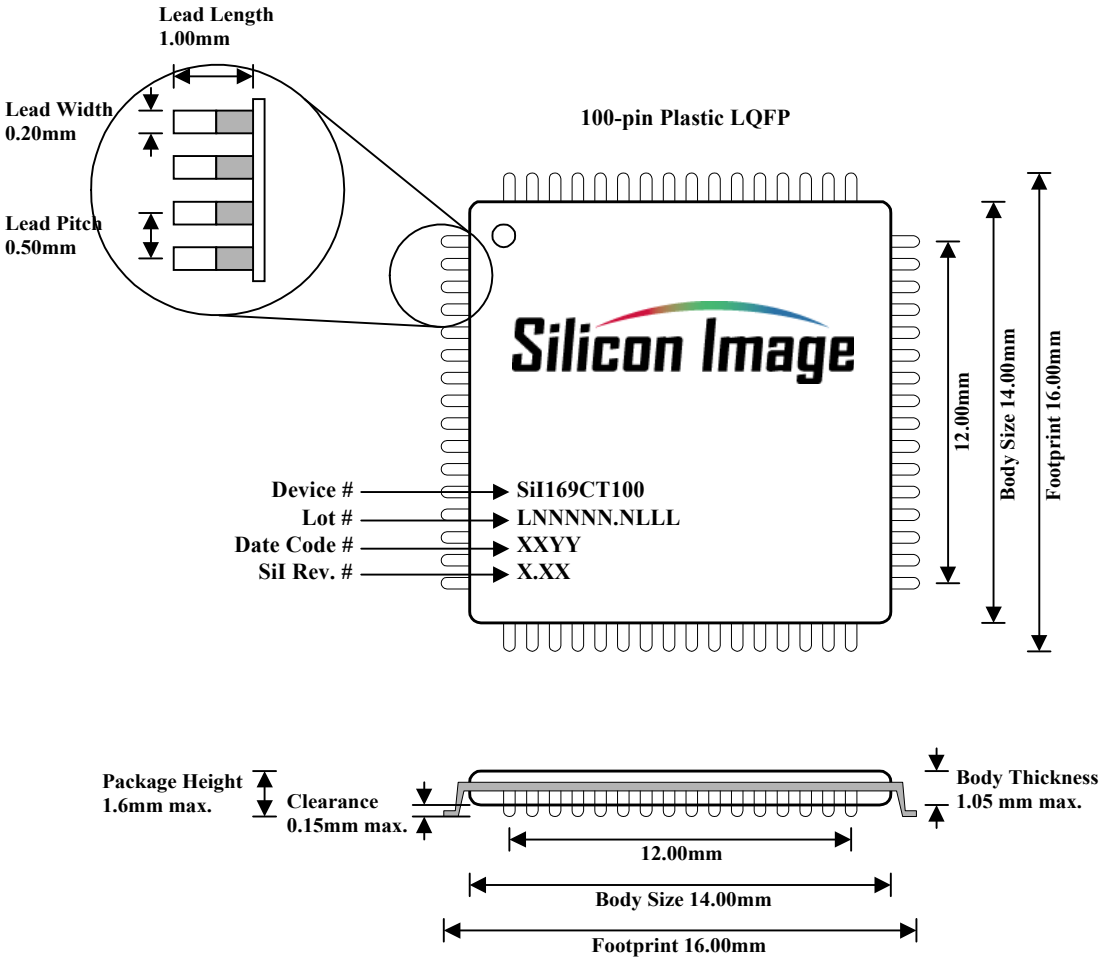
The SiI169 includes an integrated cipher engine that calculates all the required values based on an associated set of keys and KSV. The keys and KSV are stored in the SiI169 and consist of 40 keys of 56-bits each and a 40-bit KSV value that is unique to the set of keys. Each host and display will have their own set of keys.

The authentication process is initiated by clearing and then setting the TX_ANSTOP bit in the host transmitter (SiI170) to generate a pseudo-random value A_n. Both A_n and A_{KSV} are then written to the appropriate register in the receiver (WR_AN, WR_AKSV). The receiver register set address space is defined in the HDCP specification so any host driver will work with any HDCP compliant receiver. Writing these values to the receiver causes the receiver to initiate its own calculations that are used to decrypt the incoming video signal. The receiver's B_{KSV} value is read from and written to the WR_BKSV register of the transmitter. Using B_{KSV}, the transmitter will calculate a value R_0. The host side software driver should read the value R_0 from the transmitter and the corresponding value R_0' from the receiver and check for a match. If the values are equivalent, then both the transmitter and receiver are synchronized and

authentication has been successful. The encryption enable bit of the transmitter, ENC_EN, is then set and the transmitter begins encrypting. Reading R_i and R_i' is repeated every 128 frames to ensure that an authenticated link is maintained.

Package Dimensions

100-pin LQFP Package Dimensions



SiI169 Package Diagram

Order Part Number: SiI169CT100

Appendix A – Heatsinking for SiI169

PCB Thermal Design Options

The SiI 169 is packaged in a thermally enhanced 100 pin LQFP with an exposed metal pad (7.5mm x 7.5 mm) on the package designed for improved thermal dissipation. To improve the heat removal from the package, the exposed thermal pad may be soldered to a thermal landing area on the PCB, as described in the following section, entitled “Implementation Guidelines for Thermal Land Design”.

Implementation of the thermal landing area on the PCB can, in some cases, make trace routing and board design complicated. In some applications, it may be desirable to eliminate the thermal landing area on the PCB.

Generally the thermal performance of a package can be represented by the following parameter (JEDEC standard JESD 51-2, 51-6):

θ_{JA} , Thermal resistance from junction to ambient

$$\theta_{JA} = (T_J - T_A) / P_H$$

Where T_J is the junction temperature
T_A is the ambient temperature
P_H is the power dissipation

θ_{JA} represents the resistance to the heat flows from the chip to ambient air. It is an index of heat dissipation capability. Lower θ_{JA} means better thermal performance.

Implementation of the thermal landing area, combined with complete soldering of the package to the landing area results in a θ_{JA} of 21°C/W. If the SiI 169 package is assembled to a standard PCB, without the thermal landing area, the θ_{JA} increases to 29°C/W. For comparison, the non-thermally enhanced 100 pin LQFP package has a θ_{JA} of 53°C/W, so the advantage of the exposed metal pad in the thermally enhanced SiI 169 package is significant, even without a landing area on the PCB.

In order to determine the requirements for soldering the SiI169 to the PCB, the following analysis is insightful. Assuming a worst case scenario, with operation at the maximum ambient temperature of 70°C, at maximum voltage (3.6V) and worst case pattern (TBD) – the junction temperature would be 35°C above ambient, or 105°C. This is still well below the maximum junction temperature of 125°C, providing suitable margin even without requiring the use of solder and a specific landing area on the PCB. For comparison, with the improved thermal dissipation that results from complete soldering of the thermal pad on the chip to a thermal landing area on the PCB, the package temperature would be 23°C above ambient – or roughly 12°C cooler than a chip with no solder.

Based on this analysis, the need for designing a thermal landing area on a PCB for use with the SiI 169 receiver should be considered an optional design choice by the customer, and is not an absolute requirement.

For more information regarding Thermal Design Options, please see Application Note SiI-AN-0045, Enhanced Thermal Packaging Options for SiI 169.

Implementation Guidelines for Thermal Land Design:

As described above, a thermal land on the PCB may be incorporated on the PCB to improve the heat removal from the package. An example of this is shown in Figure 14, which depicts the exposed heat pad and Figure 15, which shows a LQFP Thermal Land Design on a PCB. The size of this thermal land can be smaller or larger than the exposed pad on the package. A clearance of at least 0.25 mm should be designed on the PCB between the outer edges of the thermal land and the inner edges of pad pattern for the leads to avoid any shorts.

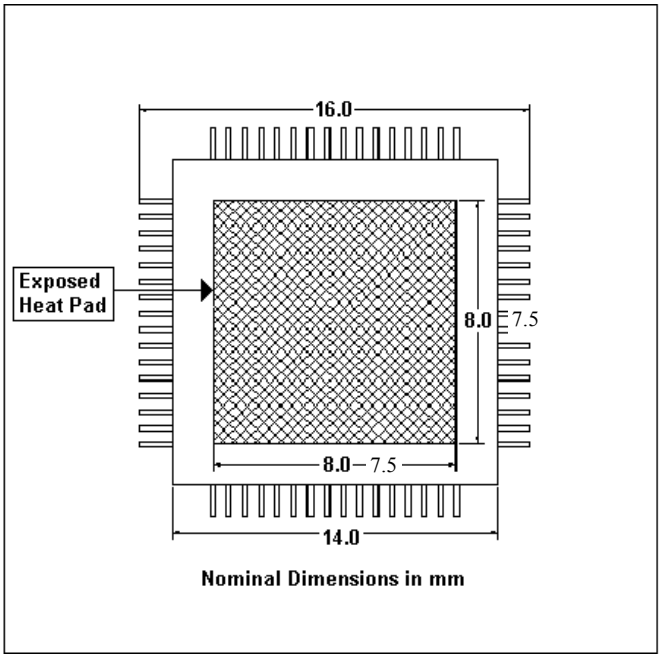


Figure 14. Bottom View of Thermally Enhanced 100-pin TQFP Package

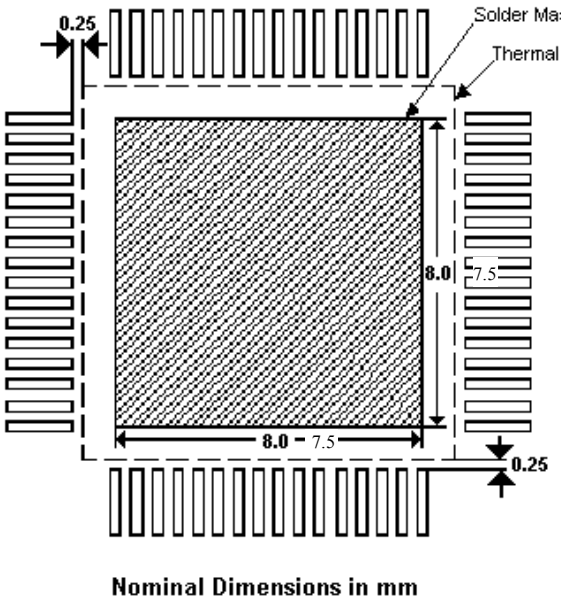


Figure 15. TQFP Thermal Land Design on PCB

When a thermal land on the PCB is used to provide a means of improved heat transfer from the package to the board through a solder joint, thermal vias are required to remove the heat from the PCB. It is recommended that these vias connect to the ground plane of the PCB. These vias provide a heat transfer path from the top surface of the PCB to the inner layers and the bottom surface of the package. An array of vias should be incorporated in the thermal pad at 1.2 mm pitch grid, as shown in Figure 16. Thermal

Pad Via Grid. It is also recommended that the via diameter should be around 12 to 13 mils (0.30 to 0.33 mm) and the via barrel should be plated with 1 oz copper to plug the via. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad and the thermal land. If the copper plating does not plug the vias, the thermal vias can be "tented" with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 4 mils (0.1 mm) larger than the via diameter.

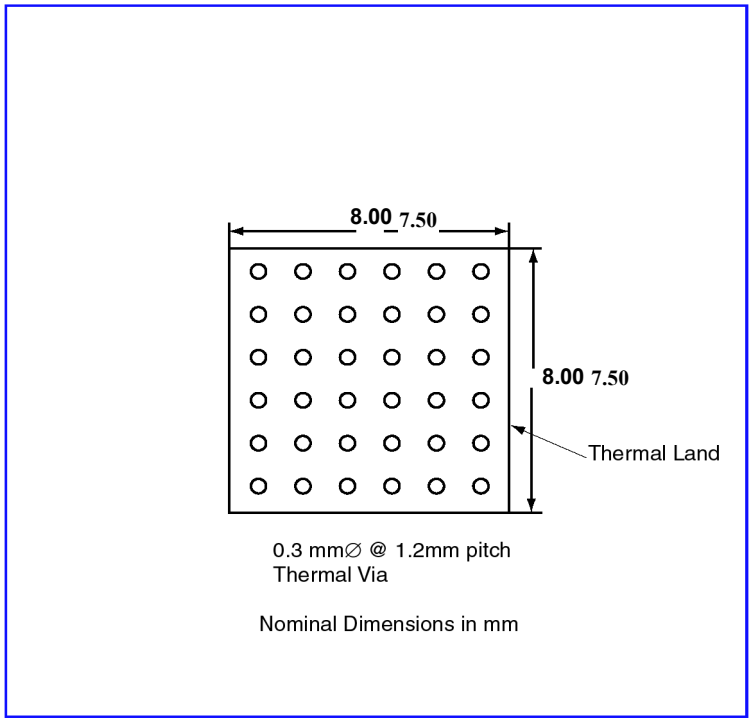


Figure 16. Thermal Pad Via Grid

Board Mounting Guidelines

The following are general recommendations for mounting exposed pad leadframe devices on the motherboard. This should serve as the starting point in assembly process development and it is recommended that the process should be developed based on past experience in mounting standard, non-thermally enhanced packages.

Stencil Design

For improved heat transfer, the exposed pad on the package may be soldered to a thermal land on the PCB. This requires solder paste application not only on the pad pattern for lead attachment but also on the thermal land using the stencil. While for standard (non-thermally enhanced) leadframe based packages the stencil thickness depends on the lead pitch and package coplanarity only, the package standoff also needs to be considered for the thermally enhanced packages to determine the stencil thickness. For a nominal standoff of 0.1 mm, the stencil thickness of 5 to 8 mils (depending upon the pitch) should still provide good solder joint between the exposed pad and the thermal land. The aperture openings should be the same as the solder mask opening on the thermal land. Since a large stencil opening may result in poor release, the aperture opening can be subdivided into an array of smaller openings, similar to the thermal land pattern shown in Figure 17. Recommended Stencil Design. The above guidelines will result in the solder joint area to be about 80 to 90% of the exposed pad area.

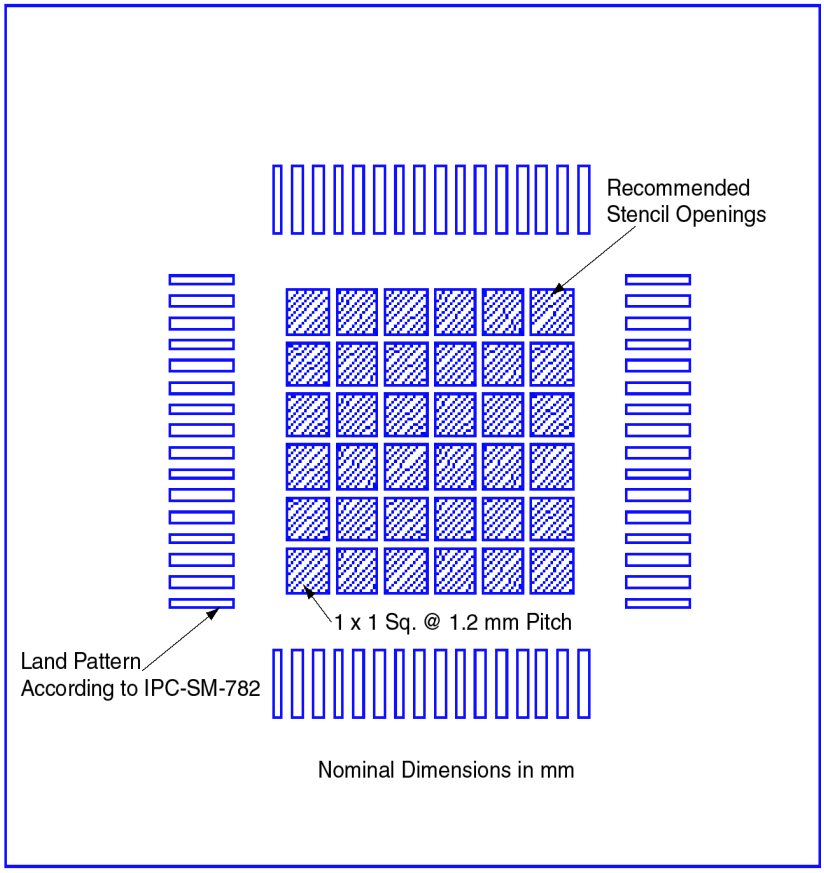


Figure 17. Recommended Stencil Design

Appendix B – Designing In SiI169 Using SiI159

The SiI159 is being made available in Engineering Sample form for customers designing in the SiI169. The devices are functionally the same with a few exceptions that are noted here. The main differences are:

- SiI169 Integrated HDCP Keys
- Pin compatibility (pins 40, 41, 84, 100)
- SiI169 HDCP operation over 100MHz
- SiI169 Bandwidth

SiI169 Integrated HDCP Keys

The SiI159 uses an external E^2PROM to store the HDCP keys. In the SiI169 these keys are integrated into the device and pre-programmed with either public or production HDCP keys. The two pins used for the I^2C interface to the E^2PROM are replaced and used for configuration pins as described in Table 5.

Pin Compatibility

There are a few pin differences between the SiI159 and SiI169. The primary difference is the absence of the master I^2C interface to the HDCP E^2PROM as this is now integrated into the SiI169. The SiI169 is intended only for use in HDCP applications so the MODE pin has been eliminated and replaced with AVCC for compatibility with the SiI161B. The OCK_INV pin has been moved to pin 41. The default setting should tie the pin LOW. The SiI169, like the SiI161B, has an internal HSYNC de-jitter circuit. Pulling pin 40 HIGH turns ON this circuitry. The pin differences are summarized in Table 5.

Table 5. Pin Differences Between SiI159 and SiI169.

Pin Number	SiI159		SiI169	
	Pin	Notes	Pin	Notes
40	CTL1/KSCL	I^2C clock to HDCP E2PROM, CTL1 if MODE = HIGH	HS_DJTR	Turns on/off HSYNC de-jitter circuitry, tie pin LOW to turn off
41	CTL2/KSDA	I^2C data to HDCP E2PROM, CTL2 if MODE = HIGH	OCK_INV	Use to invert the output clock. Default by tying LOW.
84	MODE	Selects HDCP or SiI151B (Receiver only) operation	AVCC	Device always in HDCP mode, compatible with SiI161B pinout
100	SCL/OCK_INV	SCL required for HDCP use, OCK_INV only usable if MODE = HIGH	SCL	SCL required for HDCP operation, OCK_INV on pin 41

SiI169 HDCP Operation Over 100MHz

The SiI169's HDCP decryption circuitry can operate over the full-range of the receiver core (25-165 MHz). This compares to the SiI159 which HDCP circuitry should not be used above 100 MHz.

SiI169 Bandwidth

The SiI169 TMDS receiver core operates over the full DVI bandwidth of 25 – 165 MHz. The SiI159's receiver core is only specified for operation up to 112 MHz.

Application Information
To obtain the most updated Application Notes and other useful information for your design application, please visit the Silicon Image web site at ***www.siimage.com***, or contact your local Silicon Image sales office.

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Revision History

Revision	Date	Comment
0.96	2/02	Initial release of SiI169 datasheet with integrated HDCP keys

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www.panellink.com

Customer:

SAMSUNG ELECTRONICS CO., LTD.

Attention:

Your ref. No.:

Your Part No.:

No. D030007 (1/)

Date: Feb. 05, 2003

SPECIFICATIONS

ALPS
MODEL : TDHU2-004A

Spec. No. :

Sample No.:

RECEIPT STATUS
RECEIVED
By. Date
Signature
Name
Title

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Sales

ALPS PRODUCT SPECIFICATION

TEMPORARY SPECIFICATION

DIGITAL and ANALOGUE FRONT-END MODULE

MODEL NUMBER: TDH (8-VSB , QAM , NTSC)

CUST. MODEL NO.	ALPS MODEL NO.

					DSGD.	
					CHKD.	TITLE TDHU PRODUCT SPECIFICATION
					APPD.	(1/ 14)
SYMB.	DATE OR NO.	APPD.	CHKD.	DSGD.	**ALPS ELECTRIC CO., LTD.**	

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1. TECHNICAL SPECIFICATION

ITEM No.	ITEM	Condition
1-1	Input	
	· Input Frequency Range	54MHz to 864MHz
	· Channel Bandwidth	6MHz
	· Channel Assignment	US Standard
	· Input Signal Level	-80dBm to -20dBm (8-VSB) -15dBmv to +15dBmv (64 QAM) -12dBmv to +15dBmv (256 QAM)
	· Input Impedance	75 ohms nominal
	· Modulation Modes	8VSB / 64QAM / 256QAM / NTSC
1-2	Output	
	· Output Format	Digital ch. : MPEG-2 Transport Stream in serial All Digital Outputs are 3.3V CMOS levels Refer to the NXT2004 Data Sheet and API Manual. Analogue ch. : CVBS , AF Audio output and 2nd SIF output (4.5MHz)
	· Output Impedance	Analogue ch. : Video output load : 10k ohms : S-IF output load : 100k ohms
1-3	Control format	IIC Compatible Interface NXT2004 Slave core, whose I/O operates at 3.3V or 5V tolerant. Refer to the NXT2004 Data Sheet and API Manual. (Appendix, "Program Tuner PLL Channel Change") The reference frequency step of the Tuner section PLL is 62.5kHz. X'tal: 4MHz, Reference divider: 64, IF center frequency: 44MHz
1-4	Power Supply Voltages	Pin Number / Operating Supply Voltages 3 / B2(+5V) +5.0V±0.25V DC 5 / B3(+32V) +32V±1.6V DC 12 / B4(+3.3V) +3.3V±0.3V DC 14 / B5(+2.5V) +2.5V±0.25V DC 15 / B6(+1.2V) +1.2V±0.12V DC

1. TECHNICAL SPECIFICATION

ITEM No.	ITEM	Condition
1-5	Current Consumption	Pin Number / Typ. / Max. 3 / B2(+5V) / 240mA / 360mA 5 / B3(+32V) / – / 2mA 12 / B4(+3.3V) / 17mA / 60mA 14 / B5(+2.5V) / 150mA / 260mA 15 / B6(+1.2V) / 170mA / 250mA
1-6	Environmental Specifications	
1-6-1	Temperature	Operating 0 to +60℃ Storage -10 to +70℃
1-6-2	Humidity	Operating Less than 80 % RH(at40℃) Storage Less than 95 % RH(at40℃)

2. Standard Test Conditions

Test for electrical specification shall be performed at following at following condition unless the otherwise specified.

ITEM No.	ITEM	CONDITION
2-1	Ambient Conditions	Temperature 25±2 deg C Humidity 65±5% RH
2-2	Power Supply	Pin Number Operating Supply Voltages 3/B2 (+5V) +5.0V ±0.1V DC 5/B3 (+32V) +32V ±0.1V DC 12/B4 (+3.3V) +3.3V ±0.1V DC 14/B5 (+2.5V) +2.5V ±0.1V DC 15/B6 (+1.2V) +1.2V ±0.1V DC

3. Absolute Maximum Voltage

ITEM No.	ITEM	CONDITION
3	Absolute Maximum Voltage	Pin Number Maximum Voltages 3/B2 (+5V) +5.5V DC 5/B3 (+32V) +34V DC 12/B4 (+3.3V) +3.6V DC 14/B5 (+2.5V) +2.75V DC 15/B6 (+1.2V) +1.32V DC

4. Electrical Specifications

ITEM	SPECIFICATION				CONDITION
	MIN.	TYP.	MAX.	UNIT	
4-1 **RF Input Specification**					
4-1-1 ANT Input Return Loss		6		dB	50 to 864MHz
4-1-2 ANT Leakage			 46 54	 dB dB	Other terminal should be Termination (75ohms) 30 - 950MHz 950 - 1750MHz
4-1-3 LO Phase Noise		90		dBc/Hz	@ 10kHz offset

4. Electrical Specifications

ITEM	SPECIFICATION				CONDITION
	MIN.	TYP.	MAX.	UNIT	
4-2 Digital Output Specification ATSC (8-VSB)					Note: All item is judged by TOV
4-2-1 Input Sensitivity		-80		dBm	
4-2-2 Dynamic range		90		dB	
4-2-3 Image NTSC Interference Protection Ratio		-45		dB	Desire Input Level -68dBm
4-2-4 Adjacent NTSC Interference Protection Ratio		-37 -37		dB	〈N -1〉 @-68dBm 〈N+1〉 @-68dBm
4-2-5 Co-Channel NTSC Interference Ratio		2		dB	Desire Input Level -48dBm
4-2-6 AWGN Condition		15.4 15.5		dB	@-48dBm @-68dBm
4-2-7 Static Multipath		1.0 1.8		dB	@ 1μS @15μS
4-2-8 Dynamic Multipath		1.4		dB	@ 1μS @ 5Hz
4-2-9 Acquisition time		200		mS	This time is between send channel data and MPEG2 DATA Output. Typ. time is the average of 10 times.

NOTE : measurement condition

<Desired signal discription>

Input Discription : 8-VSB

<Undesired signal discription>(ITEM 4-2-3~5)

NTSC : Video 75% color bars FM sound : 400Hz tone (level P/S : 7dB, ±25kHz deviation)

<The judge point>(ITEM 4-2-1,3~8)

TOV(BER of 3×10^{-6} at TS output)

4. Electrical Specifications

ITEM	SPECIFICATION				CONDITION
	MIN.	TYP.	MAX.	UNIT	
4-3 Digital Output Specification FAT (QAM / ITU-J.83B)					
4-3-1 Input Level Range	-15		+15	dBmV	
4-3-2 AWGN Condition		23.0		dB	C/N for TOV Note 1.
4-3-3 Inter Modulation condition		23.5		dB	C/N for TOV Note 2.

Note 1.

Channel assumption:

1 desired digital 64 QAM channel at RF input level of +10 dBmV

Note 2.

Channel assumption:

1 desired digital 64 QAM channel at RF input level of +10 dBmV,
and 135 undesired analogue AM-VSB cannels at RF input level of +15 dBmV.

4. Electrical Specifications

ITEM	SPECIFICATION MIN.	TYP.	MAX.	UNIT	NOTE
4-4 Analogue Output Specification					
4-4-1 Video Output Level	0.80	1.00	1.20	Vp-p	Standard color bar : 87.5 % mod. RF inputlevel : 70dBμV P/S level : 6dB
4-4-2 Video S/N	42.0			dB	100 % white signal 87.5 % modulation Subcarrier trap : ON HPF : 100 Khz , LPF : 4.2 MHz ANT input level : 70dBμV P/S level : 6dB
4-4-3 Noise Limiting Sensitivity			50.0	dBμV	100 % white signal 87.5 % modulation Subcarrier trap : ON HPF : 100 kHz , LPF : 4.2 MHz Video S/N = 30 dB P/S level : 6dB
4-4-4 Video Frequency Characteristics [CH:12]					Full sweep : 87.5 % mod. Based on 100 kHz Input Level : 70dBμV P/S level : 6dB
1.0 MHz		0		dB	
2.0 MHz		0			
3.0 MHz		0			
3.58 MHz		-1.0			

ITEM	SPECIFICATION				NOTE
	MIN.	TYP.	MAX.	UNIT	
4-4-5 Differential Gain	-10		+10	%	10 stair-steps: 87.5 % mod. Set modulation at the peak of 10 th chroma signal. Input level : 70dBμV
4-4-6 Differential Phase	-10		+10	deg	
4-4-7 Audio Output Level		480		mVrms	400 Hz / ±25 kHz Dev. Standard color bar : 87.5 % mod. De-emphasis : ON RF input level : 70dBμV P/S level : 6dB
4-4-8 Audio Distortion			2	%	400 Hz / ±25 kHz Dev. Black burst signal : 87.5 % mod. De-emphasis : ON RF input level : 70dBμV P/S level : 6dB
4-4-9 Audio S/N		55		dB	400 Hz / ±25 kHz Dev. Standard color bar : 87.5 % mod. De-emphasis : ON P/S = 6 dB RF input level : 70dBμV P/S level : 6dB
4-4-10 SIF output level (4.5MHz)		360		mVp-p	Video Standard color bar : 87.5% mod Audio : No modulation RF input level : 70dBμV P/S level : 6dB

5. Mechanical Information

5-1. Module Pin Information.

Pin No.	Definition	Purpose	Note
1	N/C	No connection	This terminal MUST be keep OPEN
2	RF AGC	RF AGC	This terminal is used for the monitoring RF AGC voltage.
3	B2 +5V	Power Supply	For the MOPLL IC.
4	AFT OUT	Analogue Output	AFT S curve output.
5	B3 +32V	Power Supply	For the Tuning.
6	GND	GND	Tie to GND plane
7	RESET	Module Control	Resets the module to default configuration. Active low.
8	ERROROUT	MPEG-2 Interface	Transport stream error. The current packet contains uncorrectable error.
9	VIDEO	Analogue Output	Composite video base band signal output
10	Ana_SW	X-TAL ON/OFF	Analog function is high
11	SIF	Analogue Output	2ndSIF output.
12	B4 +3.3V	Power Supply	For I/O of the VSB/QAM demodulator IC
13	GND	GND	Tie to GND plane
14	B5 +2.5V	Power Supply	For Core of the VSB/QAM demodulator IC
15	B6 +1.2V	Power Supply	For Core of the VSB/QAM demodulator IC
16	PKT SYNC	MPEG-2 Interface	Indicates the beginning of a transport package by asserting PSYNC during the sync byte of the message. Active high.
17	MD_EN	MPEG-2 Interface	MPEG Data Enable out, this signal indicates when the MPEG output data is valid. Active high.
18	M_DATA_7	MPEG-2 Interface	Parallel MPEG Data 7 Output
19	M_DATA_6	MPEG-2 Interface	Parallel MPEG Data 6 Output
20	M_DATA_5	MPEG-2 Interface	Parallel MPEG Data 5 Output
21	M_DATA_4	MPEG-2 Interface	Parallel MPEG Data 4 Output
22	M_DATA_3	MPEG-2 Interface	Parallel MPEG Data 3 Output
23	M_DATA_2	MPEG-2 Interface	Parallel MPEG Data 2 Output
24	M_DATA_1	MPEG-2 Interface	Parallel MPEG Data 1 Output
25	M_DATA_0	MPEG-2 Interface	Parallel MPEG Data 0 Output
26	M_CLOCK	MPEG-2 Interface	The clock synchronizes the data stream. The clock signal is pulsed each time a valid data word is output on the DATA 0-7 .
27	SDA	I^2C Bus Interface	I^2C Serial Data Line
28	SCL	I^2C Bus Interface	I^2C Serial Clock Line

ITEM No	ITEM	Specification
5-2	Appearance Structure	Dimensions as mechanical drawing
5-3	RF Input Connector Form	RCA Type
5-4	Weight	70g Typ.

6. Appendix

Program Tuner PLL Channel Change.

	MSB							LSB			Hex.
ADDRESS	1	1	0	0	0	MA1	MA0	0	A	Byte1	
EX)	1	1	0	0	0	0	1	0			C2
PROGRAMMABLE DIVIDER	1	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	Byte2	
EX)	0	0	1	0	0	0	0	0			20
PROGRAMMABLE DIVIDER	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	Byte3	
EX)	0	1	0	1	0	0	0	0			50
CONTROL DATA	1	X	X	AGD	R3	R2	R1	R0	A	Byte4	
EX)	1	0	0	0	0	1	0	1			85
CONTROL DATA	C1	X	RE	RST	BS4	BS3	BS2	BS1	A	Byte5	
EX)	0	0	0	0	1	0	0	0			08

EX)

Programmable data = (Desired channel center frequency) + 44M / (4M / 64)

= (473(CH14)+44) M / 62.5k

= 8272 (Dec.)

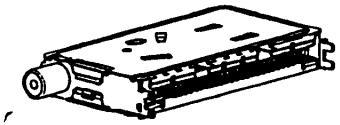
= 010 0000 0101 0000 (15 bits)

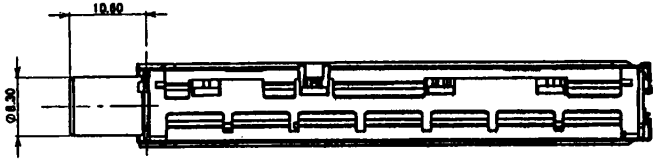
= 2050 (Hex.)

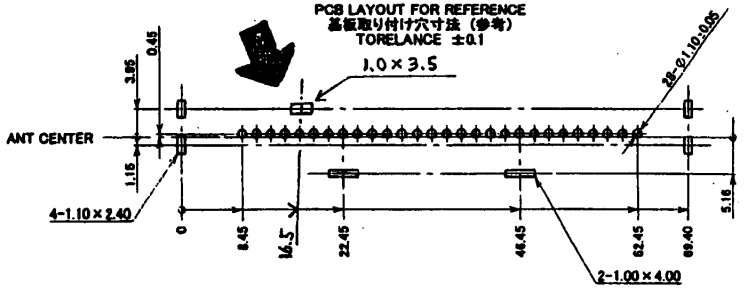
Byte 5 for charge pump current and port setting

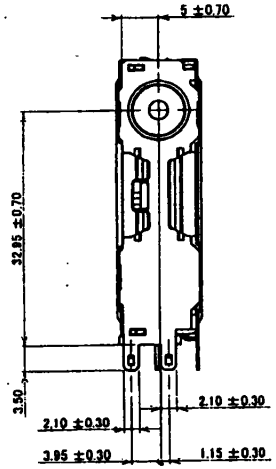
CONTROL DATA	C1	X	RE	RST	BS4	BS3	BS2	BS1	A		Hex.
54MHz – 162MHz	0	0	0	0	0	0	0	1			01
162MHz – 426MHz	0	0	0	0	0	0	1	0			02
426MHz – TBDMHz	0	0	0	0	1	0	0	0			08
TBDMHz – 864MHz	1	0	0	0	1	0	0	0			88

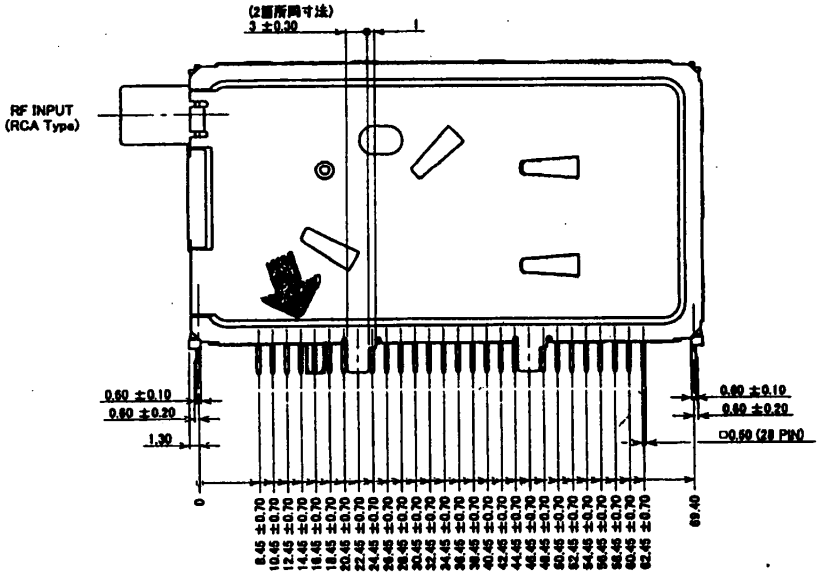
2003/01/07(TUE) 19:06:14

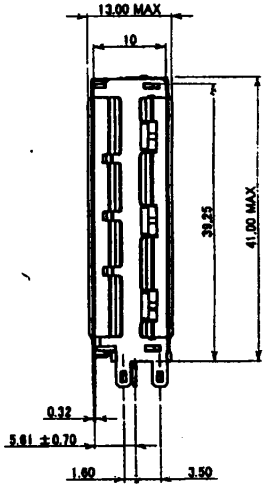


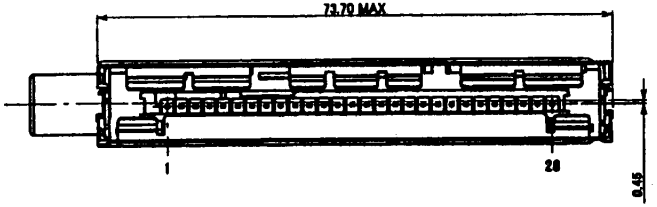












TERMINAL ASSIGNMENT

1	N/C
2	RF AGC
3	B2 +5V
4	AFT OUT
5	B3 +32V
6	GND
7	POWER RESET
8	MPEG ERROR
9	VIDEO OUT
10	~~±VIDEO OUT~~ x-tal off SW
11	SIF OUT
12	B4 +3.3V
13	GND
14	B5 +2.5V
15	B6 +1.2V
16	MPEG PKT SYNC
17	MPEG DATA EN
18	MPEG DATA 7
19	MPEG DATA 6
20	MPEG DATA 5
21	MPEG DATA 4
22	MPEG DATA 3
23	MPEG DATA 2
24	MPEG DATA 1
25	MPEG DATA 0
26	MPEG DATA CLK
27	SDA
28	SCL

NOTE

1 TOLERANCES ARE ±0.5mm, UNLESS OTHERWISE SPECIFIED.

2 THE PITCH BETWEEN TERMINALS IS SPECIFIED AT THE ROOT.

3 DATE CODE No. IS CONFORMED TO ALPS STANDARD SPECIFICATION.

4 ALPS CAN ALTER COVER HOLE DESIGN WITHOUT NOTICE IF NO ELECTRICAL DEGRADATION.

5 THE PRINTING IS ON LABEL.

CUST. MODEL No.	TDHU
ALPS MODEL No.	

PART NO.	NAME	MATERIAL	SPEC.	FINISH

ALPS ELECTRIC CO., LTD.

DSGD. Jan. 7, '03 S.Iimura	SCALE 2:1	TDH
CHKD.		TITLE ASSEMBLY DRAWING
APPD. Jan. 7, '03 T.Saito	UNIT mm	DOCUMENT NO.

ZONE | SYMB | DATE OR NO. | APPD. | CHKD. | DSGD.

KEY No.

(A2・図面用紙)